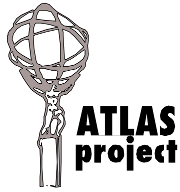

ATLAS Project Document No.	*Institute Document No.*	*Created:* **17/07/00**	*Page:* **1 of 7**
ATL-xx-xx-xxxx		*Modified:* **dd/mm/yy**	*Rev. No.:* **A**

Project breakdown name

Design changes in the Cu/Polyimide barrel hybrid version 4

abstract

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Distribution List

SCT

History of Changes

Rev. No.	***Date***	***Pages***	***Description of changes***
A	17/07/00	All	First version
	19/07/00	4	Description of "tempret" and "DGNDsense"
	19/07/00		Electrical schematics and layer layouts approved

1 Introduction

The ATLAS SCT uses Cu/Polyimide flex circuit hybrids for the barrel and the forward sections. The hybrids have been developed for the readout ASIC, ABCD, which has been evolved as ABCD1, ABCD2T, and ABCD3T as of this document. Because of distinct difference of the geometrical configuration of the hybrid in the SCT barrel and forward modules, the barrel as "centre-tap" and the forward "end-tap", the hybrid for each type of module has been developed in the barrel and the forward community in parallel. This document covers the barrel hybrid. The barrel module configuration is shown in the drawing, "ATLAS SCT barrel module".

Following the successful operation of "full" modules with 12 chips of ABCD2T, the Hybrid Design Review was held at CERN on 22nd June, 2000 to review the Barrel Hybrids in depth. The version 3 was the version of the barrel hybrid at the time. The review, in summary [1], has recommended several features to be implemented in the next round of fabrication of the hybrids for the module-0. In response, the hybrid design has been updated for the version 4 and specified herein.

2 Electrical schematics

The updated schematics is shown in the figures (2 pages), "Circuit Diagram of Barrel Cu/Polyimide Hybrid for ABCD3T chips". The changes implemented over the version 3 are:

2.1 Connector pin assignment

The recommendation is

"keep the current 36-pin connector and minimize the number of changes to the current pin assignment. Remove unused pins, and

pin14 to AGND (to allow up to 4 AGND connections)

pin13 to VCC

pin7 to remain unallocated as a potential temperature return line".

Changes are made to

pin14 to AGND

pin13 to VCC

pin7 to tempret (see below).

2.2 Temperature sensing and DGND-sensing

Concerns are expressed in several paragraphs on the temperature sensing and DGND sensing. The arguments are a bit complicated:

1. The temperature reading and the DGND potential, when they are sensed at the mating connector, have uncertainty due to the voltage drops generated by the ASIC currents between the hybrid and the point of sensing. Both uncertainties are calculated to be acceptable, <0.5 K in the temperature reading and <40 mV in the DGND potential [2]. Although acceptably small, an introduction of a line can service for reducing both uncertainties.

2. There is an express of concern on the introduction of noise from the temperature sensing circuitry into DGND when the temperature return and the DGND are connected. A separate temperature return may evade the noise issue.
3. Introduction of lines must be minimized since it is an "real-estate" trade-off. The first and the second arguments are incompatible with the connection of the line to DGND.

Careful examination allows to introduce one line into the hybrid without compromising the real-estate. Thus, the change is

> A separate line for "temperature return (tempret)" of Temp1 and Temp2 sensors, being connected to the pin7 (tempret), and an optional wire-bonding pad between the tempret line and DGND near the middle of the 12 chips hybrid.

If we tie "tempret" to DGND at the hybrid, the "tempret" must be used as "DGNDsense" in the dogleg; no tie of "DGNDsense" and DGND in the dogleg is required. If we do not tie "tempret" and "DGNDsense" together on the hybrid, they must be tied in the dogleg at the point where "DGNDSense" is tied to DGND. If no-connection of the "tempret" and DGND minimizes the noise from the temperature circuitry, the "tempret" should go to the temperature circuitry separately, without connecting to "DGNDsense" in the dogleg and after; "DGNDsense" is tied to DGND in the dogleg.

2.3 Option for connecting ID4 to either SELECT or VDD

ID4 has a pull-down resistor inside the ABCD chip and the module is served by primary fibre. In case the module is required to be served by an adjacent fibre, the ID4 is set by SELECT-high. An option is requested to set the ID4 high without SELECT-high connection.

Change is

> A VDD wire-bonding pad is provided next to the SELECT line pad.

3 Layer structure

Layer structure of the hybrid is shown in the drawing of "Layer structure of the Cu/Polyimide Flex Circuit Version 4". The technology uses "adhesive-less" Cu/Polyimide sheet to build up the flex circuit. The centre core, double-sided Cu/Polyimide sheet, extends the full length of the circuitry, from the connector to the far-end hybrid. A pair of single-sided Cu/Polyimide sheets are glued on the centre core with an adhesive in order to form the four layer structure in the hybrid section; Cu is removed in the cable section to have the two layer structure. Through-holes and via's are inter-connecting between the layers: though-holes between the top (L1) and the bottom (L4) layers including inner ones; via's formed with a laser between the top and the second layer (L2) and, equally, the bottom and the second bottom layer (L3). Function of the layers are

- L1 Traces traversing the longitudinal bus lines, bonding pads/lines, and ground/shield plane
- L2 Longitudinal bus lines (in the hybrid section), in addition to the power lines (in the cable section)
- L3 Ground planes all-through the circuit

L4 Power supply planes (in the hybrid section), and ground windows

No change in the version 4 from the version 3.

4 Layer layouts

Layer layouts of the version 4 are shown in the drawings of “Layer layouts of the Cu/Polyimide Flex Circuit Version 4 (two pages)”. L1 to L4 show the layers from the top to the bottom. L1MASK is the solder mask on the top layer. L4COVER is the cover film on the bottom layer. The middle figure in the second page is the silk screen of the passive components. Changes from the version 3 to the version 4 are briefed in below:

4.1 Pin assignment, temperature/DGND sensing, and SELECT/Vdd to ID4

The layout changes corresponding to the schematics changes in the section 2 are implemented (see the layouts).

4.2 Alignment holes

There are four holes for alignment over the full layout. The purpose of the hole has changed from securing the hybrids on the module with bolts and nuts to only for alignment. Accordingly, the recommendation was

“Reduce the size of alignment holes and move either closer to the split between analogue and digital buses or closer to the other via’s... The aim is to minimize the AGND impedance.”

The change is

1. to reduce the size, and
2. to move the hole locations. All hole locations are 8.5 mm from the front edge of the hybrid. The top and the bottom holes were used to match when the hybrid was folded. The new hole location does not match and not need to because there will be no through-bolts.

4.3 Split between the digital and the analog grounds

The layer 3 has AGND and DGND bus being split. The via’s are arranged to bring up the AGND and DGND on to the top surface for “stitching” the two grounds. The AGND via’s are on the “divide” of the AGND side of split. The recommendation was

“Rearrange the split to ensure the via’s are fully located in the analogue ground”.

The change is

the split is narrowed to 200 μm in order to contain the via’s in the AGND plane.

4.4 Fiducial marks

The recommendation was

“The fiducials required on the hybrids and fan-ins by the module builders and wire-bonders should be added”.

Fiducial marks “+” are already on the hybrid for aligning the fan-ins. Fiducial marks are already on the fan-ins. The remaining change is

Fiducial marks "+" are placed around the four corners of each chips.

4.5 Minimum line and gap widths

There are number of bonding pads in the back-end of the ABCD3T chips. The minimum pitch of the pads are 180 µm. The industry's recommendation for the minimum gap of the mask is 80 µm, in the large scale mass production. This is said to ensure the straight and clean cut of the etched edges and non-existence of metal residue. After etching, the resulting gap width is widened than the mask and the tolerance recommended is -0/+20 µm. The resulting line width is 100 +0/-20 µm for the 180 µm pitch pads.

The request from the wire-bonding is to have the line width of 80 µm minimum.

The minimum line and the gap widths with tolerance are specified as

line: 100 +0/-20 µm, gap: 80 -0/+20 µm.

4.6 Stiffener in the area of connector

A concern was expressed, "A stiffener may be needed in the area of the connector. Advice should be asked for from the vendor."

The vendor has confirmed that the four layer structure in the area of the connector is adequate without a stiffener. Accordingly, no further stiffer is designed. The reliability will be tested in the pre-series.

4.7 Option to increase the Vcc/Vdd by-pass capacitors

The recommendation for the issue is

"The option should be pursued to increase the values by 2 of the Vcc/Vdd bypass capacitors in case the large in variations in digital current cause problems. There might also be gains to be realized from choosing capacitors with an optimised frequency response (it was claimed that X5R range has higher values). Provision should be made for adding extra capacitors if it can be done without compromising the layout."

1. The area between the chips is tight. A major rework is anticipated in order to put two capacitors in parallel or one size larger capacitors.
2. Effectiveness of the increase by 2 is unknown. The 12 ABCD2T chips in module did not cause problem for the large digital current variation, passing through the noise peak, with the current 100 nF capacitors.
3. From the candidate supplier of the capacitors, Murata, there is no bigger capacitors than 100 nF in the size of EIA0603 (1.6 mm x 0.8 mm). There are if one size larger, EIA0805 (2.0 mm x 1.25 mm), e.g., 470 nF (thickness 1.25 mm).
4. The difference in definition of X7R and X5R is the temperature characteristics: X7R for -55 to +125 °C, and X5R for -55 to +85 °C, for the capacitance change of ±15%. In some EIA sizes, there are capacitors having larger values in X5R, but not in EIA0603 nor EIA0805 with the voltage rating over 16 V.

From the above observations, no change is made on the layout of capacitors. We propose to stack the current EIA0603 capacitors on top in order to test the increase by 2. Once we know the ef-

fectiveness, the layout can be made to accommodate a larger size, EIA0805 capacitor, e.g.

5 Electrical specifications

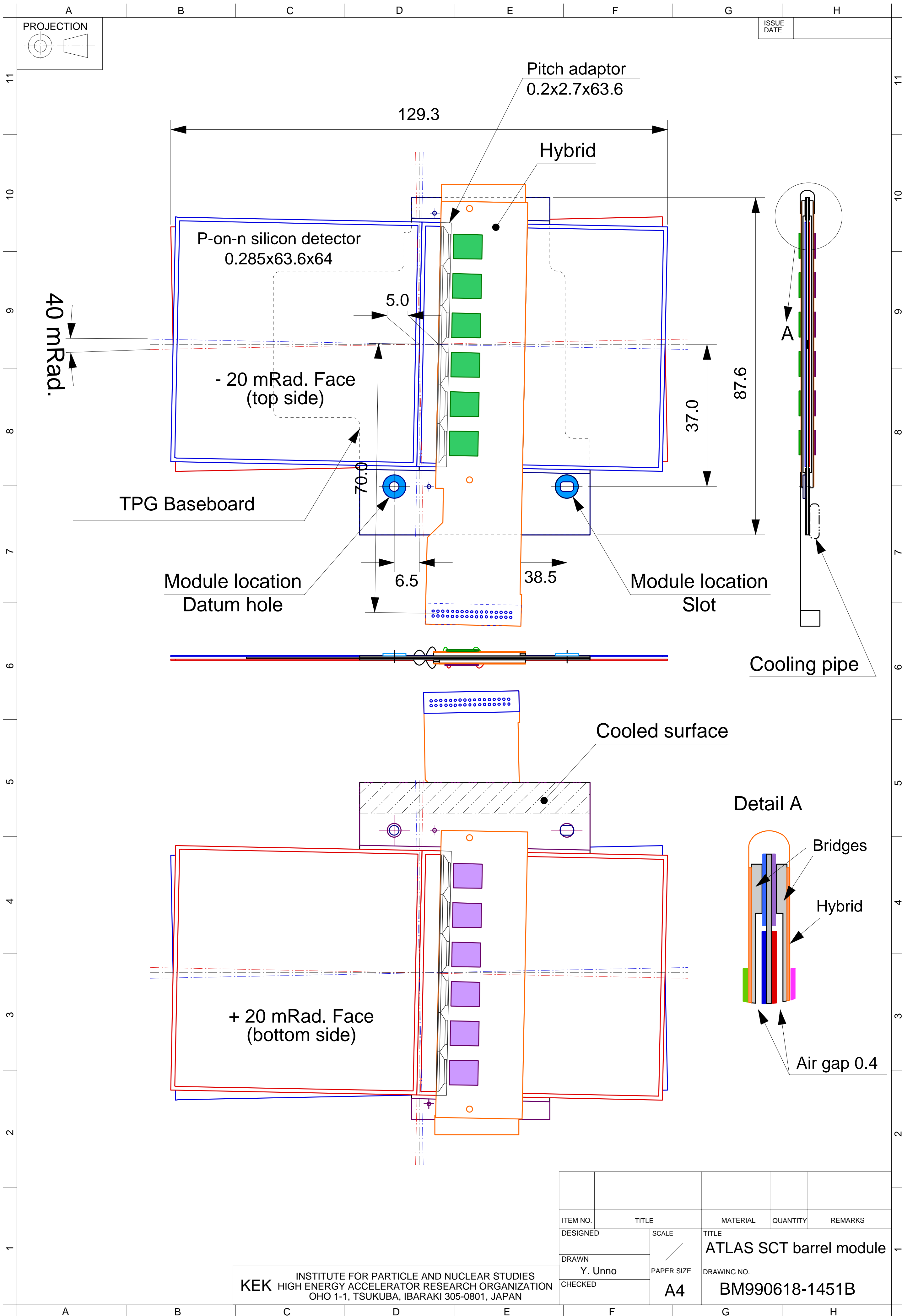
(Descriptions to be added)

No change.

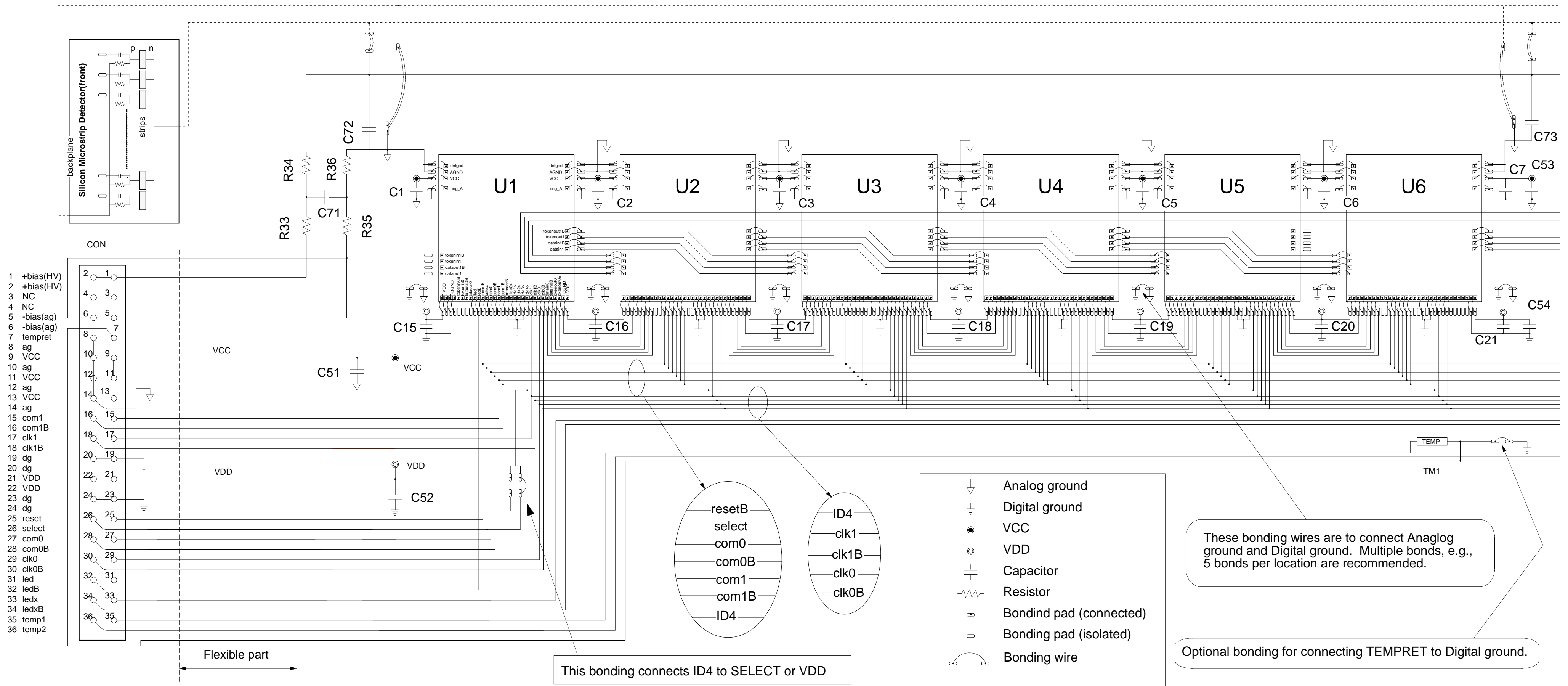
References

[1] M. Tyndel, et al., “Internal Design Review of the SCT Barrel Hybrids”, reference id, 5 July, 2000

[2] Y. Unno, et al., “Temperature readout errors in thermistors due to voltage ambiguities”, 29 June, 2000, http://atlas.kek.jp/~unno/si_hybrid/SMDparts/Temperrors.fm55.pdf



PROJECTION
ISSUE
DATE
Pitch adaptor
0.2x2.7x63.6
129.3
Hybrid
P-on-n silicon detector
0.285x63.6x64
5.0
40 mRad.
- 20 mRad. Face
(top side)
37.0
87.6
70.0
A
TPG Baseboard
Module location
Datum hole
6.5
38.5
Module location
Slot
Cooling pipe
Cooled surface
Detail A
Bridges
Hybrid
+ 20 mRad. Face
(bottom side)
Air gap 0.4
ITEM NO.
TITLE
MATERIAL
QUANTITY
REMARKS
DESIGNED
SCALE
TITLE
ATLAS SCT barrel module
DRAWN
Y. Unno
PAPER SIZE
DRAWING NO.
CHECKED
A4
BM990618-1451B
KEK
INSTITUTE FOR PARTICLE AND NUCLEAR STUDIES
HIGH ENERGY ACCELERATOR RESEARCH ORGANIZATION
OHO 1-1, TSUKUBA, IBARAKI 305-0801, JAPAN



1997.9.5 T. Kondo (KEK)
1997.9.6 V1
1997.10.10 V2
1998.1.25 V3
1998.4.10 V4
1998.4.12 V5
1998.5.8 V6 <-- Melbourune
1998.5.19 V7 <--Unno
1999.6.29 V8
1999.7.28 V8a
1999.12.1 V8b
1999.12.28 V8c
2000.1.15.V8d
2000.2.4 V8e
2000.2.9 V8f (5 -> 5.1 kohm)
2000.3.18 Helvetica font
2000.5.11 mistakes corrected
2000.7.12 new version for ABCD3T

Circuit Diagram of Barrel Cu/Polyimide Hybrid for ABCD3T chips

(ATLAS/K4ABCD3/2K09)

C74 C75

C8 C14

C55 C57

U7 U8 U9 U10 U11 U12

C9 C10 C11 C12 C13

C56 C22 C23 C24 C25 C26 C27 C28 C58

R27 100 Ohm
R28 100 Ohm
R29 100 Ohm
R30 100 Ohm

TEMP

TM2

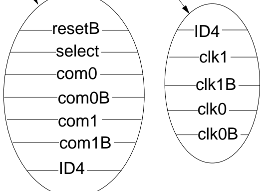
Flexible part

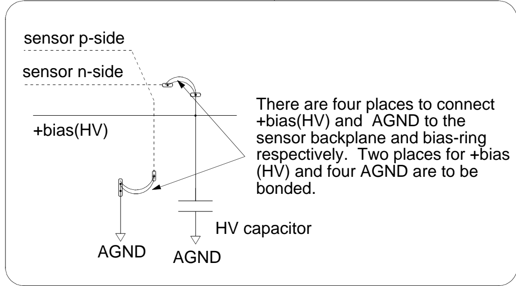
Silicon Microstrip Detector(back)

p n

strips

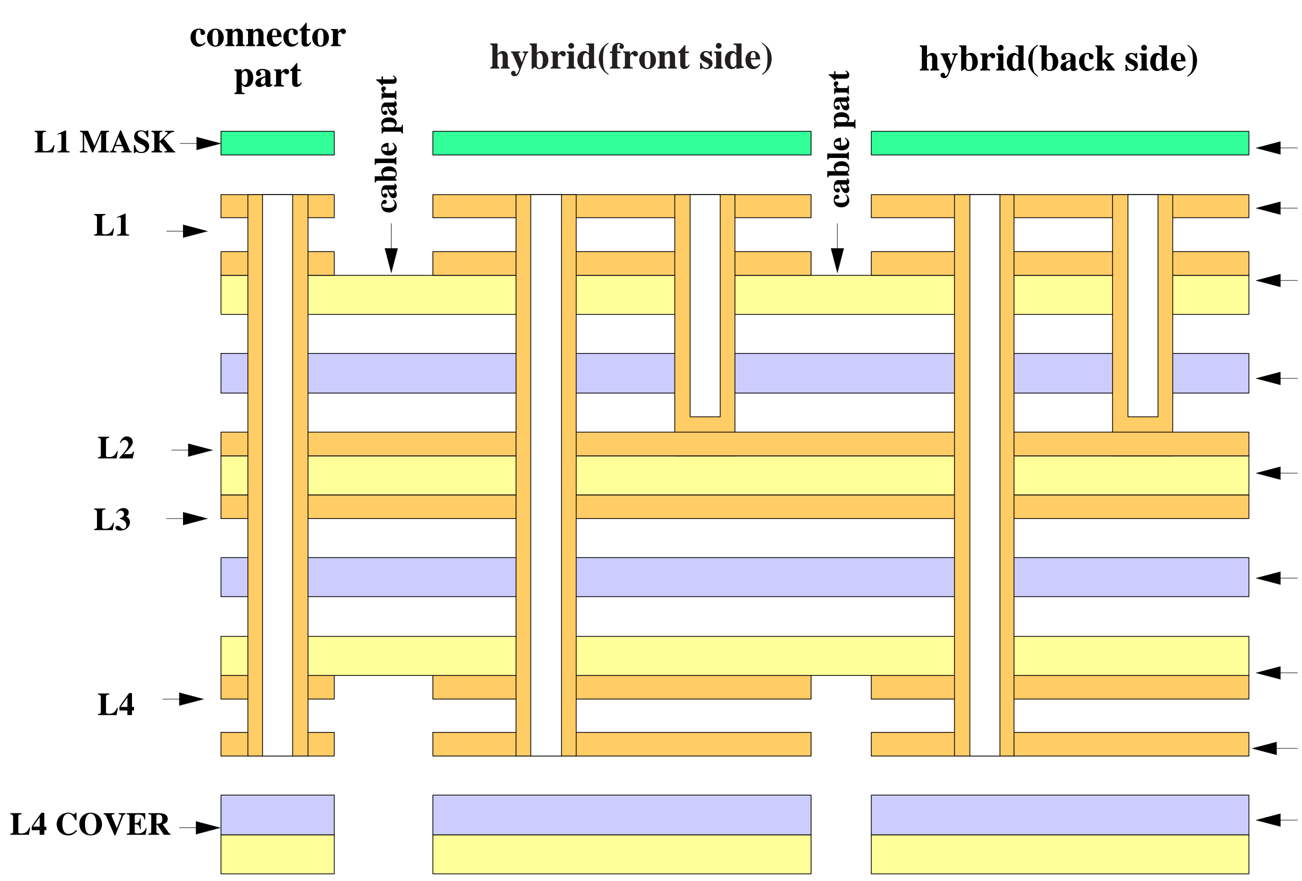
backplane





Parts list

part notation	total number	dimensions (mm)	specifications and part No.
U1 ~ U12	12	6.55 x 8.40	ABCD3T chip (version 1.1)
C1 ~ C28	22	1.6 x 0.8	100 nF, 25 V, Ceramic capacitor, Murata GRM39-X7R-104-K-25
C51 ~ C58	8	3.2 x 1.6	330 nF, 25 V, Ceramic capacitor, Murata GRM42-X7R-334-K-25
C71 ~ C75	5	3.2 x 1.6	10 nF, 630 V, Ceramic capacitor, Murata GHM1530-B-103-K-630
R27 ~ R30	4	1.6 x 0.8	100 ohm (termination of com and clock lines)
R33, R34	2	1.6 x 0.8	5.1 k ohm, resistor
R35	1	1.6 x 0.8	1 k ohm, resistor
R36	1	1.6 x 0.8	jumpering wire
TM1, TM101	2	1.6 x 0.8	10k thermistors, Semitec 103KT1608-1P
CON	1	1.27mm pitch	2 row x 18 pins connector, Samtec SFMC-140-L3-S-D

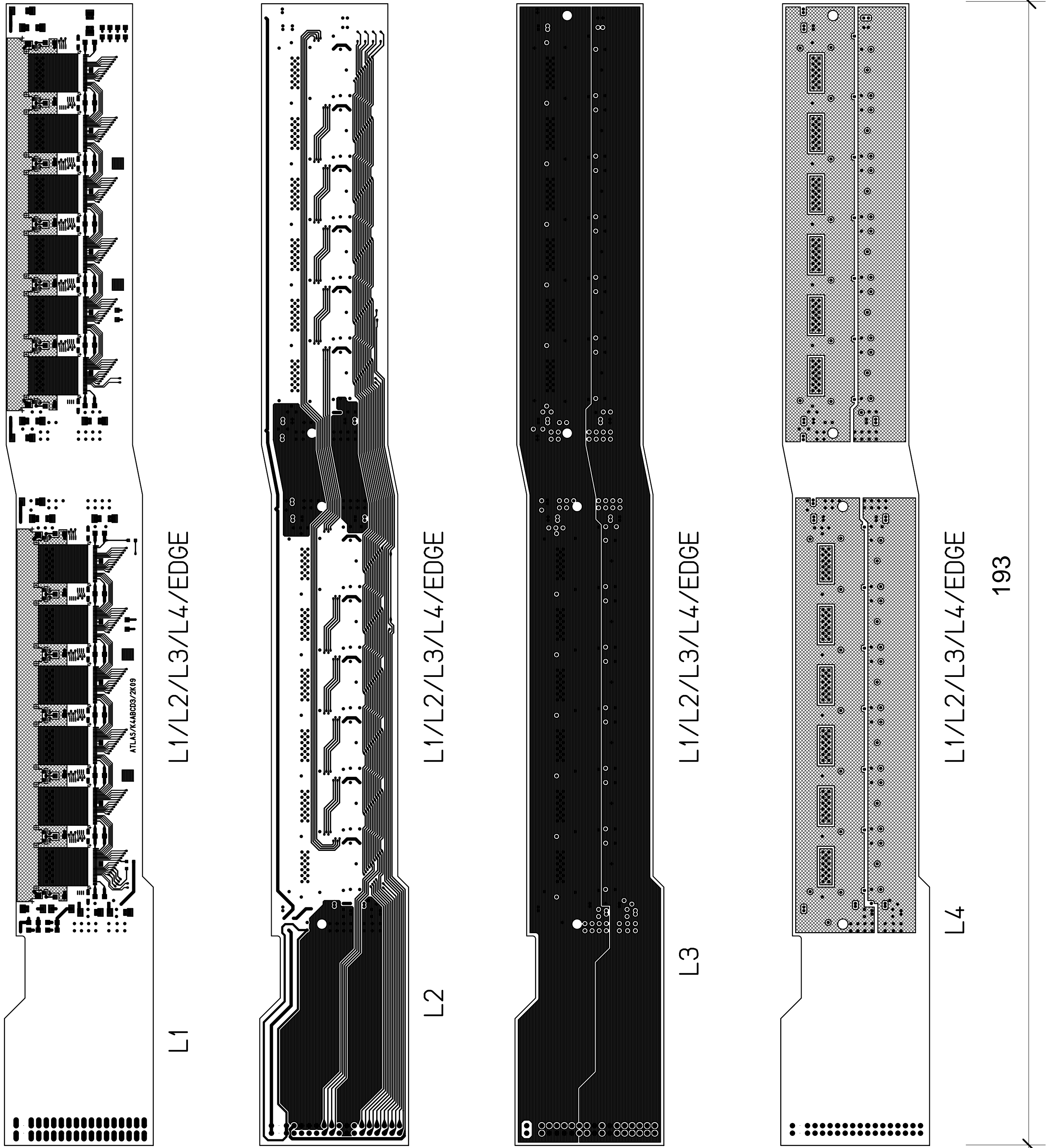


Material	Thickness µm
Photo-solder resist	20
Through-hole plating (50%mesh)	20
Polyimide-Copper(single-sided) 1/3 oz(12µm)Cu, 1 mil PI, Adhesive-less	37
Adhesive	25
Polyimide-Copper(double sided) 1/3 oz Cu, 1 mil PI, 1/3 oz Cu Adhesive-less	49
Adhesive	25
Polyimide-Copper(single-sided) 1/3 oz(12µm) Cu, 1 mil PI, Adhesive-less	37
Through-hole plating (50%mesh)	20
Polyimide cover film 1/2 mil, Adhesive 33 µm	46
Total : circuit part cable part	279 149
Surface treatment non-electroysis gold plating (0.3 µm Au, < 3 µm Ni)	

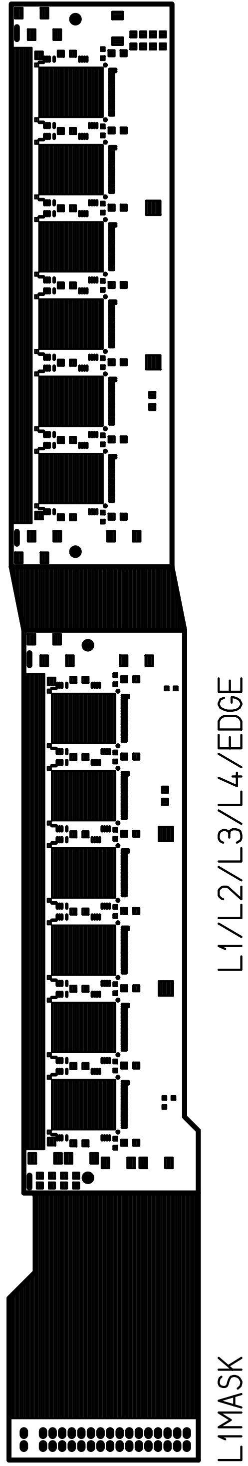
Cu/Polyimide surface build-up/high density interconnect technology:

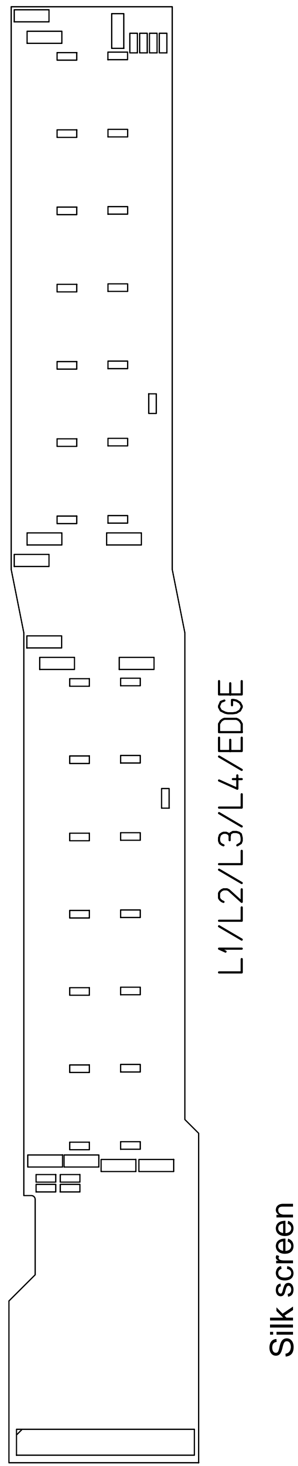
Through-hole 300 µm dia., Land 500 µm dia.
Lasar-via 150 µm dia., Land 300 µm dia., surface build-up
Min. line width 100 µm, min. gap 80 µm

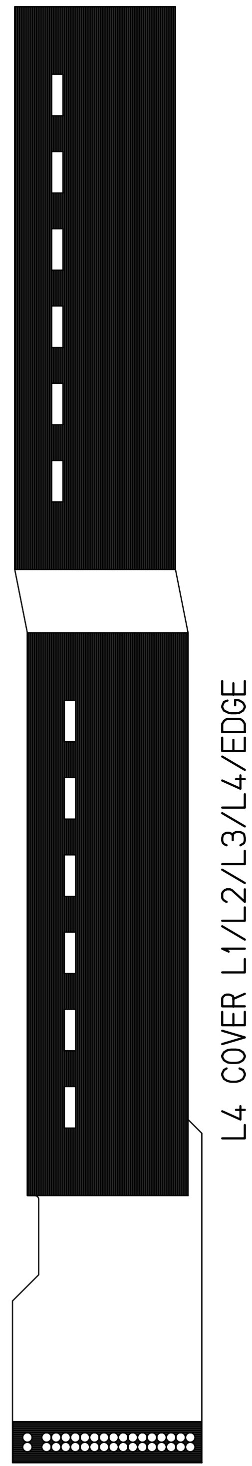
Layer Structure of the Cu/Polyimide Flex circuit version-4



Layer Layouts of the Cu/Polyimide Flex Circuit Version 4







Layer Layouts of the Cu/Polyimide Flex Circuit Version 4