Hybrid/Module Production Test Results

A. Ciocio - LBNL

Status - Hybrids

Hybrids Built	Hybrids tested OK	Hybrid on hold	Hybrids burn-in	Hybrids fanout done	Modules
73	63	10	56	34	19 *

- All current production hybrids and modules built at LBL
- UCSC getting ready with
  - hybrid-chip gluing and bonding
  - Chip replacement
  - Burn-in

* As of Feb 27 – 2 new modules have been built since then but not electrically tested yet

Wafers Used

z40800-w13		
20220040200010	Chips	00~11
20220040200011	chip	11
20220040200012	Chips	00~11
20220040200013	Chip	6
z40802-w09		
20220040200041	Chips	00~11
20220040200042	Chips	00~11
20220040200045	Chips	07~11
z40802-w14		
20220040200043	Chips	00~11
20220040200044	Chips	00~11
20220040200045	Chips	00~06
z40803-w01		
20220040200069	Chips	00~11
20220040200070	Chips	00~10
20220040200071	Chips	00~11
20220040200072	Chips	00~11
20220040200073	Chips	00~11
20220040200074	Chips	00~11
z40803-w02		
20220040200046	Chips	00~11
20220040200075	Chips	00~11
20220040200076	Chips	00~11
z40803-w03		
20220040200059	Chips	00~11
20220040200060	Chips	00~11
20220040200077	Chips	00~11
20220040200079	Chips	00~11
20220040200080	Chips	00~11
z40803-w04		
20220040200078	Chips	00~11
z40803-w05		
20220040200054	Chips	00~11
20220040200055	Chips	00~11
20220040200056	Chips	00~11
20220040200058	Chips	00~11

z40859-w01		
20220040200027	Chips	00~11
20220040200029	Chips	00~11
20220040200033	Chips	01~11
20220040200035	Chips	00~08, 10~11
20220040200040	Chips	00~07
z40859-w02		
20220040200013	Chips	00~05, 07~11
20220040200014	Chips	00~11
20220040200015	Chips	00~11
20220040200016	Chips	00~11
20220040200017	Chips	00~11
20220040200020	Chip	1
20220040200033	Chip	0
20220040200034	Chip	1
20220040200035	Chip	9
20220040200036	Chip	7
20220040200040	Chips	08~11
z40859-w03		
20220040200026	Chips	00~11
20220040200028	Chips	00~11
20220040200030	Chips	00~11
20220040200031	Chips	00~11
20220040200036	Chips	00~06, 08~11
z40862-w01		
20220040200061	Chips	00~11
20220040200062	Chips	00~11
20220040200063	Chips	00~11
20220040200067	Chips	00~10
z40862-w02		
20220040200064	Chips	00~11
20220040200065	Chips	00~11
20220040200066	Chips	00~11
20220040200067	Chip	11
20220040200068	Chips	00~05
20220040200070	Chip	11

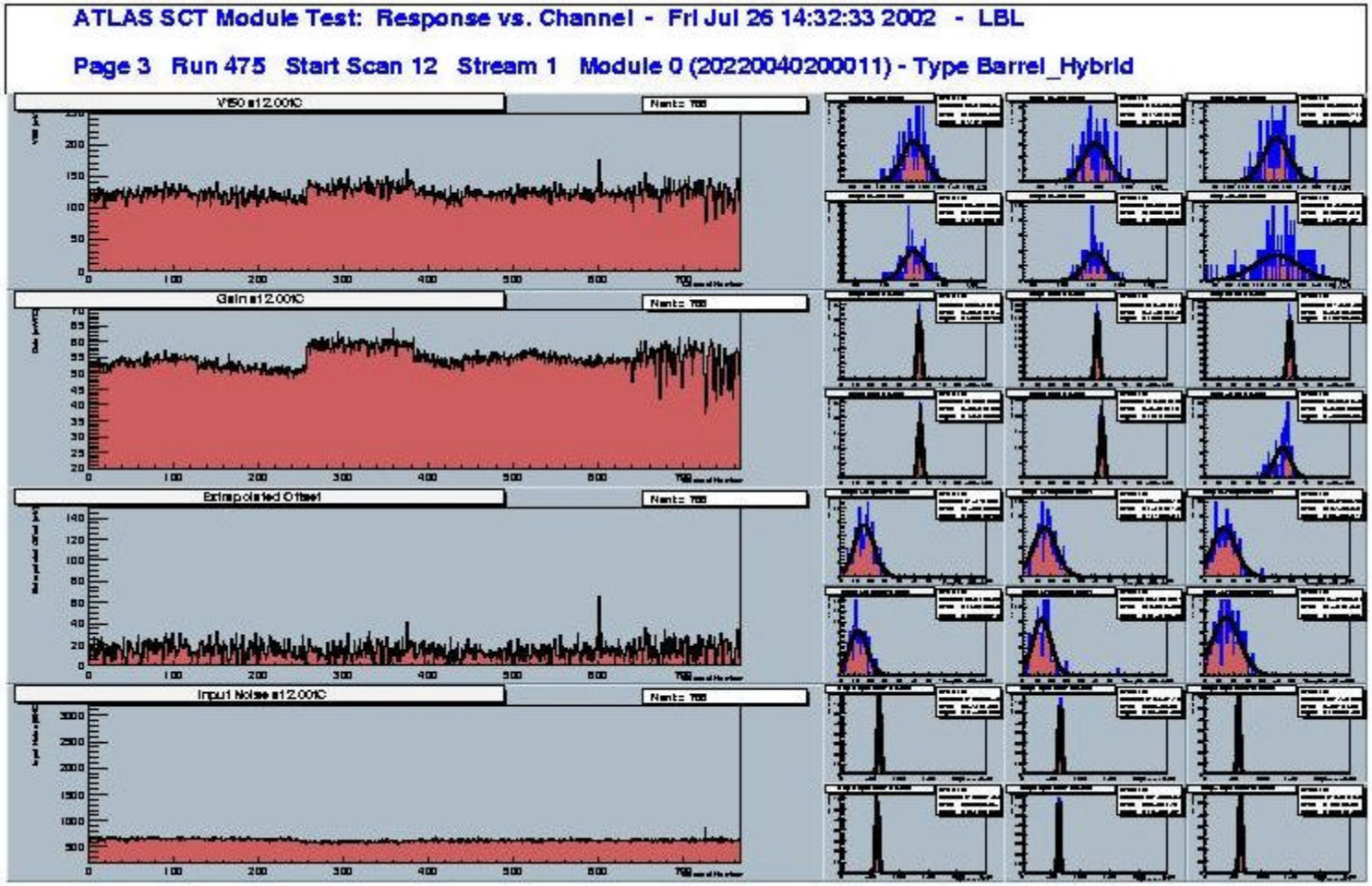
z40859-w04		
20220040200032	Chips	00~11
20220040200034	Chips	00, 02~11
20220040200037	Chips	00~11
20220040200038	Chips	00~11
20220040200039	Chips	00~07
z40859-w09		
20220040200018	Chips	00~11
20220040200019	Chips	00~11
20220040200021	Chips	00~11
20220040200022	Chips	00~11
20220040200039	Chips	08~11
z40859-w11		
20220040200008	Chips	00~11
20220040200009	Chips	00~11
20220040200011	Chips	00~10
z40859-w14		
20220040200020	Chips	00, 02~11
20220040200023	Chips	00~11
20220040200024	Chips	00~11
20220040200025	Chips	00~11
z40862-w09		
20220040200052	Chips	00~11
20220040200053	Chips	00~11
20220040200057	Chips	00~11
20220040200068	Chips	06~11
z40862-w11		
20220040200047	Chips	00~11
20220040200049	Chips	00~11
20220040200050	Chips	00~11
20220040200051	Chips	00~11

Defective Chips

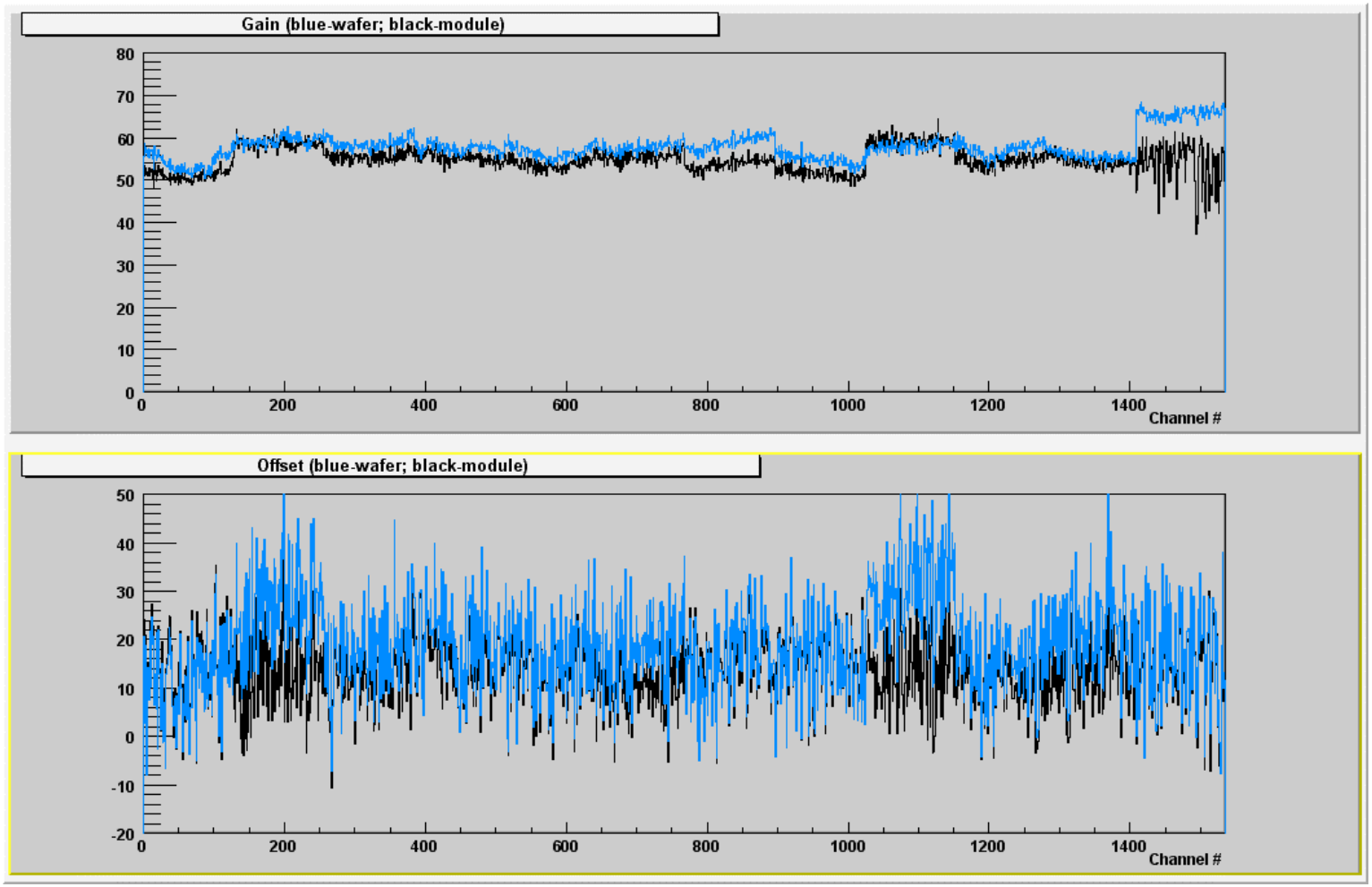
73 Hybrids built - 876 Chips - 12 (+2) defective ASIC's (1.6%)

Hybrid ID		ASIC ID	Defect
20220040200011	Chip 11	Z40859-W11-253	Large Gain Spread
20220040200013	Chip 6	Z40859-W02-51	chipped
20220040200020	Chip 1	Z40859-W014-5	TOKEN failure
20220040200021	Chip 8	Z40859-W09-136	Large Gain Spread
20220040200022	Chip 10	Z40859-W09-196	High Offset
20220040200035	Chip 6	Z40859-W01-171	Time Walk test failure
20220040200039	Chip 2	Z40859-W04-223	Large Gain Spread
20220040200039	Chip 10	Z40859-W09-204	chipped
20220040200046	Chip 9	Z40803-W02-132	Large Gain Spread
20220040200047	Chip 0	Z40862-W11-10	TrimDAC loading
20220040200054	Chip 4	Z40803-W05-18	Large Gain Spread
20220040200058	Chip 7	Z40803-W05-158	Trim DAC loading
20220040200068	Chip 1	Z40862-W02-232	Large Gain Spread
20220040200073	Chip 0	Z40803-W01-1	Strobe Delay failure

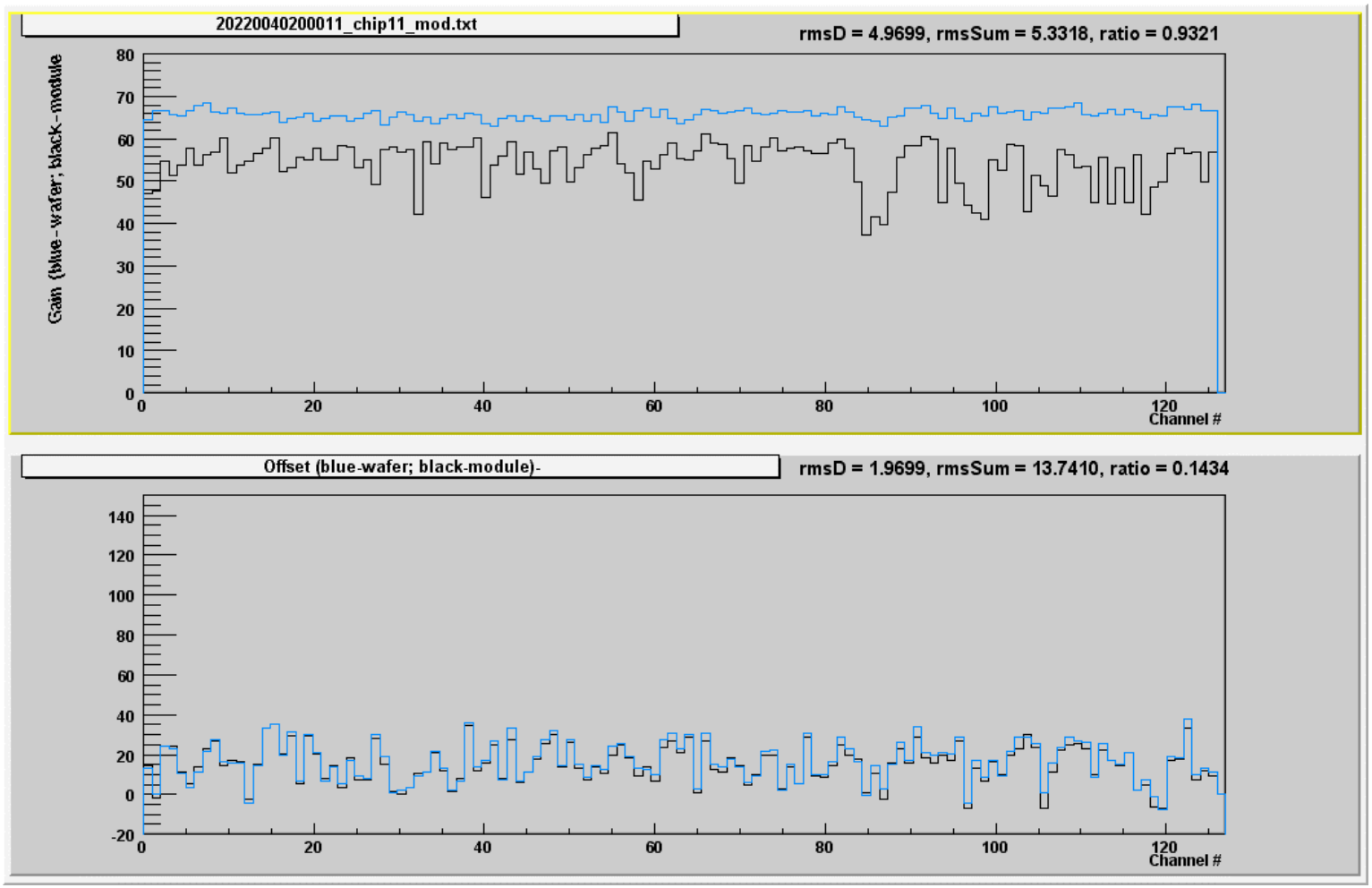
Hybrid 20220040200011
chip 11 Large Gain Spread



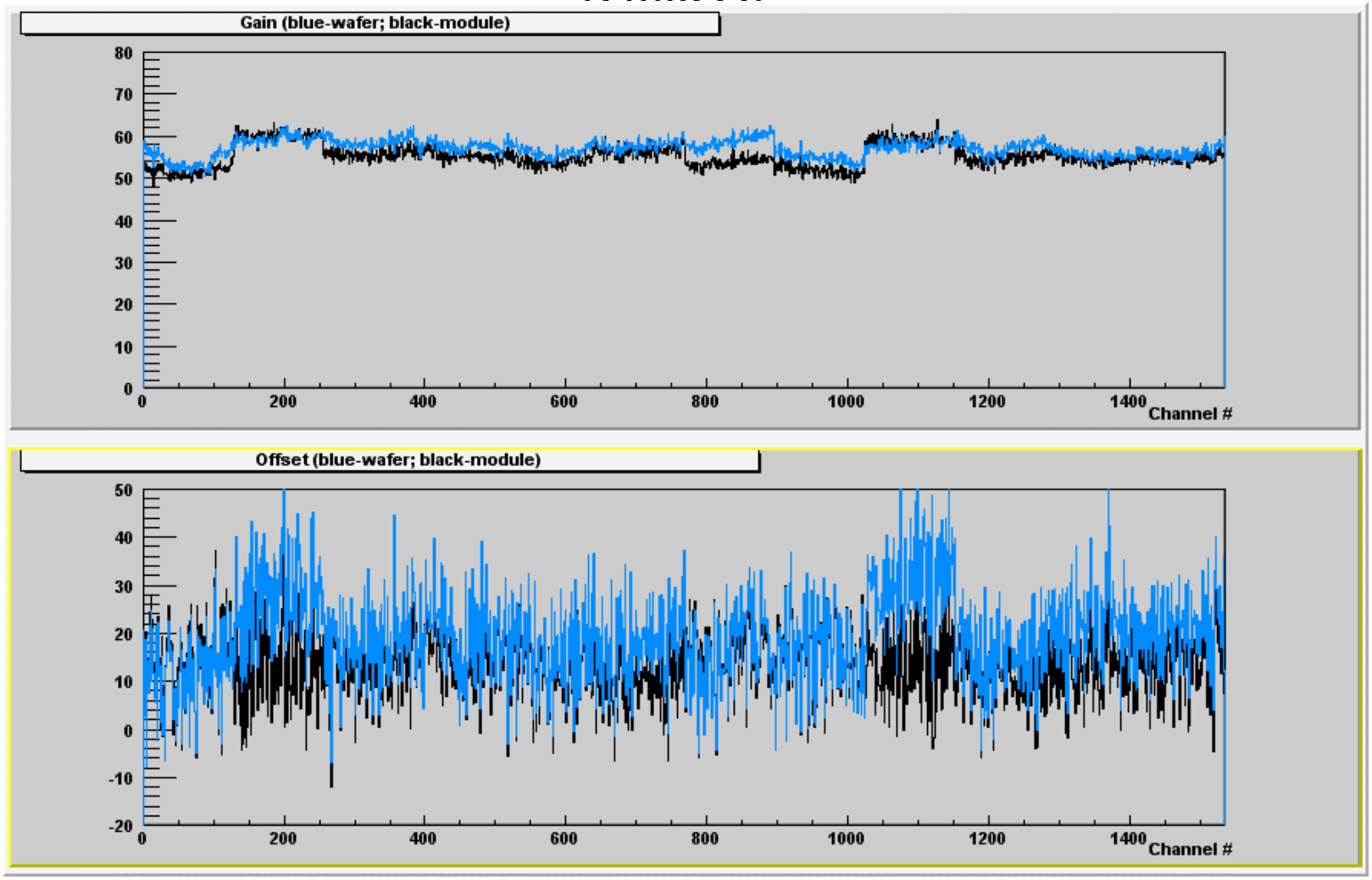
Hybrid 20220040200011
Wafer/Hybrid Comparison



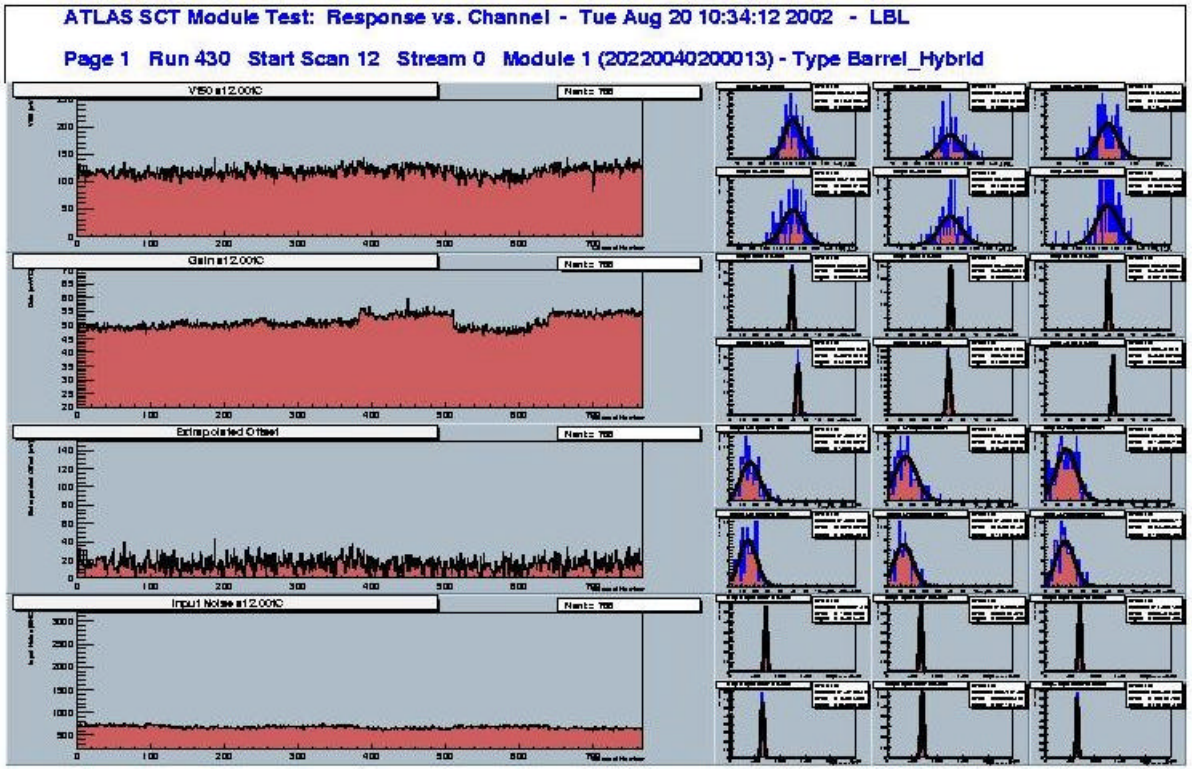
Hybrid 20220040200011
Chip 11 Wafer/Hybrid Comparison



Hybrid 20220040200011
Wafer/Hybrid Comparison after chip 11 replaced



Hybrid 20220040200013
Chip 2-5 Digital Tests Failure starting at 33°C



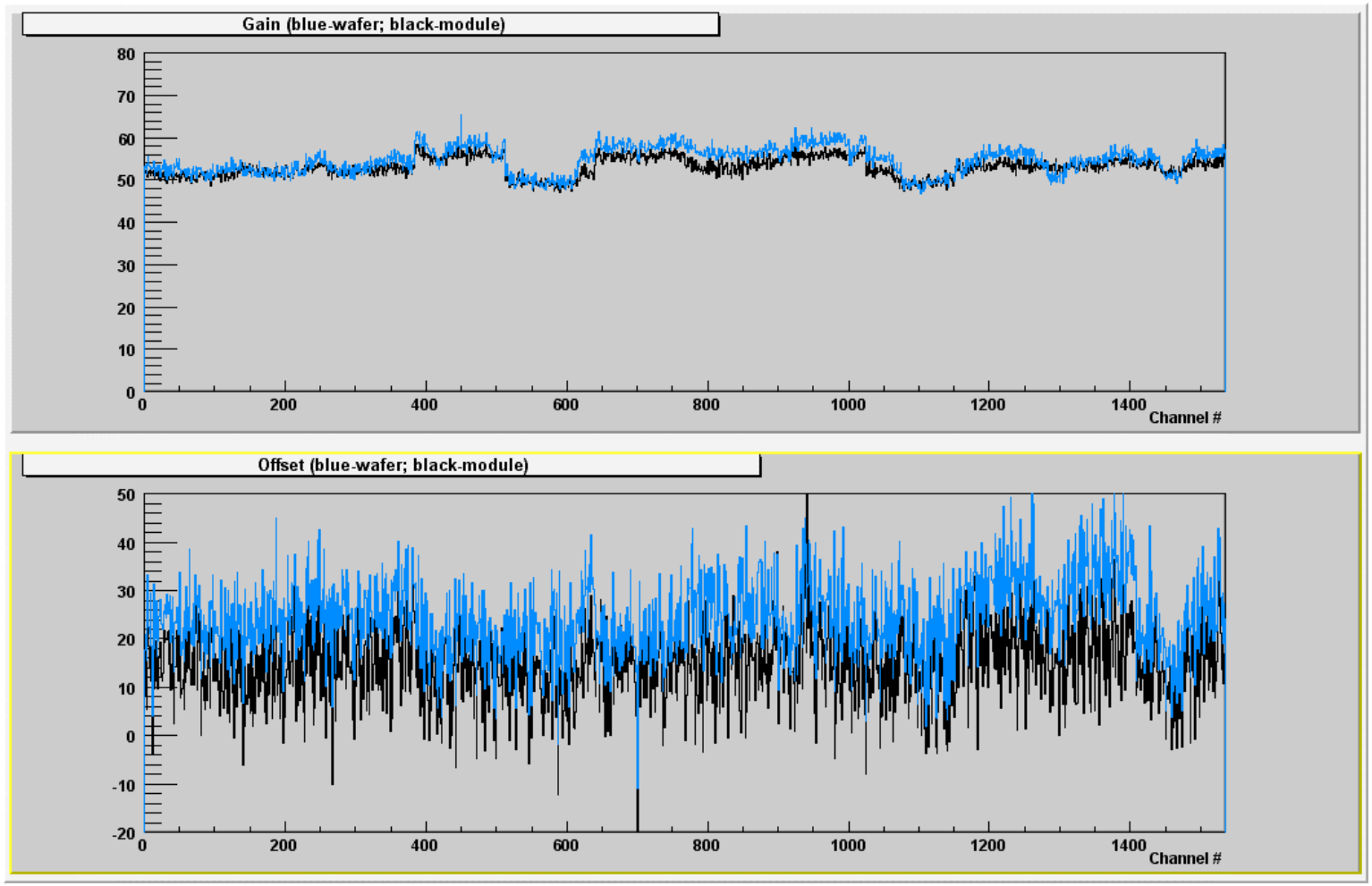
Three Point Gain Response at 37°C

Hybrid tests:
FullBypassTest: fails at Vdd = 3.5V but works fine at higher Vdd

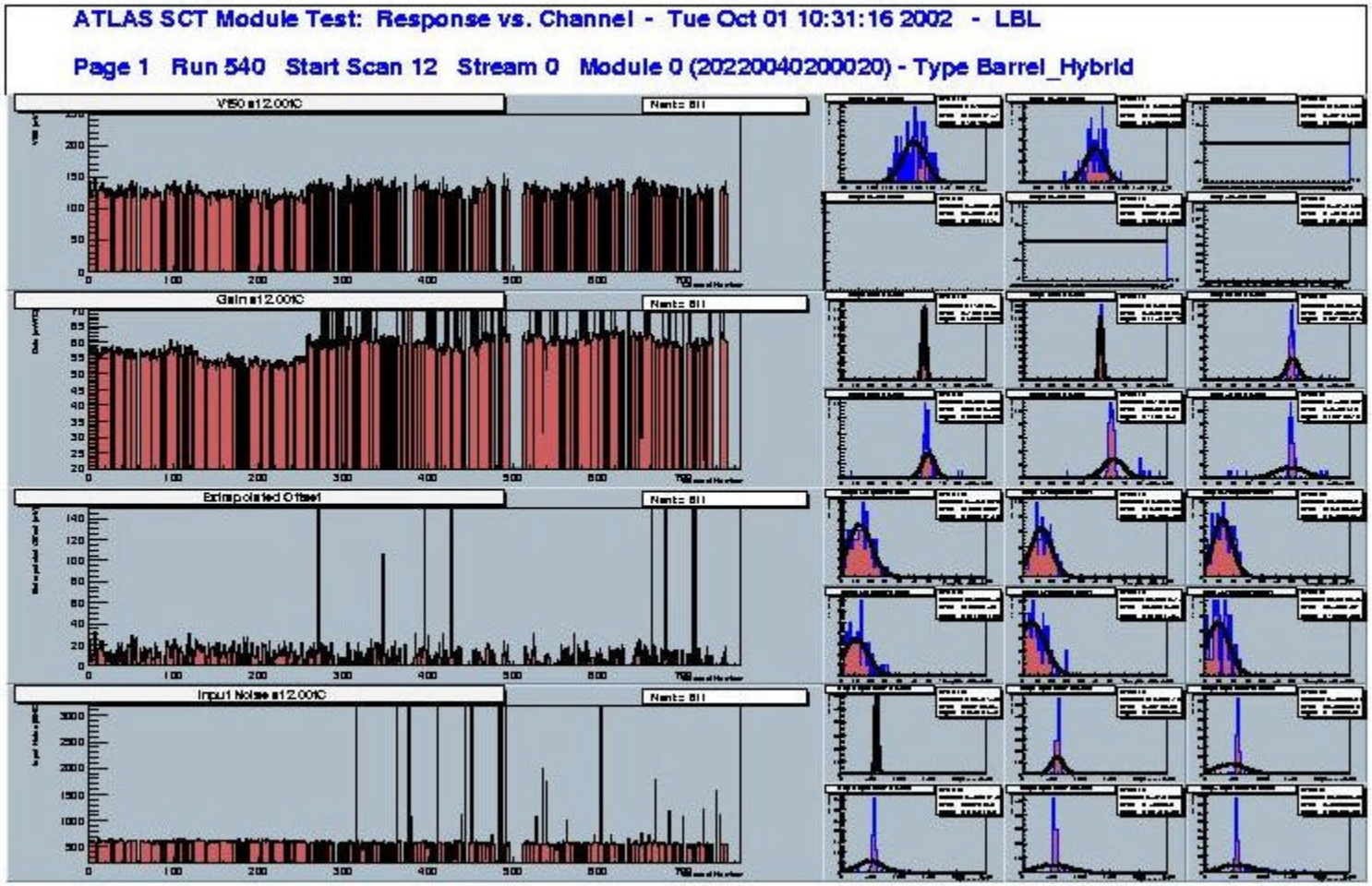
Wafer TV tests:
At 40 and 50 MHz all chips TV(eff) = 1 and all Vdd(eff) =1
except chip S02: at 50 MHz and Vdd=3.3V for TV2 to TV5 eff =0

The timing of the token passing is quite critical. At higher temperatures the CMOS is slower, so it could get closer to the edge.
It might be related to the quality of the clock signal.
It might work at a different system.

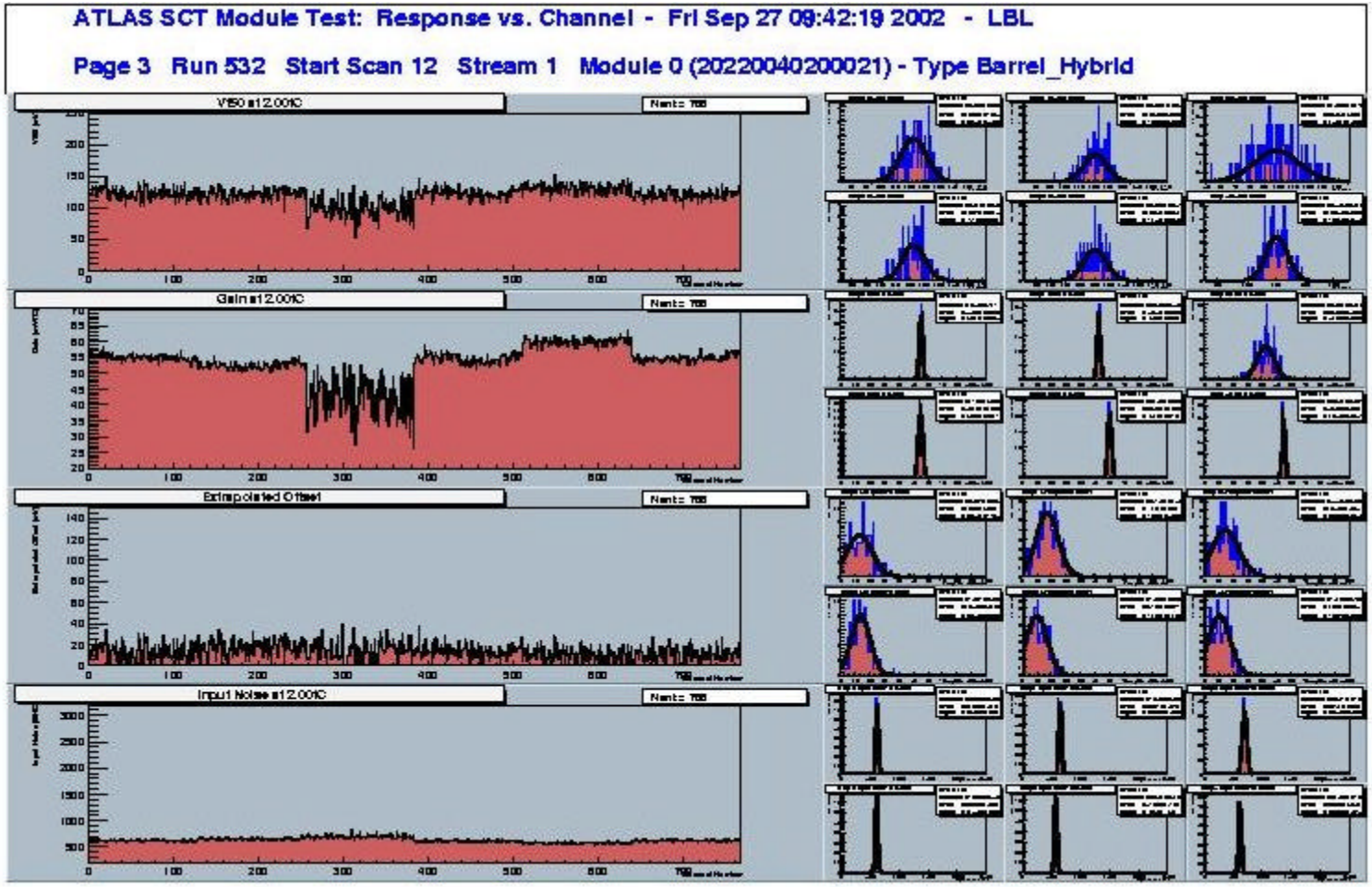
Hybrid 20220040200013
Wafer/Hybrid Comparison



Hybrid 20220040200020
chip 1 TOKEN Failure

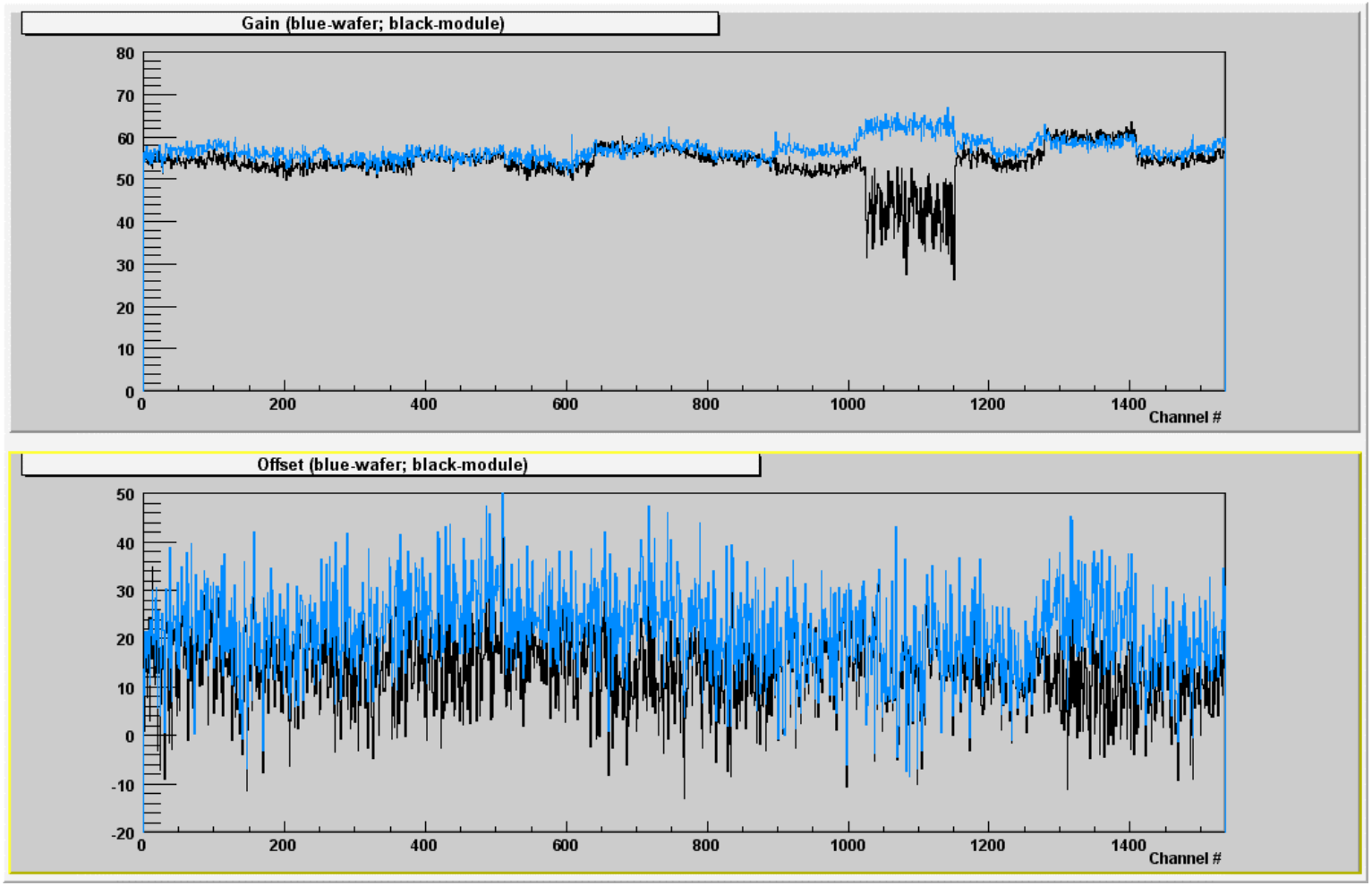


Hybrid 20220040200021
chip 8 Large Gain Spread

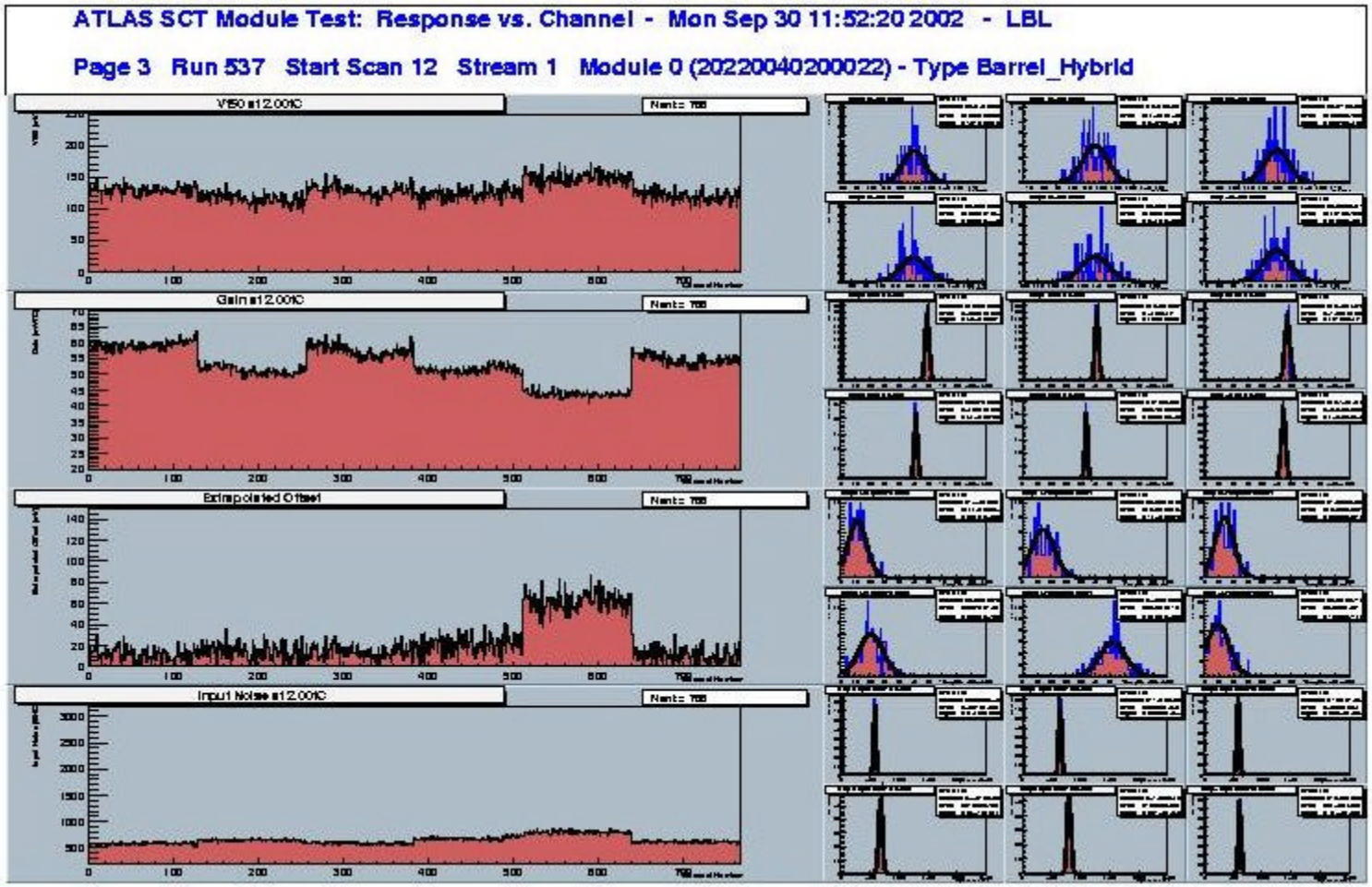


Chip started to work well at Vcc=3.7V - Voltage drop at the hybrid 50 mV
Under wafer test (test performed at UCSC) works at nominal Vcc

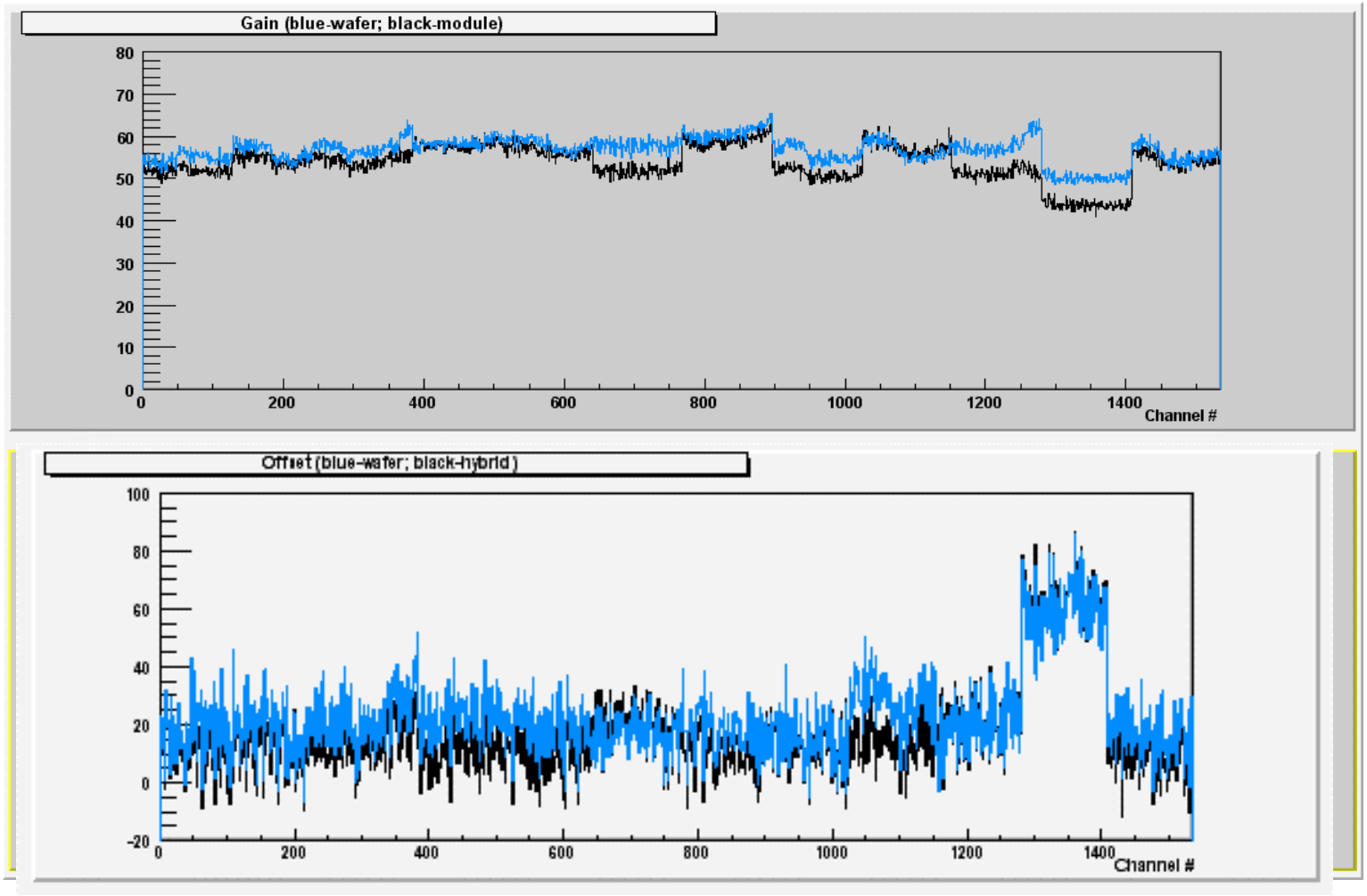
Hybrid 20220040200021
Wafer/Hybrid Comparison



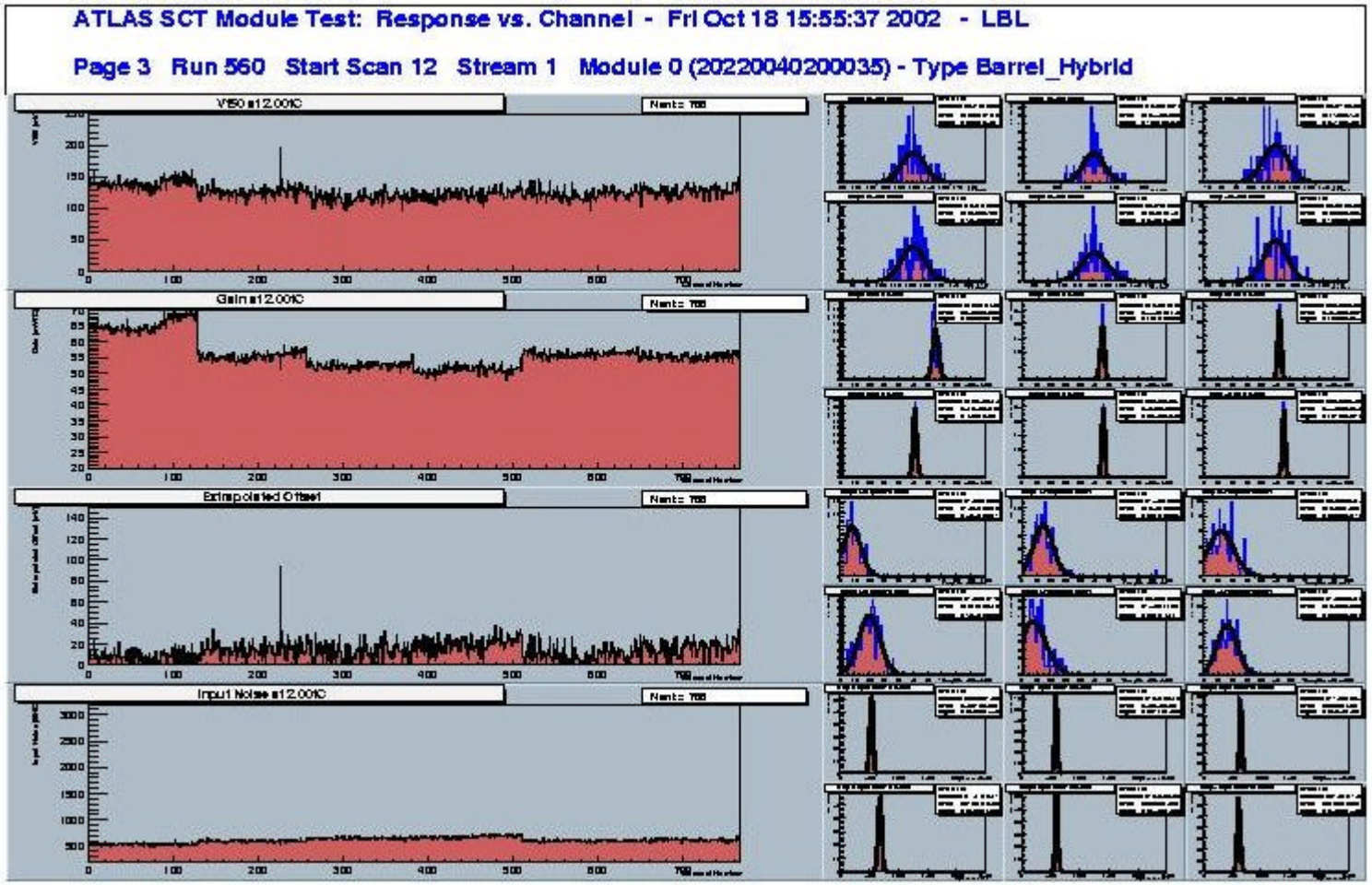
Hybrid 20220040200022
Chip 10 High Offset



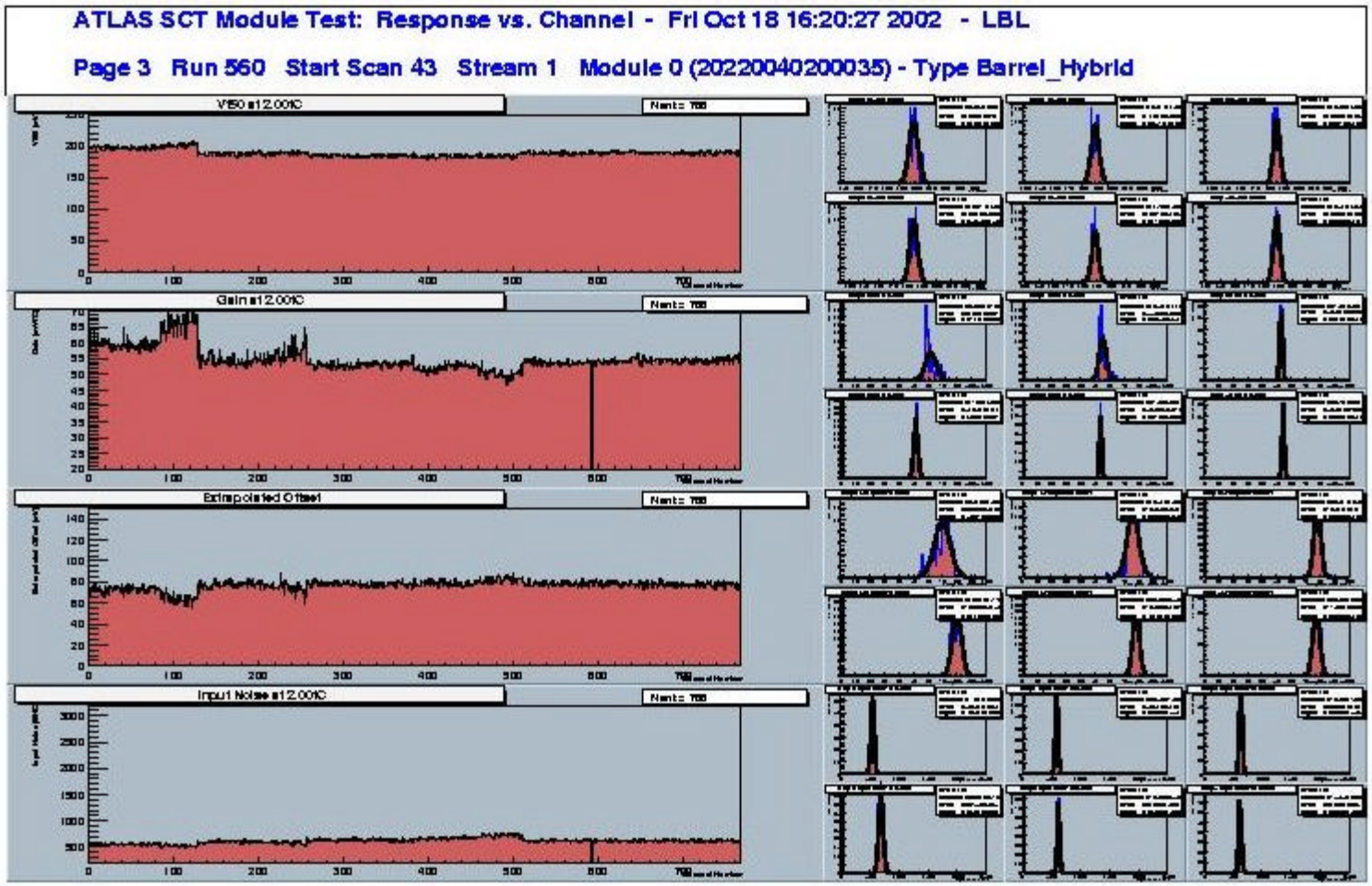
Hybrid 20220040200022
Wafer/Hybrid Comparison



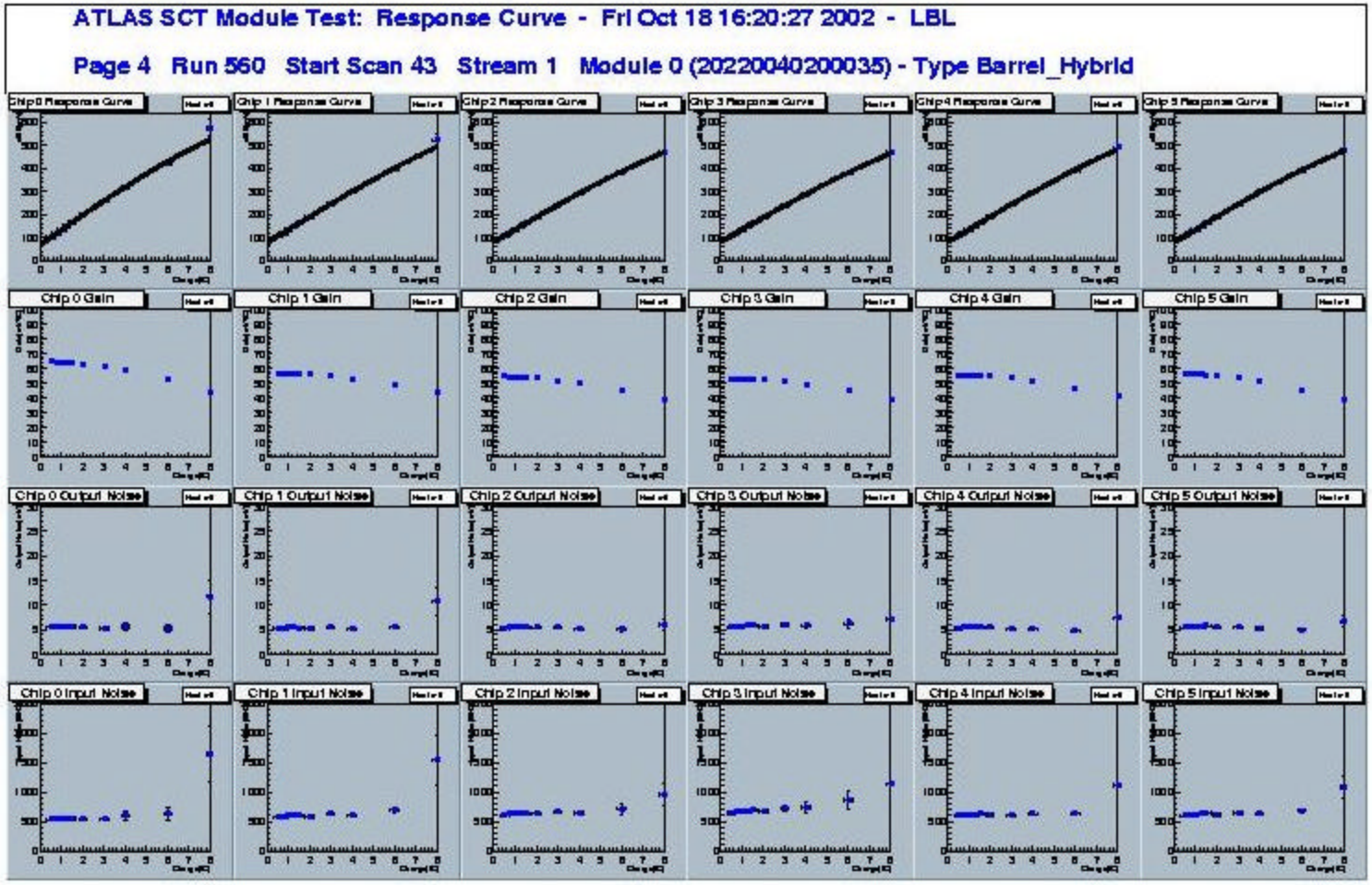
Hybrid 20220040200035
Chip 6 (M8) High Gain (3Pt)



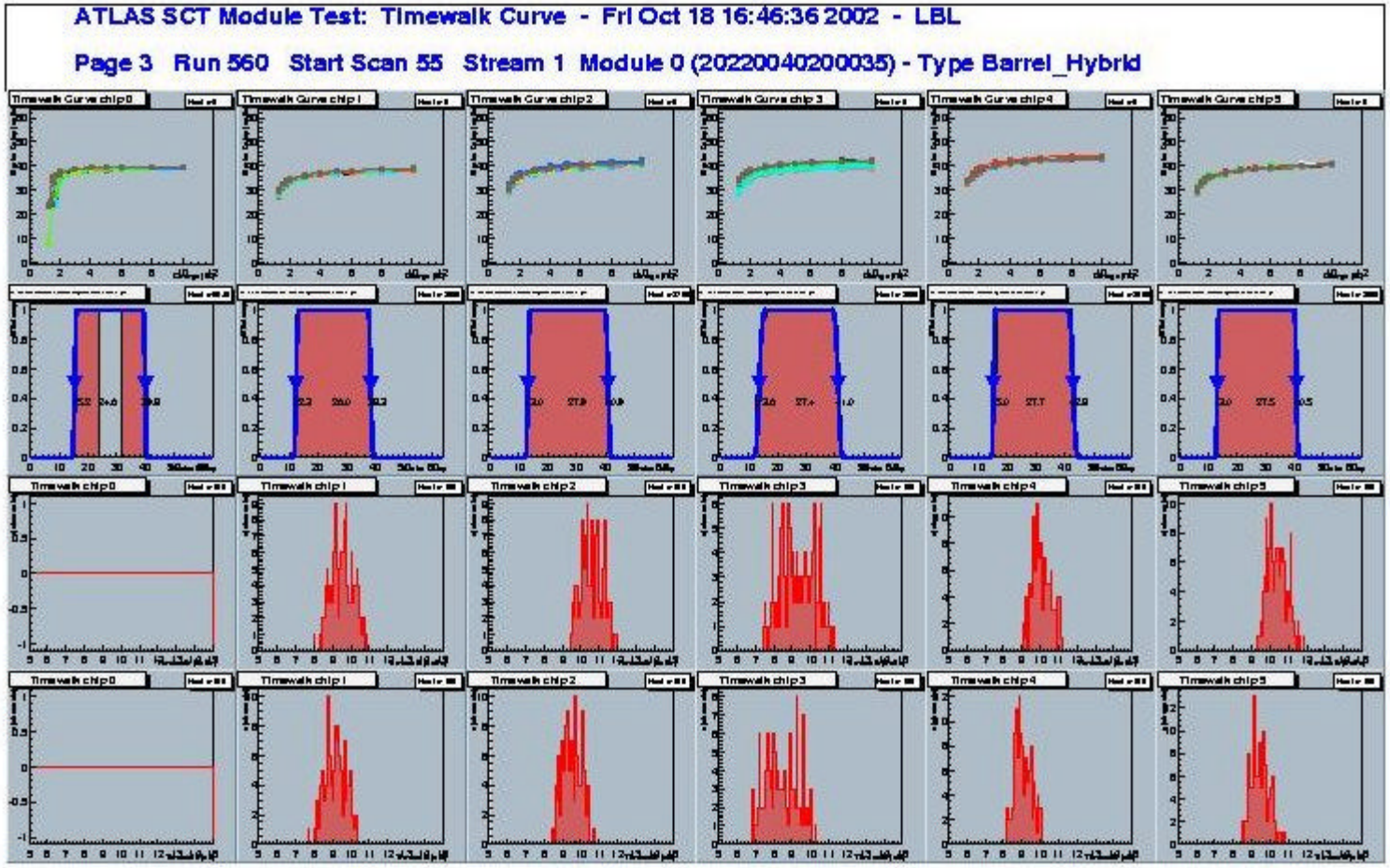
Hybrid 20220040200035
Chip 6 (M8) High Gain (After trim)



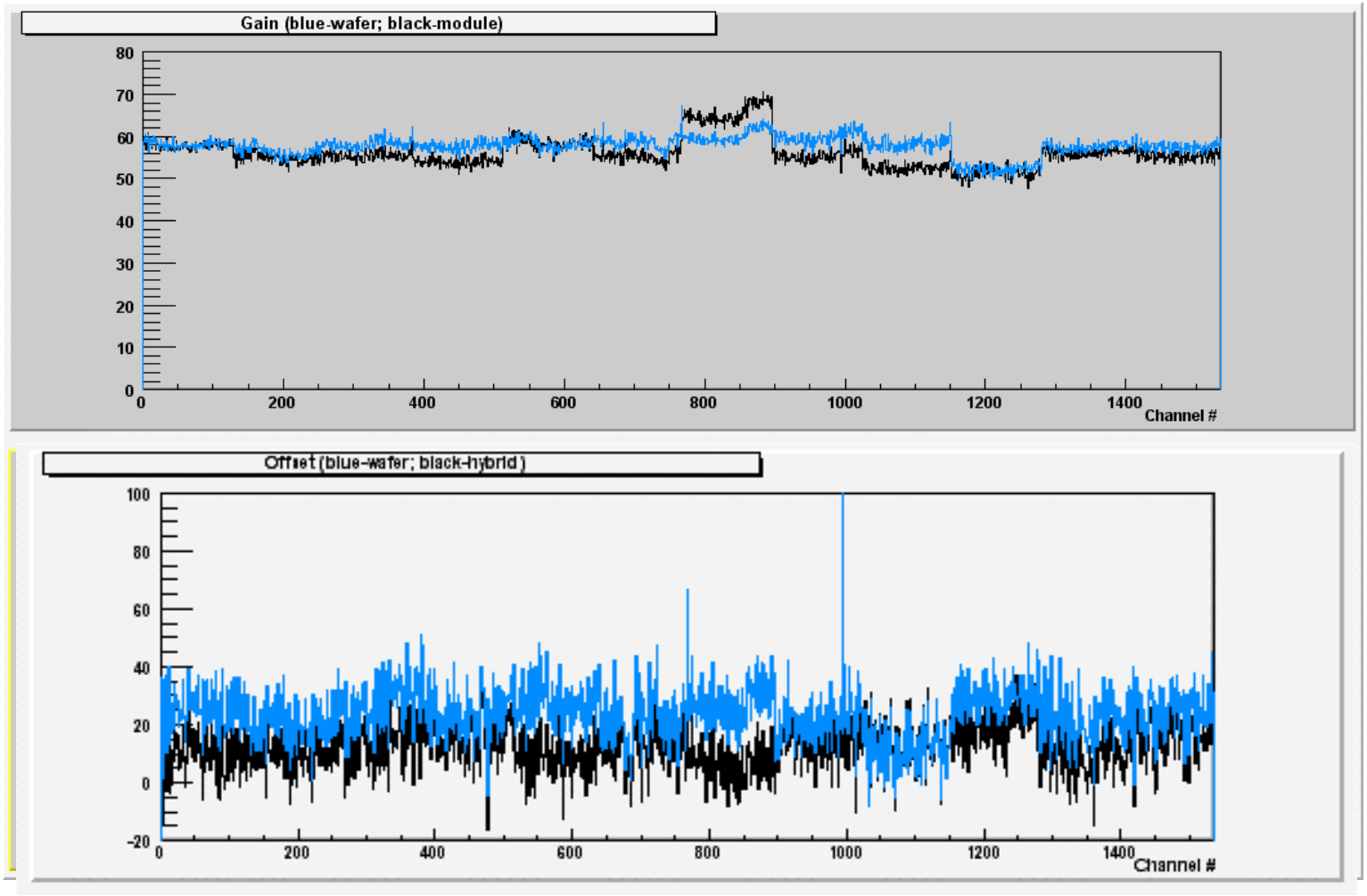
Hybrid 20220040200035
Chip 6 (M8) High Gain (after trim)



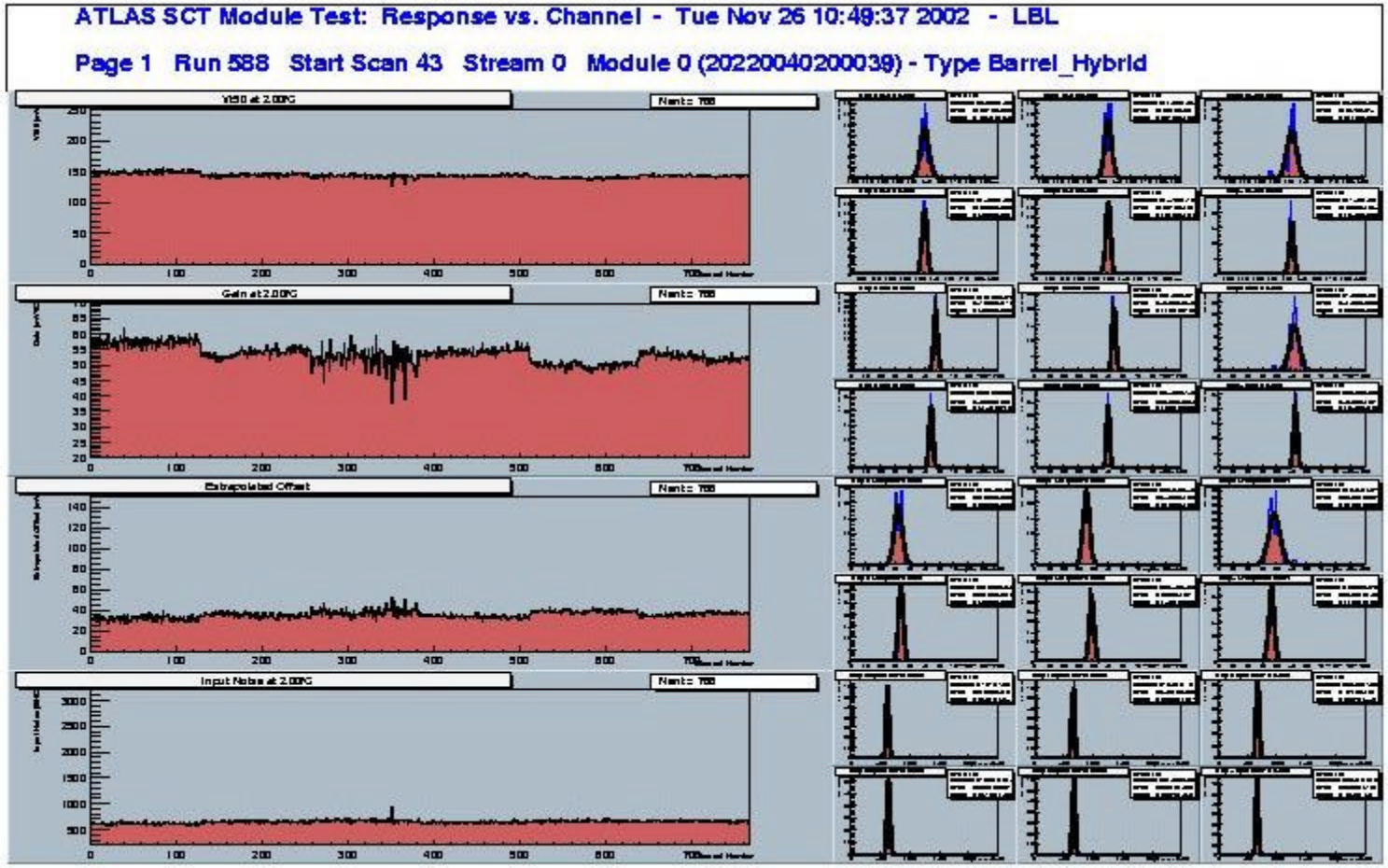
Hybrid 20220040200035
Chip 6 (M8) Time Walk Failure



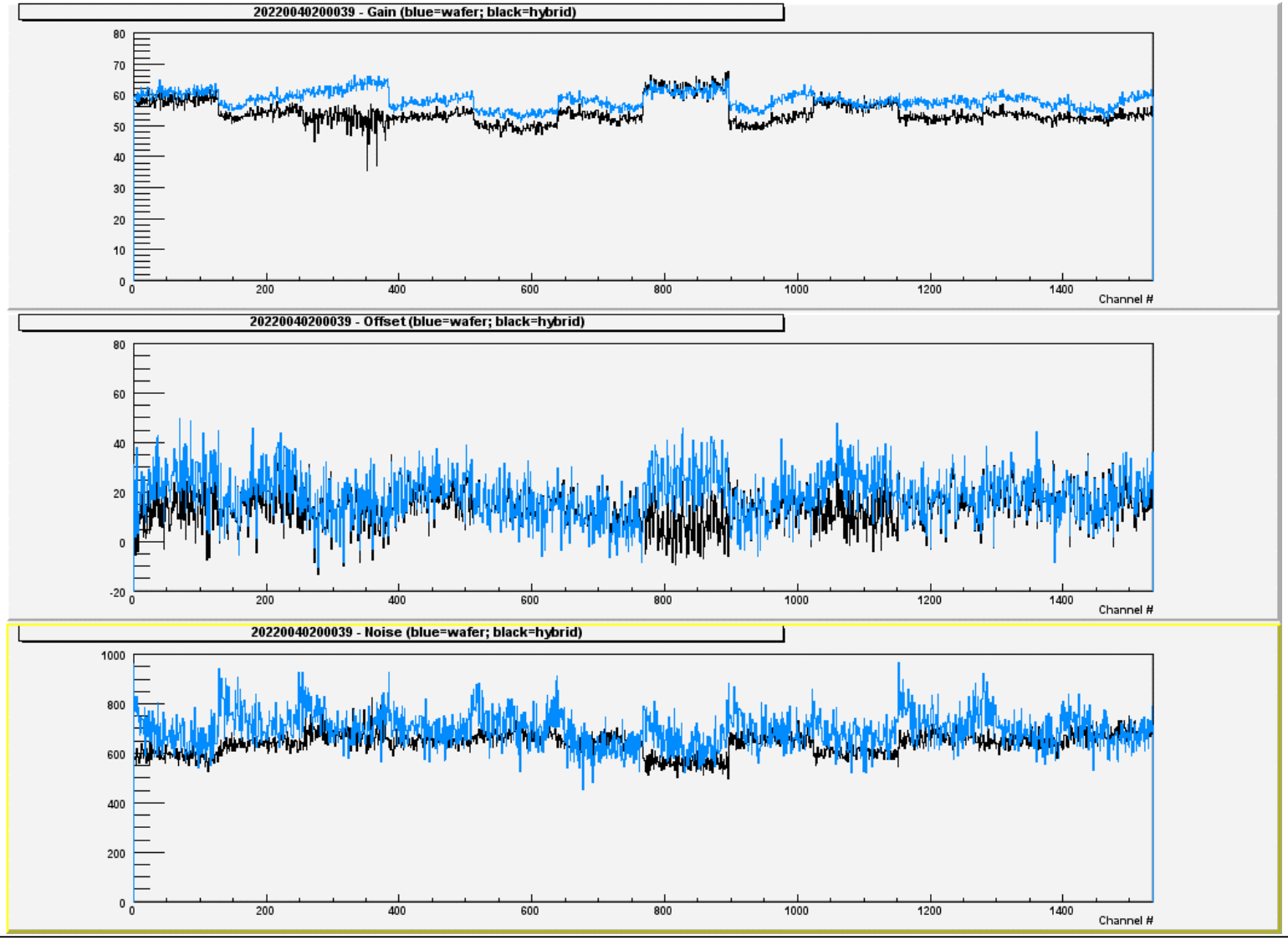
Hybrid 20220040200035
Wafer/Hybrid Comparison



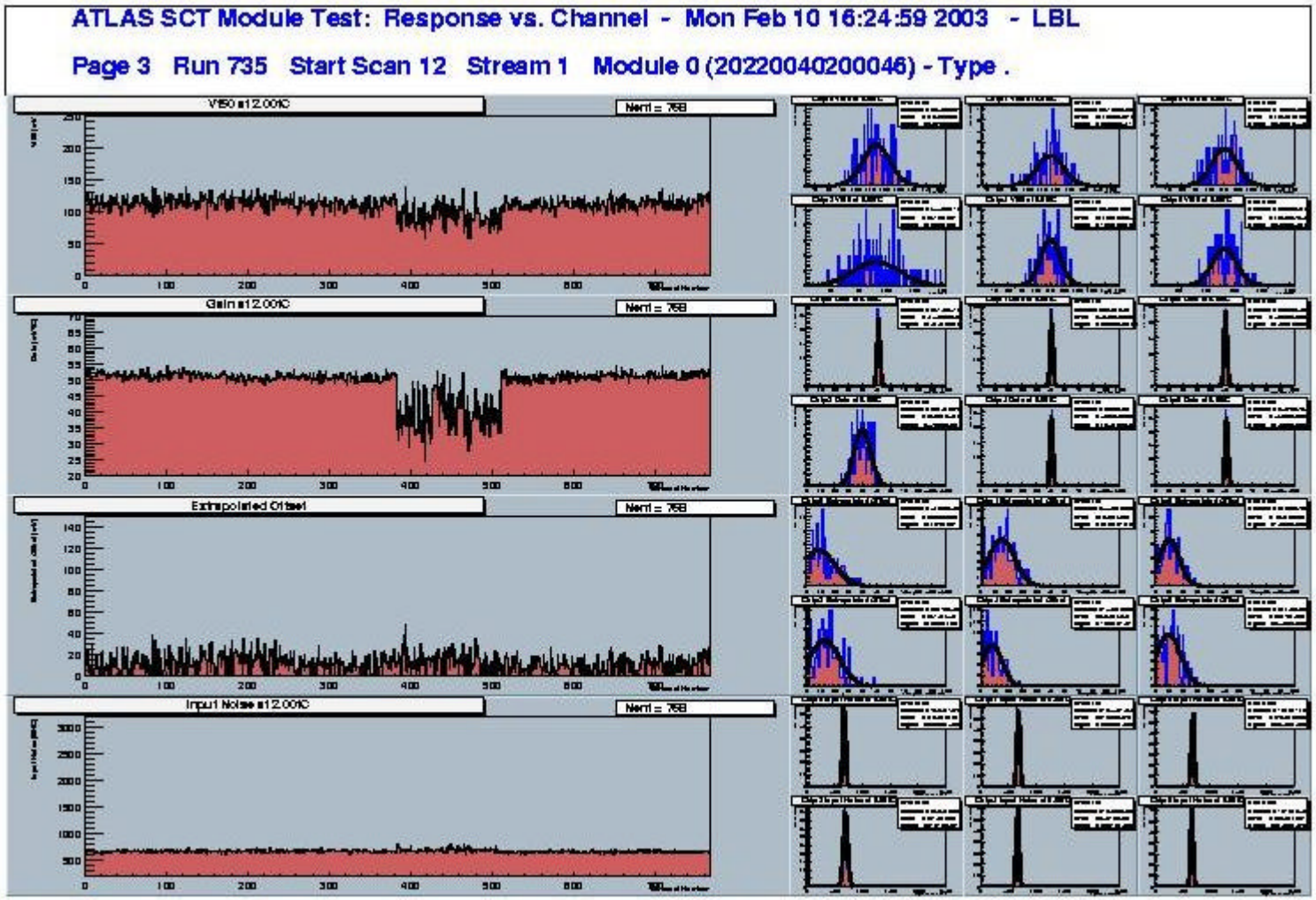
Hybrid 20220040200039
Chip 1 Large Gain Spread



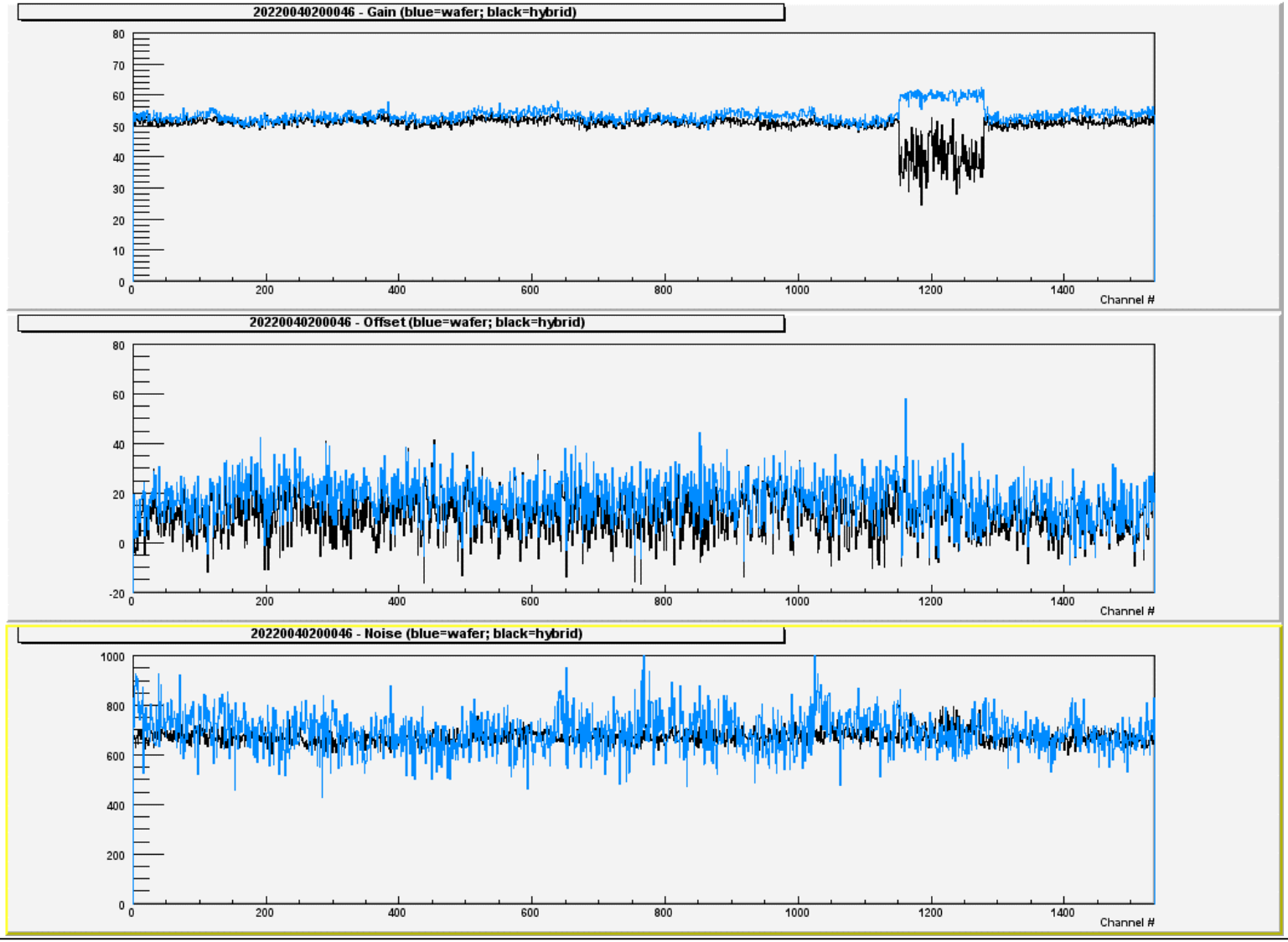
Hybrid 20220040200039
Wafer/Hybrid Comparison



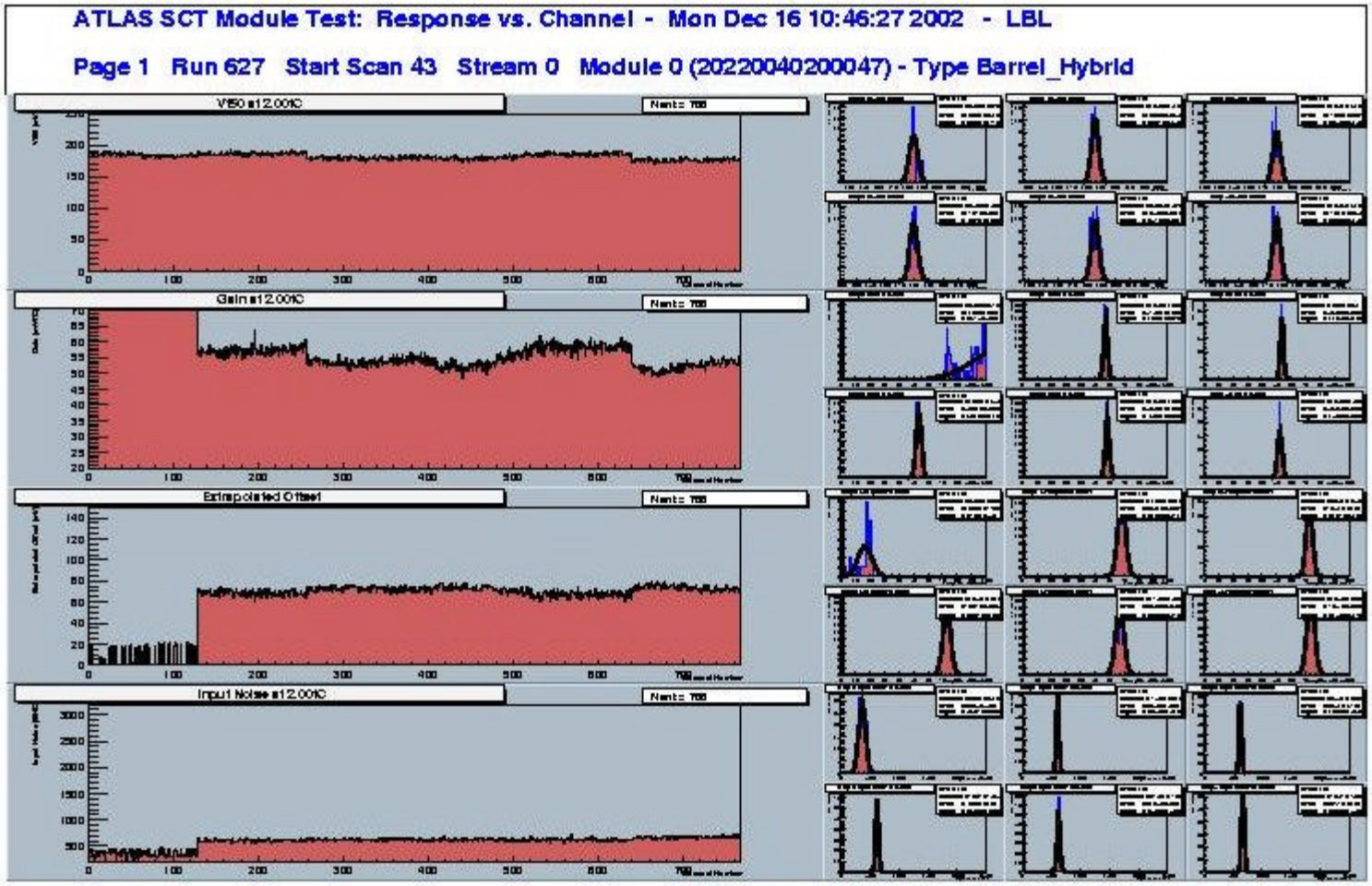
Hybrid 20220040200046
Chip 9 Large Gain Spread



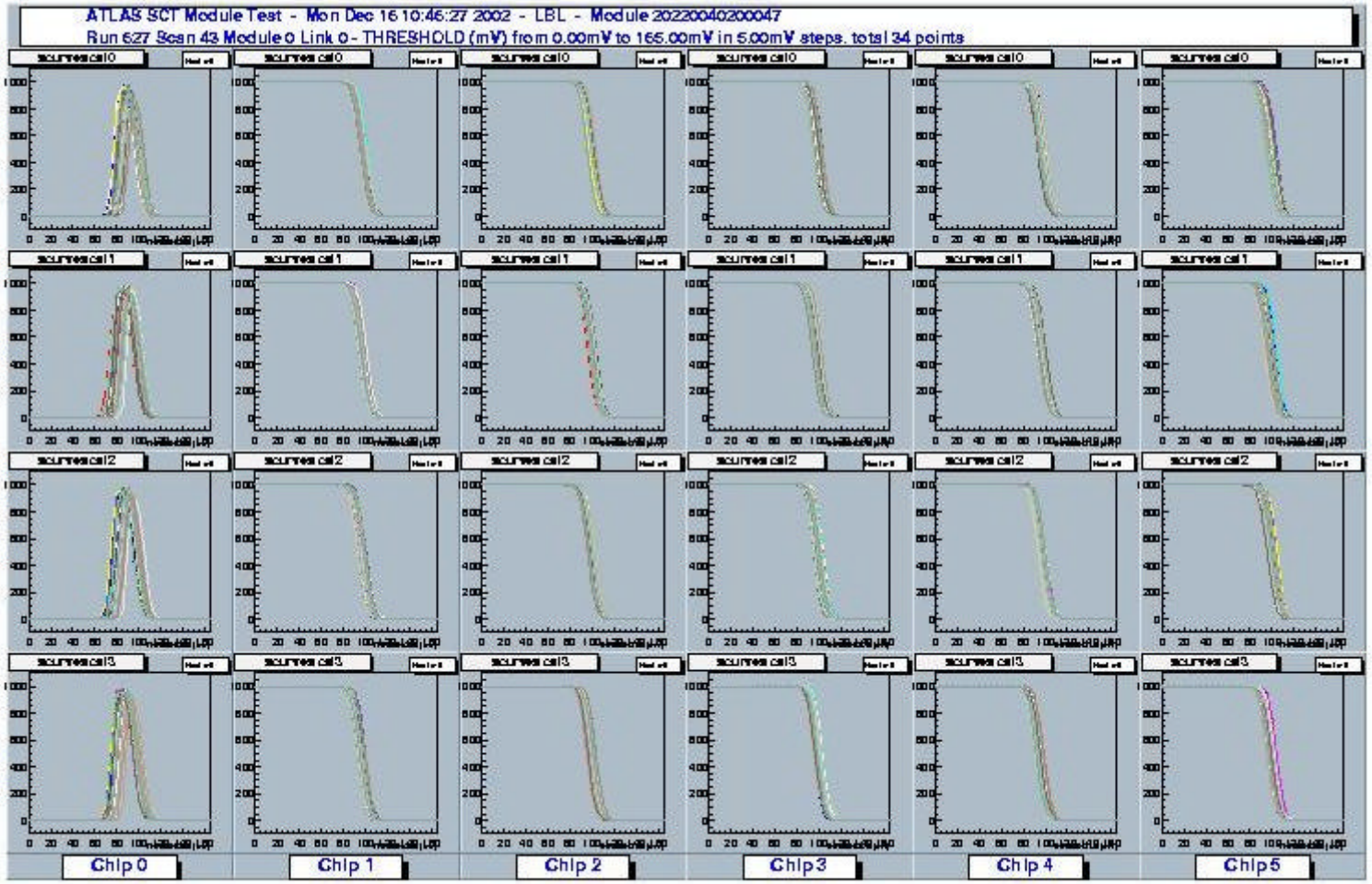
Hybrid 20220040200046
Wafer/Hybrid Comparison



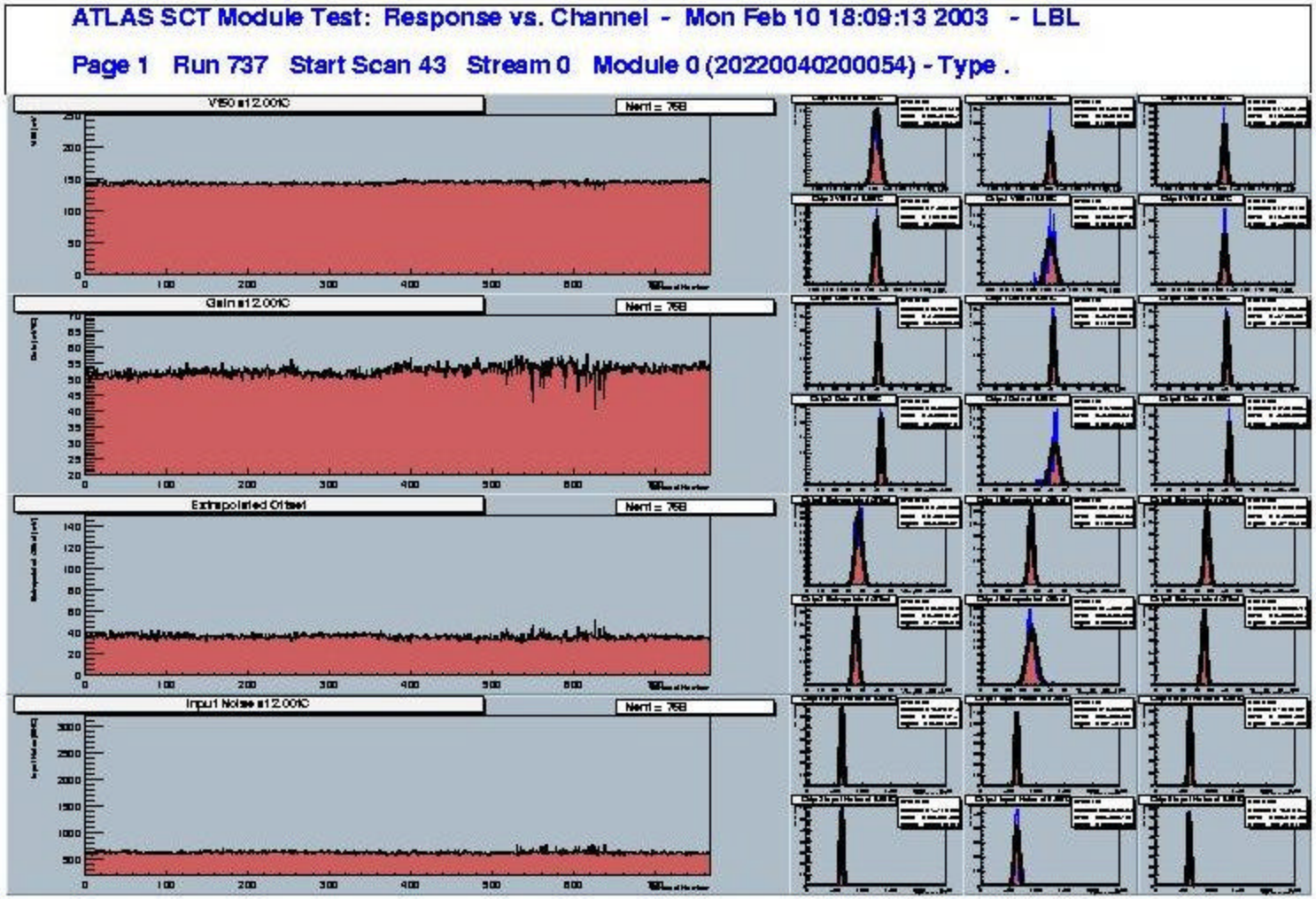
Hybrid 20220040200047
Chip 6 Trim DAC Loading



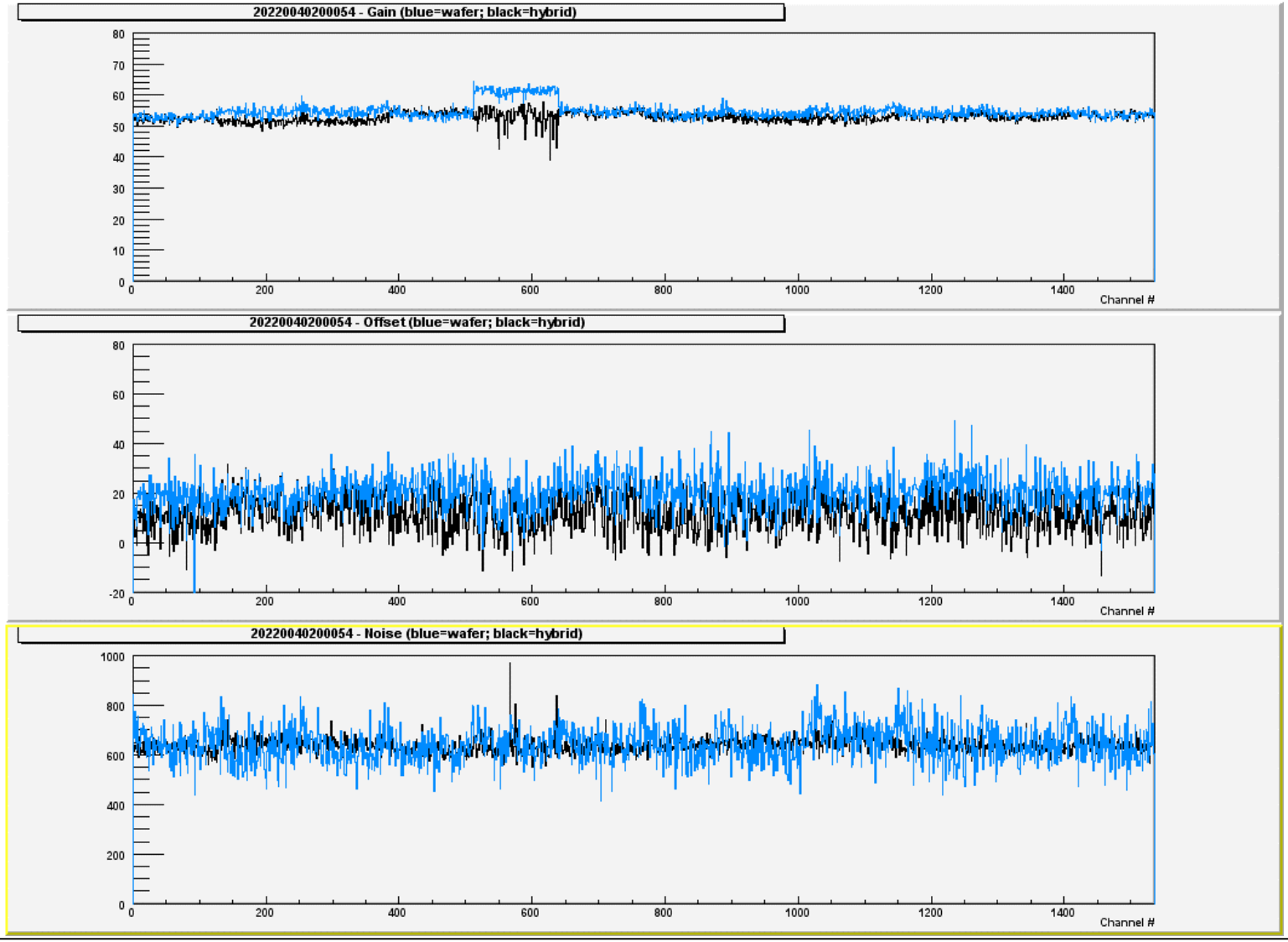
Hybrid 20220040200047
Chip 6 Trim DAC Loading



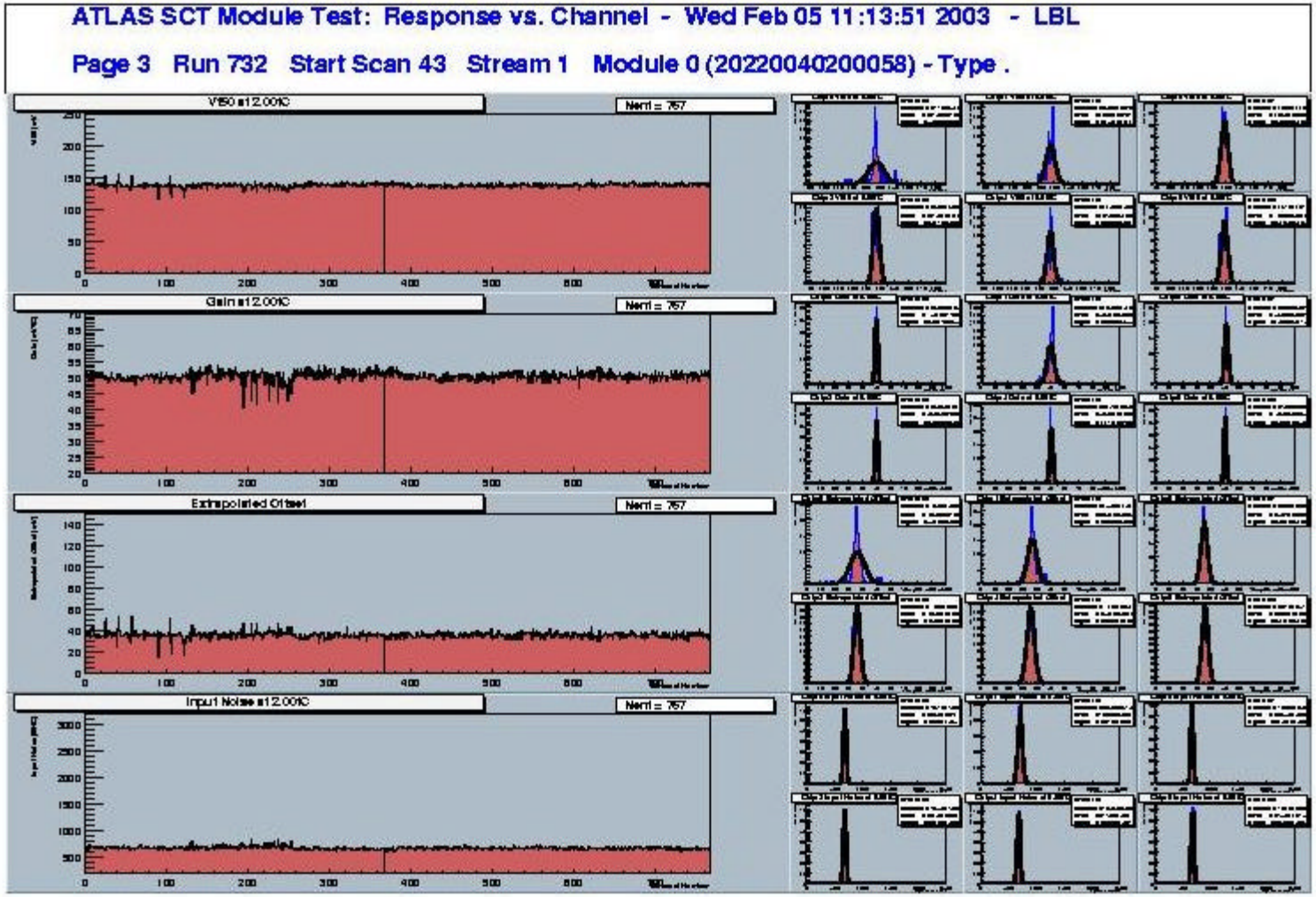
Hybrid 20220040200054
Chip 6 Large Gain Spread



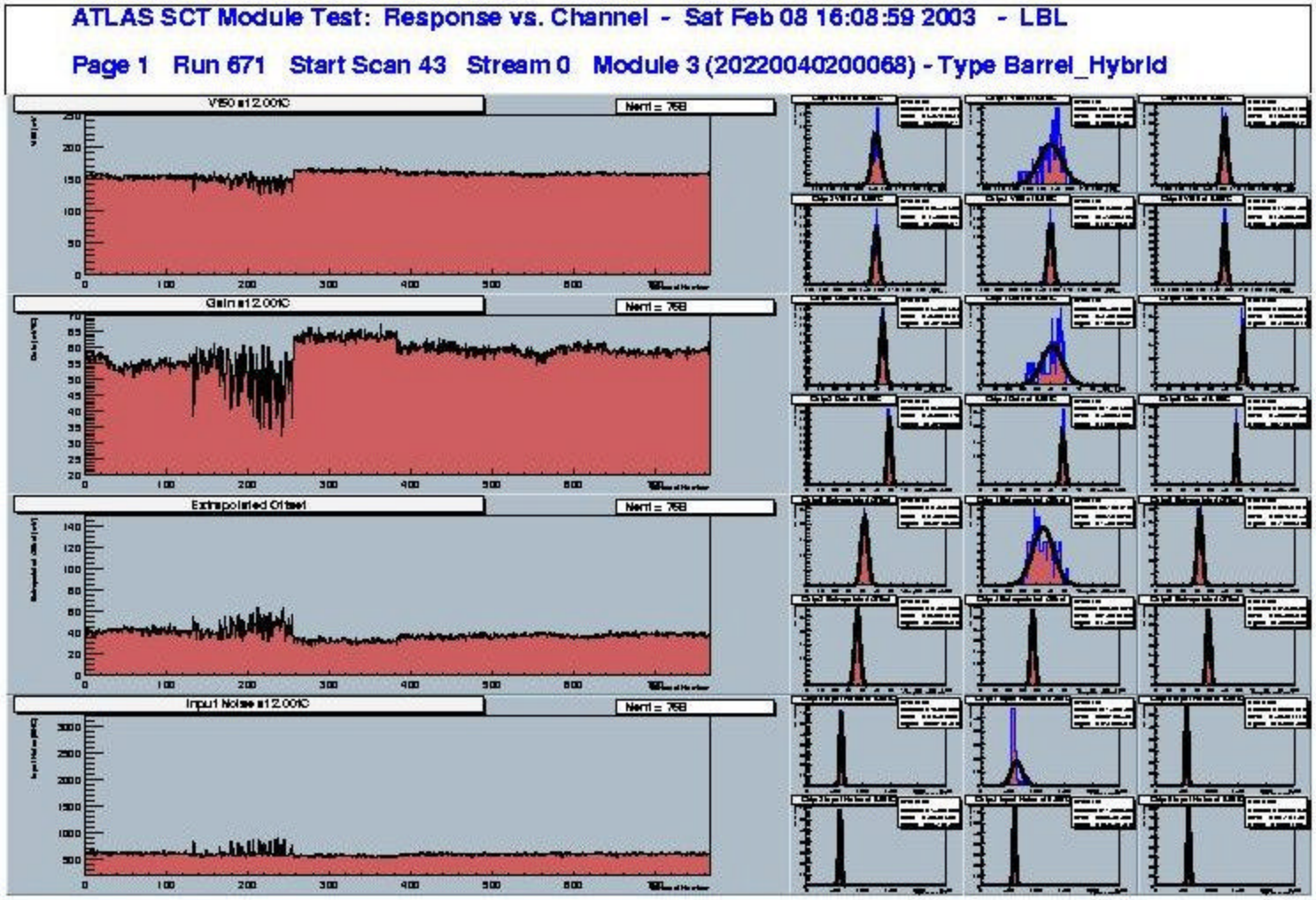
Hybrid 20220040200054
Wafer/Hybrid Comparison



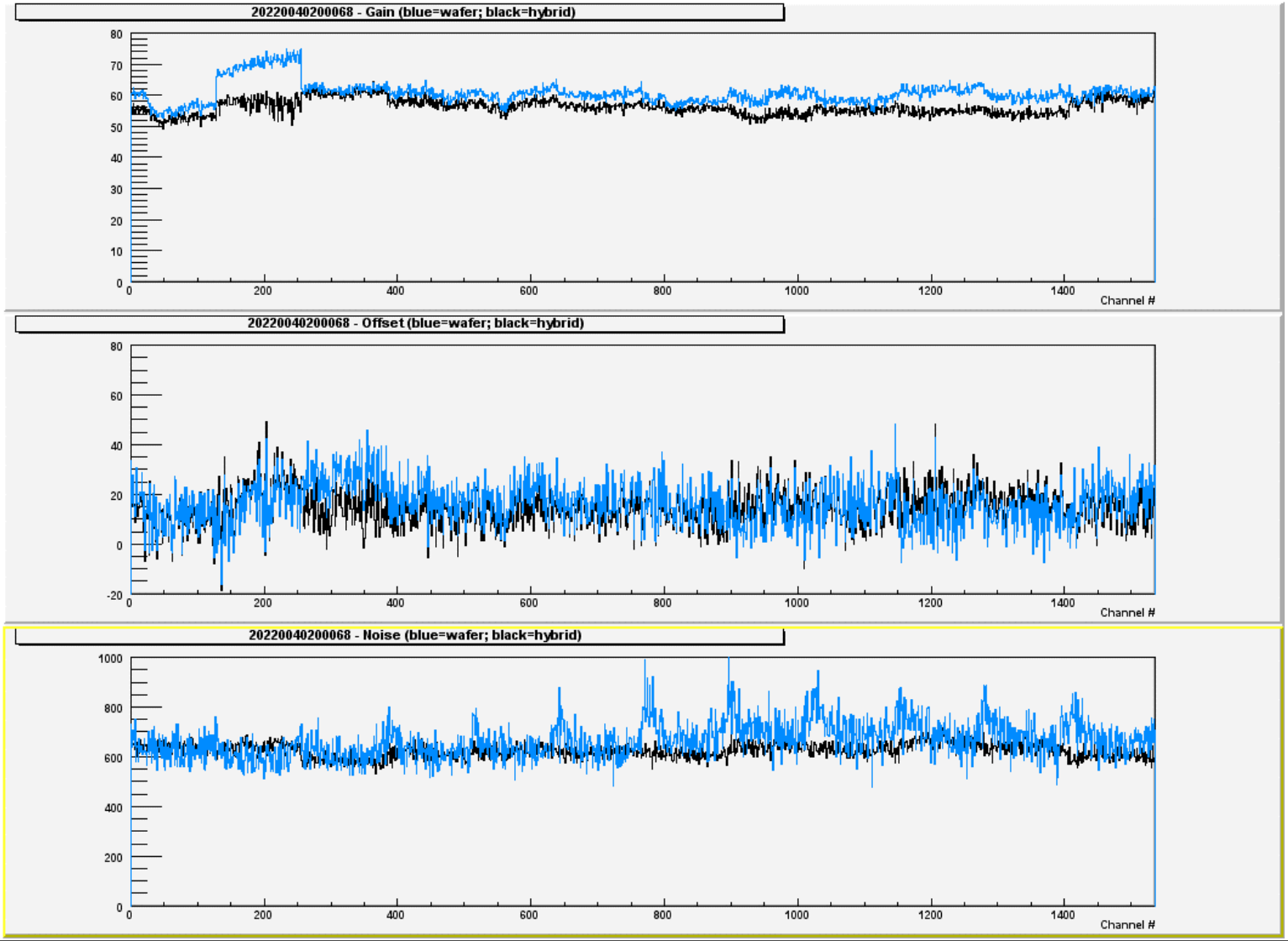
Hybrid 20220040200058
Trim DAC Loading



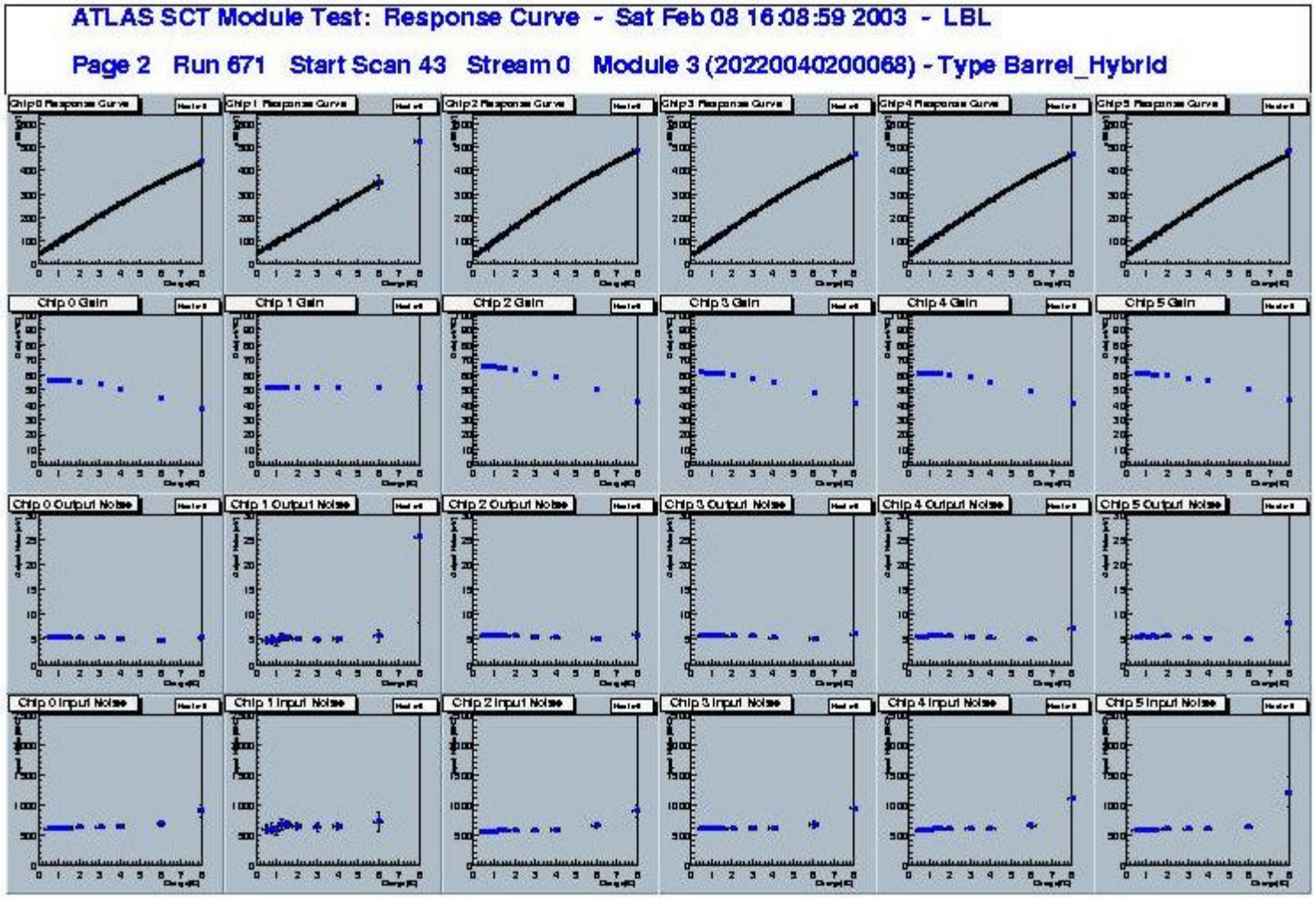
Hybrid 20220040200068
Chip 6 Large Gain Spread - cold



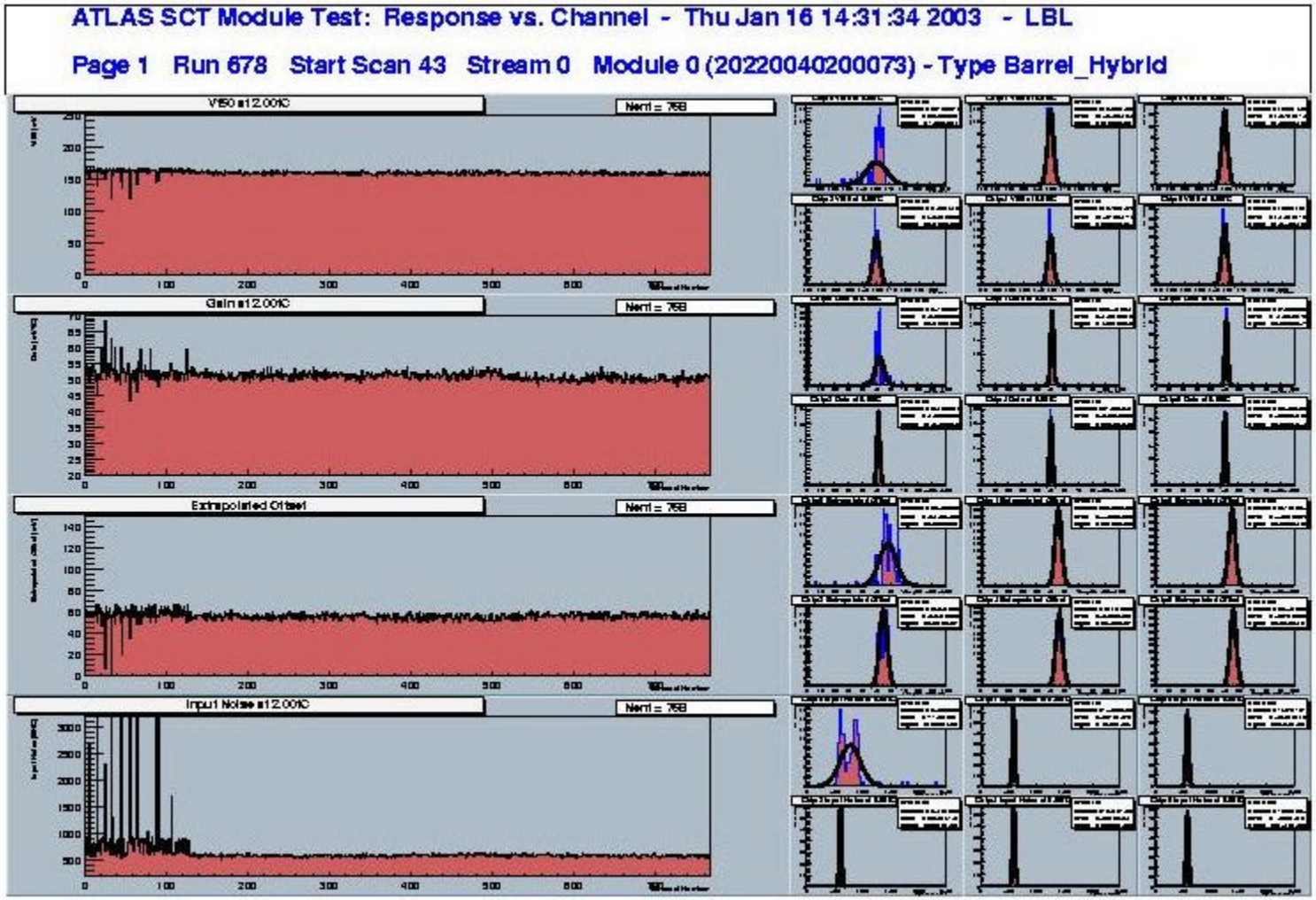
Hybrid 20220040200068
Wafer/Hybrid Comparison



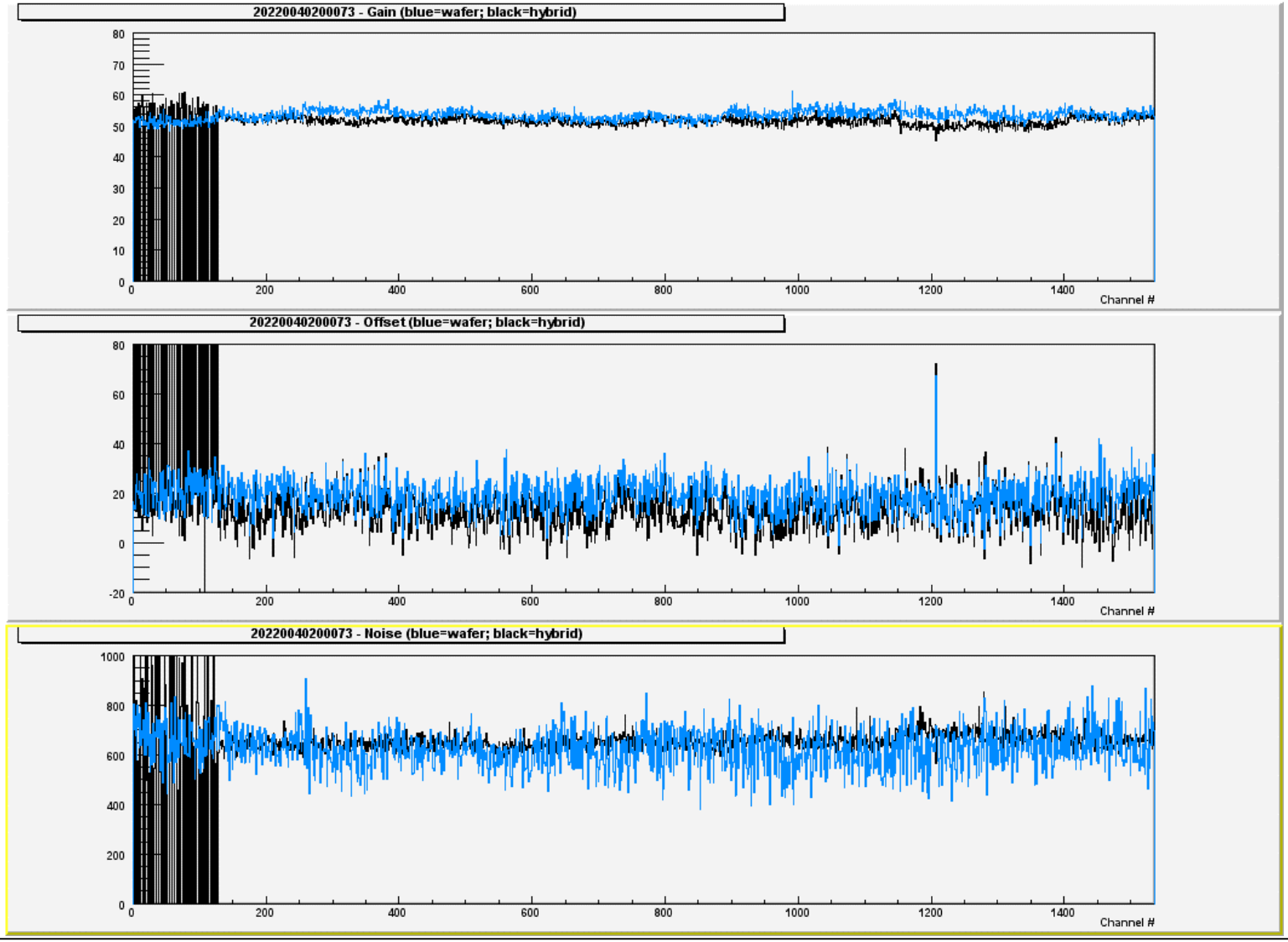
Hybrid 20220040200068
Chip 6 Large Gain Spread - cold



Hybrid 20220040200073
Chip 0 Strobe delay

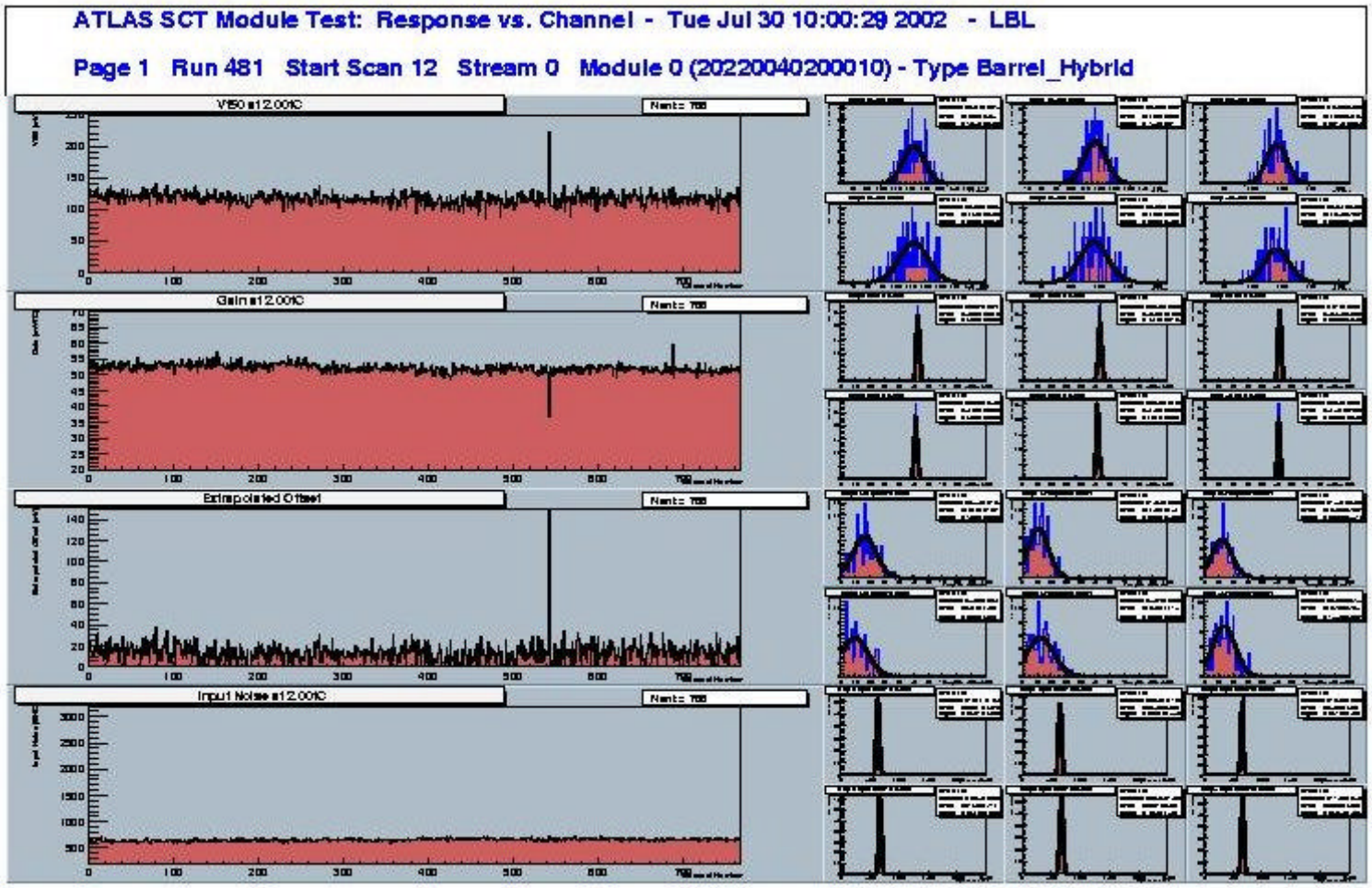


Hybrid 20220040200073
Wafer/Hybrid Comparison



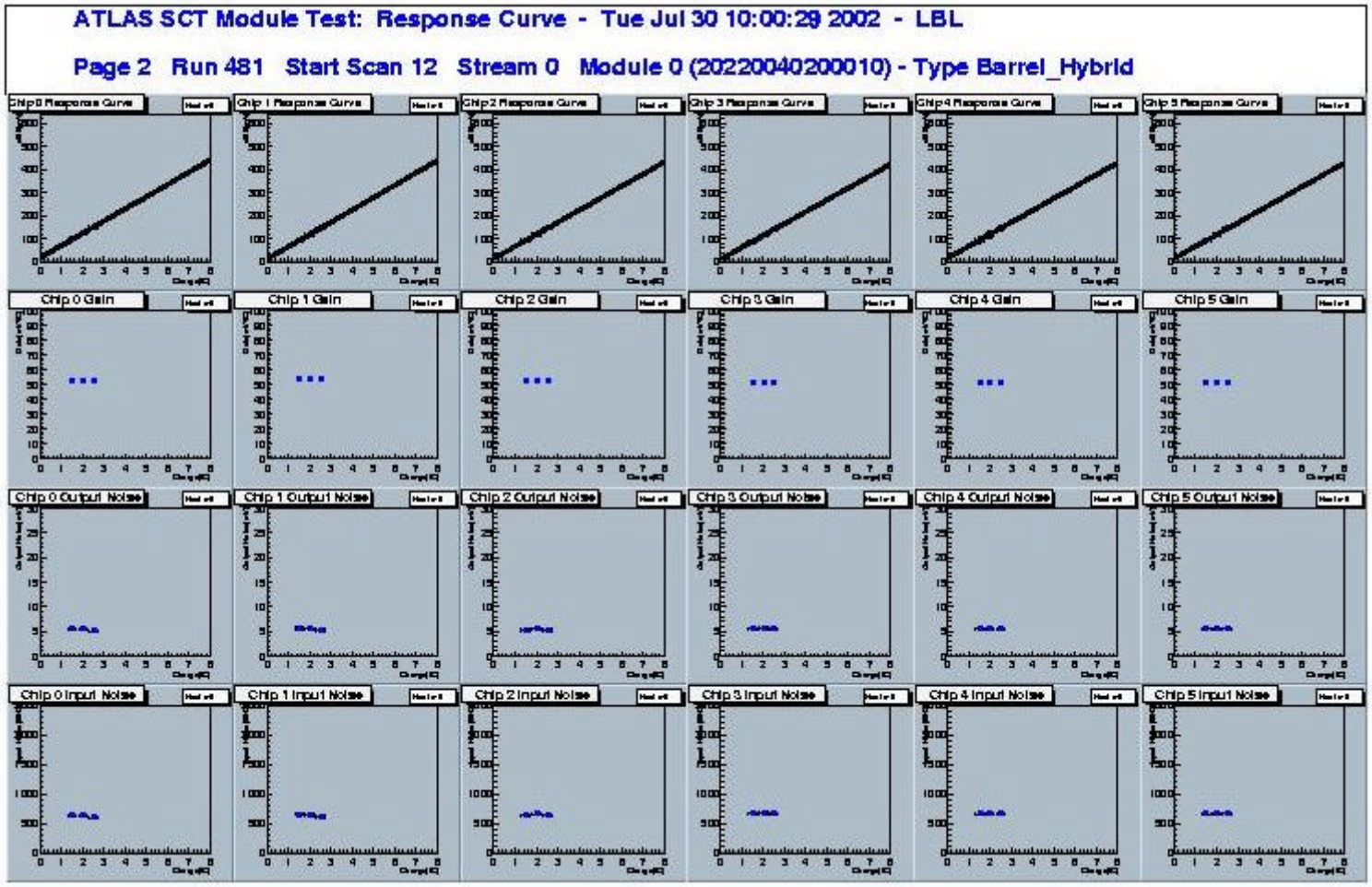
Hybrid 20220040200010

High Offset (low gain)



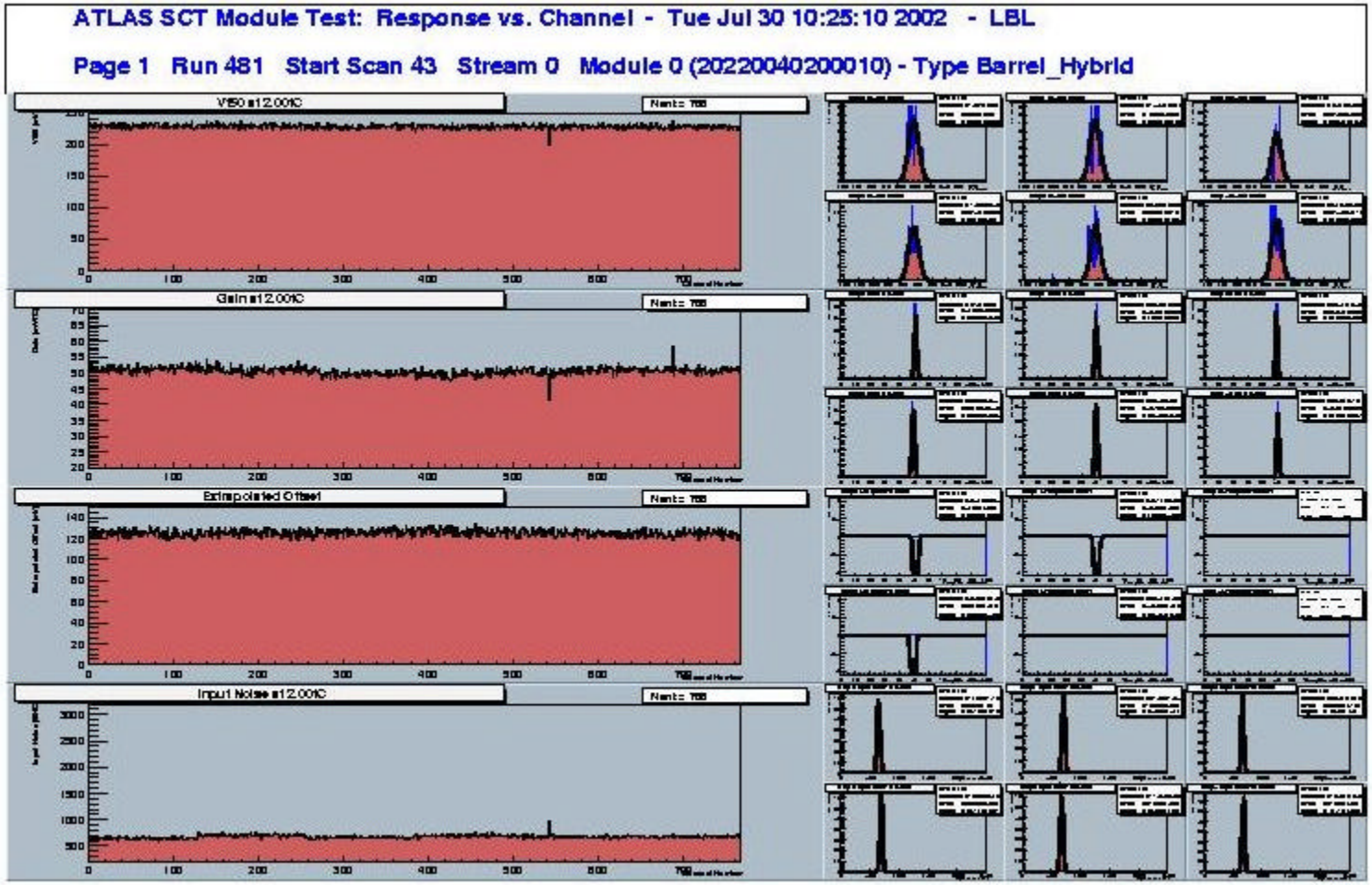
Hybrid 20220040200010

High Offset (low gain)



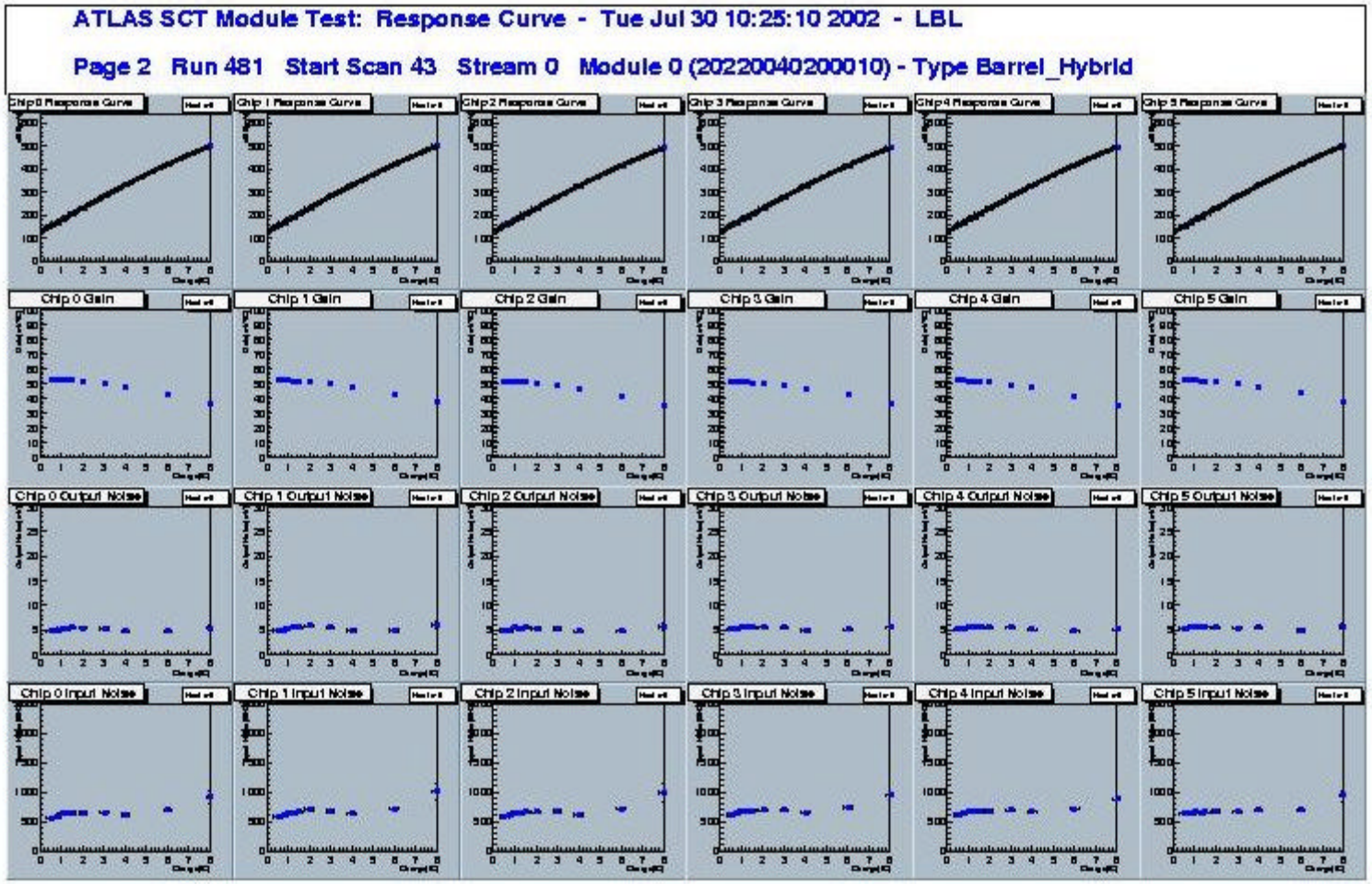
Hybrid 20220040200010

High Offset (low gain)

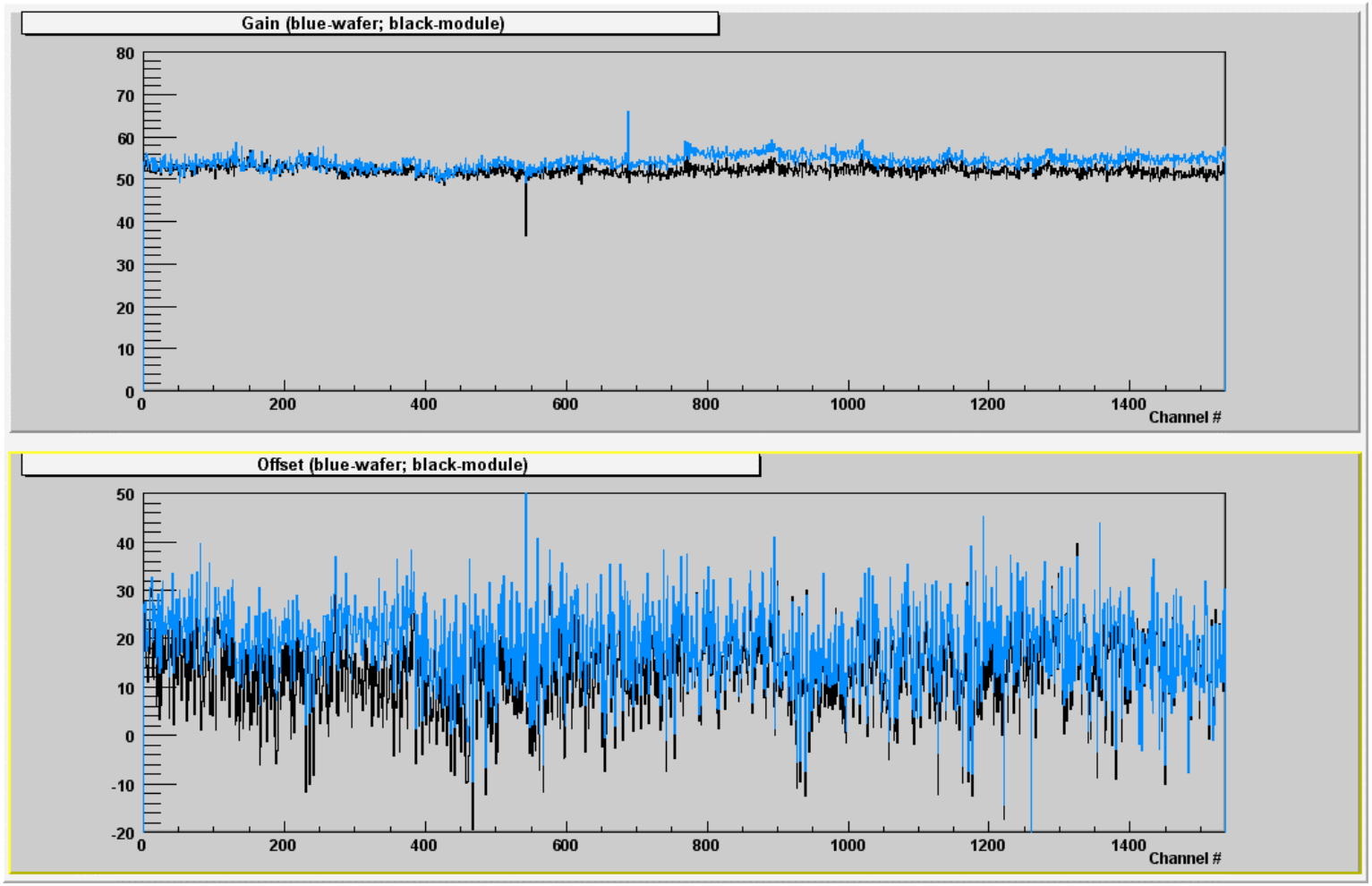


Hybrid 20220040200010

High Offset (low gain)



Wafer/Hybrid Comparison
Hybrid 20220040200010



Chip Response – New Cuts

- New cuts in the TrimRange Scan algorithm

- Noisy channels are now identified by the cut 1.15*(chip mean noise)

- Code to automatically exclude suspect data due to "8fC effect"
  The fitted range is adjusted to exclude points (charge > 5.0fC)
  for which the output noise is > 1.5*the mean output noise taken over all charges

- Channels with anomalous gain are now identified as follows:
  hi_gain channels have gain greater than (1.25 * mean_chip_gain)
  lo_gain channels have gain less than (0.75 * mean_chip_gain).
  This is in agreement with the gain cuts used during chip testing.

Overall Issues

- **Gain non-uniformity** (but mostly in agreement with wafer data)
  - Wafer/Hybrid Comparison to confirm chips are within spec
  - Possible chip pre-selection/better matching from looking at Wafer data of chips available to use

- **Large Gain spread** for several chips on a given hybrid at 0°C (Hybrid LTT) after trim
  - The threshold DAC has a tendency to saturate.
  - This effect kicks in at slightly lower thresholds as a hybrid is cooled down.
  - The 8fC point is out of line (off to higher threshold) during low temperature tests.
  - For some hybrids it can be seen also at room temperature.
  - This can effect the fitting of the response curve, hence the false high gain.
  - Not including the 8fC point in the RC fit helps.
  - Only 1 chip lost at cold (20220040200068)

- **LTT time**
  - LTT- Burn-in test results show no time dependence for defects
    - Any additional defects occur immediately:
    - 1 defective chips (large gain spread at cold)
    - 1 slow chip (at warm)
    - very few noisy/dead channels (almost none)

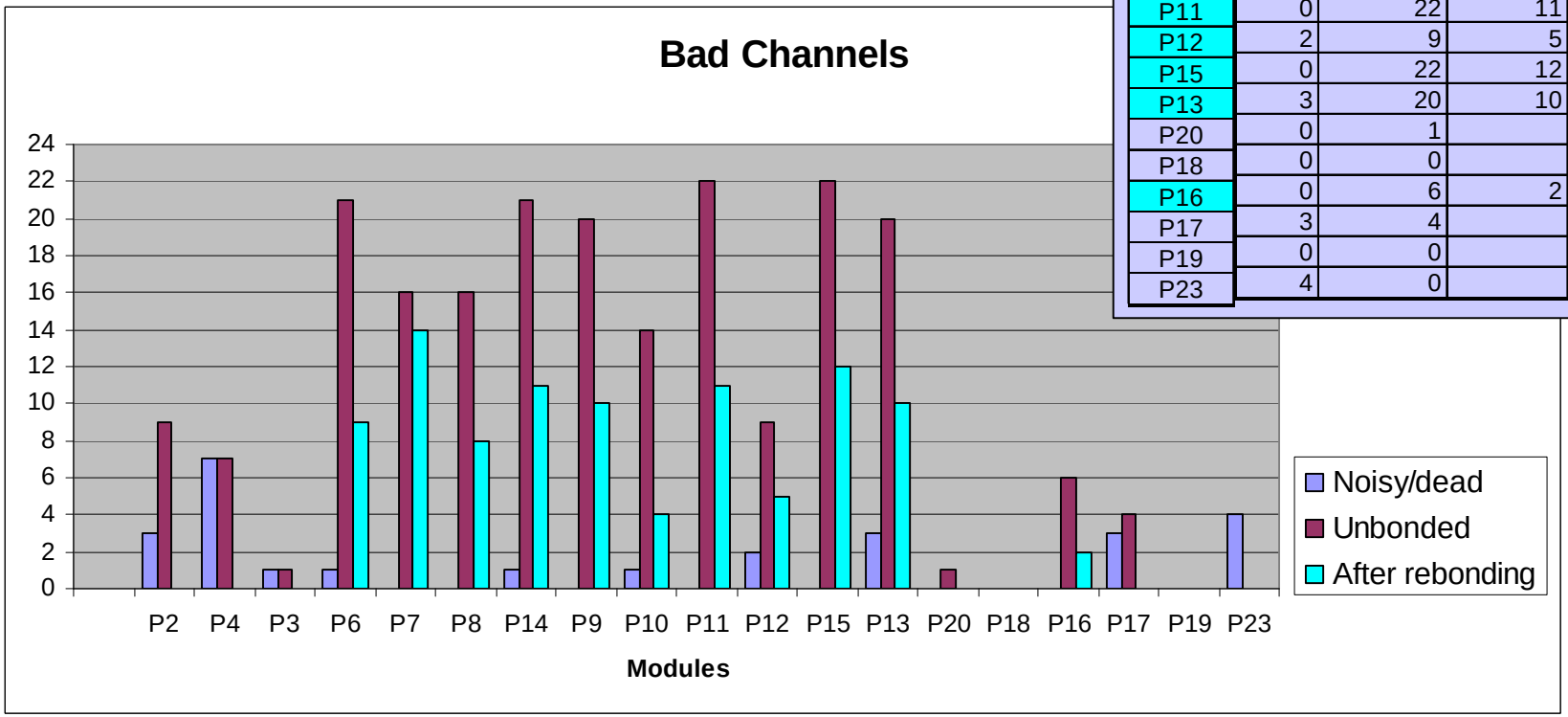
Modules Electrical Results

Hybrid ID	Module	LC(μA) 15^0C 350V Initial	LC(μA) 15^0C 500V Initial	LC(μA) 15^0C 350V before LTT	LC(μA) 15^0C 500V before LTT	Noise Occupancy (LTT)		Noisy/ dead	Unbonded	After rebonding	Total bad channels (Module)
20220040200008	P2	0.758	0.963	0.738	0.922	4.50E-07	3.60E-06	3	9		12
20220040200009	P4	0.195	0.256	0.225	0.266	1.60E-07	6.50E-06	7	7		14
20220040200010	P3	0.256	0.287	0.256	0.297	2.90E-07	3.00E-06	1	1		2
20220040200011	P6	1.097	1.917	0.748	0.861	7.20E-07	7.10E-06	1	21	9	10
20220040200012	P7	0.266	0.307	0.277	0.318	9.20E-07	3.20E-06	0	16	14	14
20220040200013	P8	0.666	0.738	0.625	0.707	8.10E-07	2.30E-05	0	16	8	8
20220040200015	P14	0.328	0.482	0.297	0.369	7.30E-07	3.10E-05	1	21	11	12
20220040200016	P9	0.266	0.287	0.236	0.266	1.70E-07	9.80E-06	0	20	10	10
20220040200017	P10	0.359	0.430	0.410	0.482	7.60E-07	1.10E-05	1	14	4	5
20220040200018	P11	0.285	0.328	0.4	0.502	5.20E-07	4.30E-06	0	22	11	11
20220040200019	P12	0.471	0.605	0.256	0.287	6.30E-07	5.50E-06	2	9	5	7
20220040200020	P15	0.277	0.307	0.41	0.461	1.40E-07	3.80E-06	0	22	12	12
20220040202223	P13	0.369	0.400	0.338	0.471	1.50E-06	4.50E-06	3	20	10	13
20220040200024	P20	0.195	0.215					0	1		1
20220040200028	P18	0.205	0.246	0.205	0.246	1.60E-05	6.90E-05	0	0		0
20220040200037	P16	0.379	0.451	0.225	0.256	2.00E-07	2.00E-05	0	6	2	2
20220040200038	P17	0.174	0.225	0.205	0.246	9.70E-06	1.00E-04	3	4		7
20220040200040	P19	0.215	0.246	0.236	0.256	1.10E-05	5.90E-05	0	0		0
20220040200041	P23	0.543	0.738					4	0		4

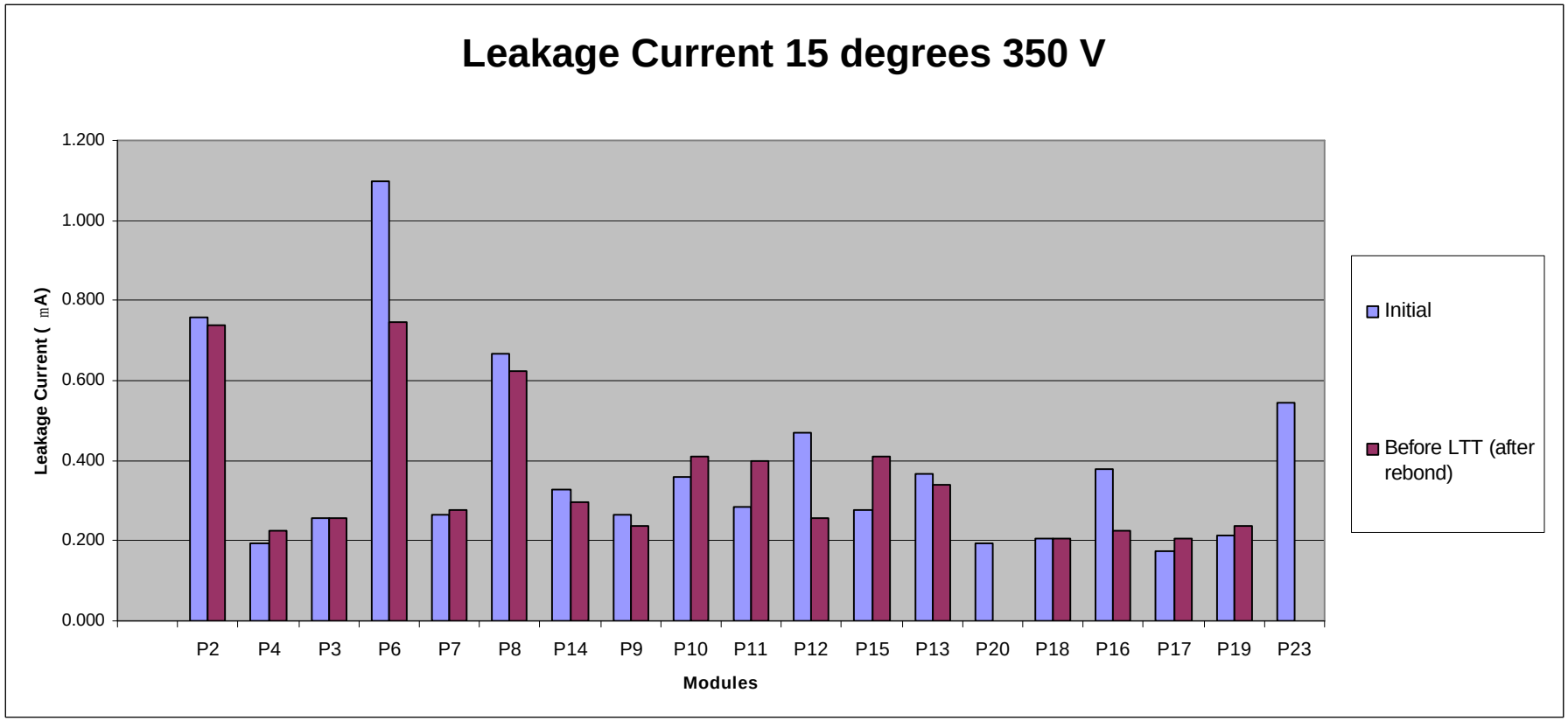
- 19 electrical modules built (as of Feb 27) + 2 new not electrically tested yet
- 17 modules all tests completed + 2 in progress

Bad Channels

Module	Noisy/ dead	Unbonded	After rebonding	Total bad channels (Module)
P2	3	9		12
P4	7	7		14
P3	1	1		2
P6	1	21	9	10
P7	0	16	14	14
P8	0	16	8	8
P14	1	21	11	12
P9	0	20	10	10
P10	1	14	4	5
P11	0	22	11	11
P12	2	9	5	7
P15	0	22	12	12
P13	3	20	10	13
P20	0	1		1
P18	0	0		0
P16	0	6	2	2
P17	3	4		7
P19	0	0		0
P23	4	0		4

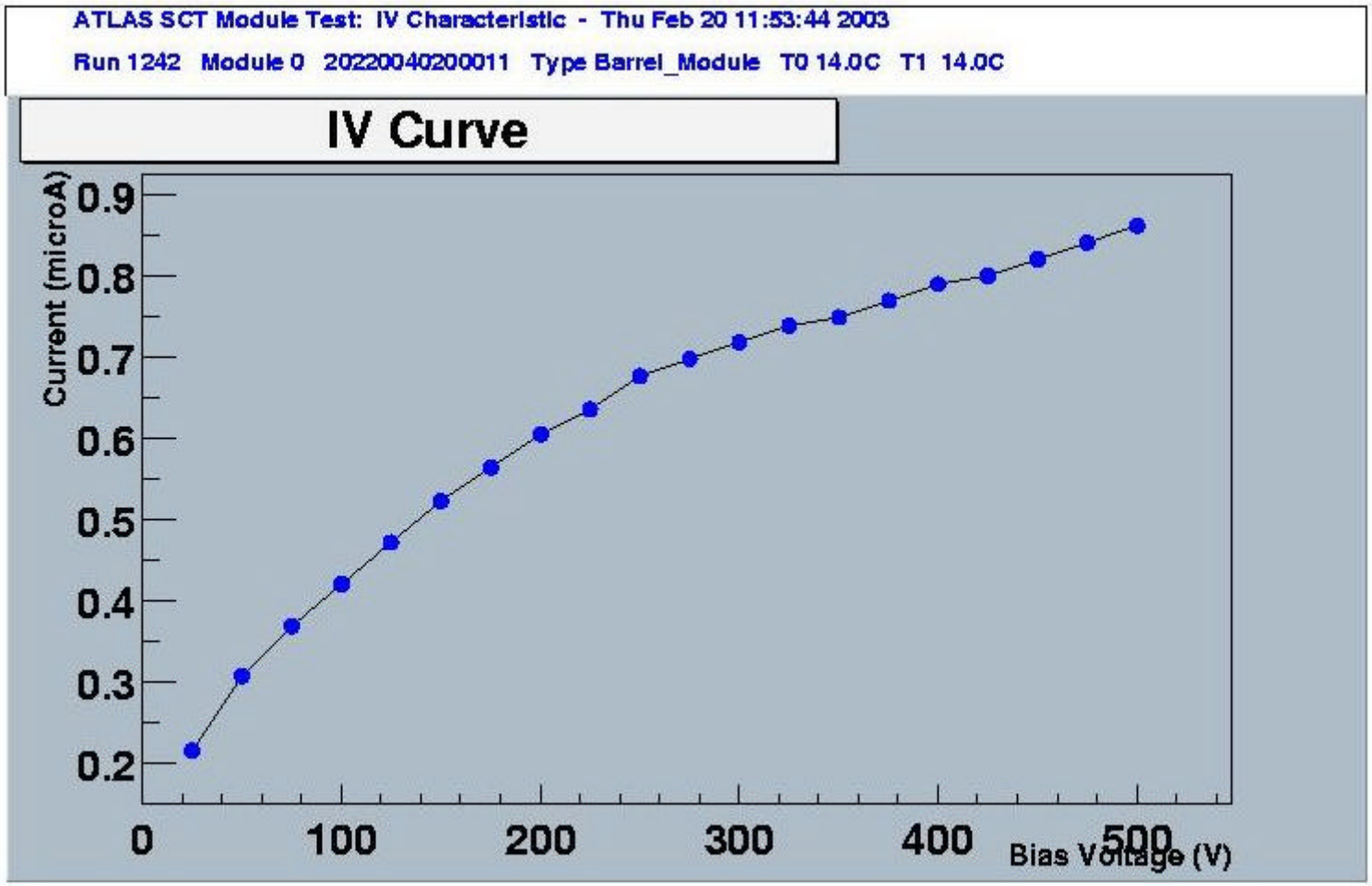


Leakage current after rebonding



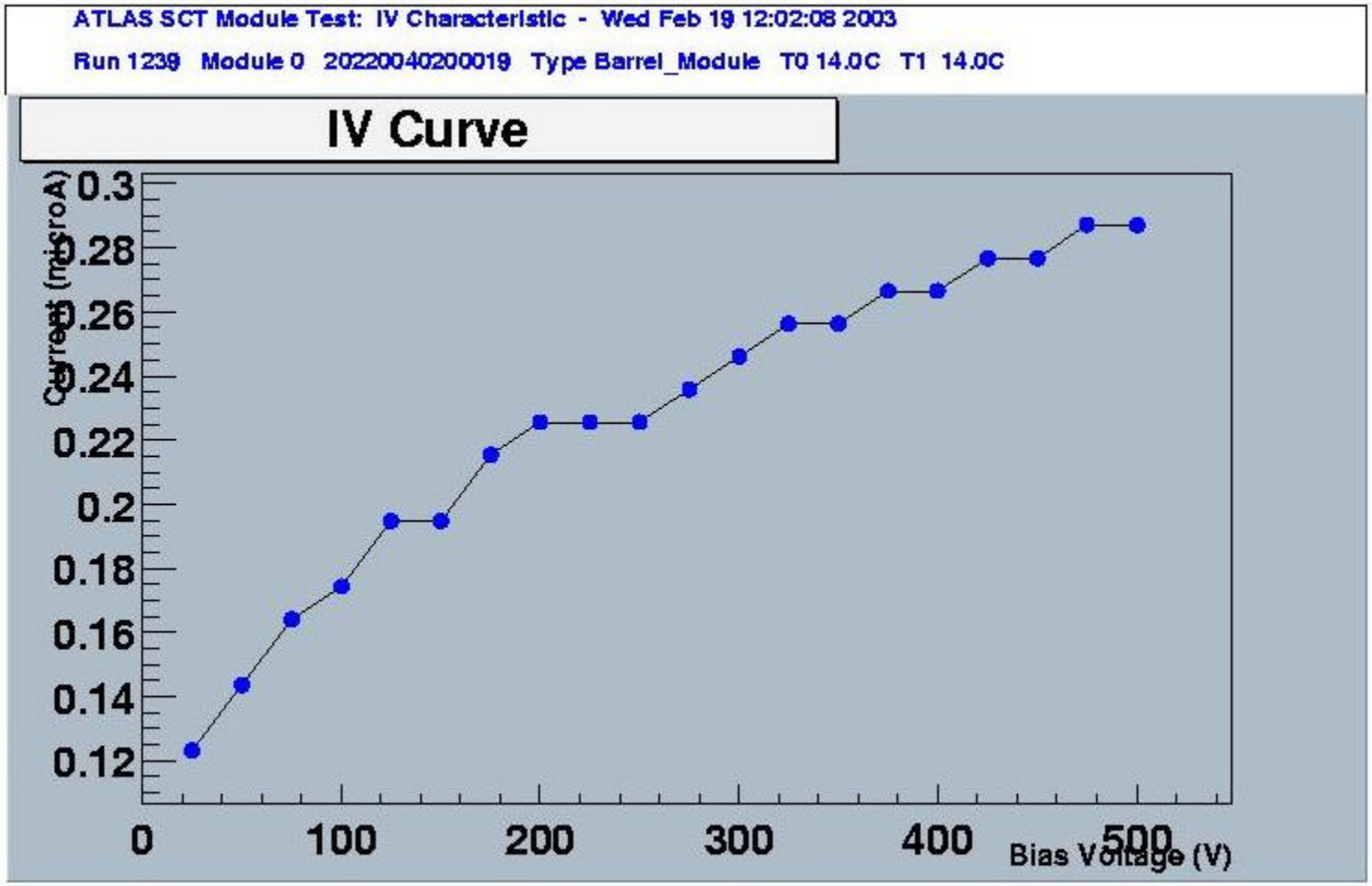
Module P6 (20220040200011) IV Curve

15^0 C



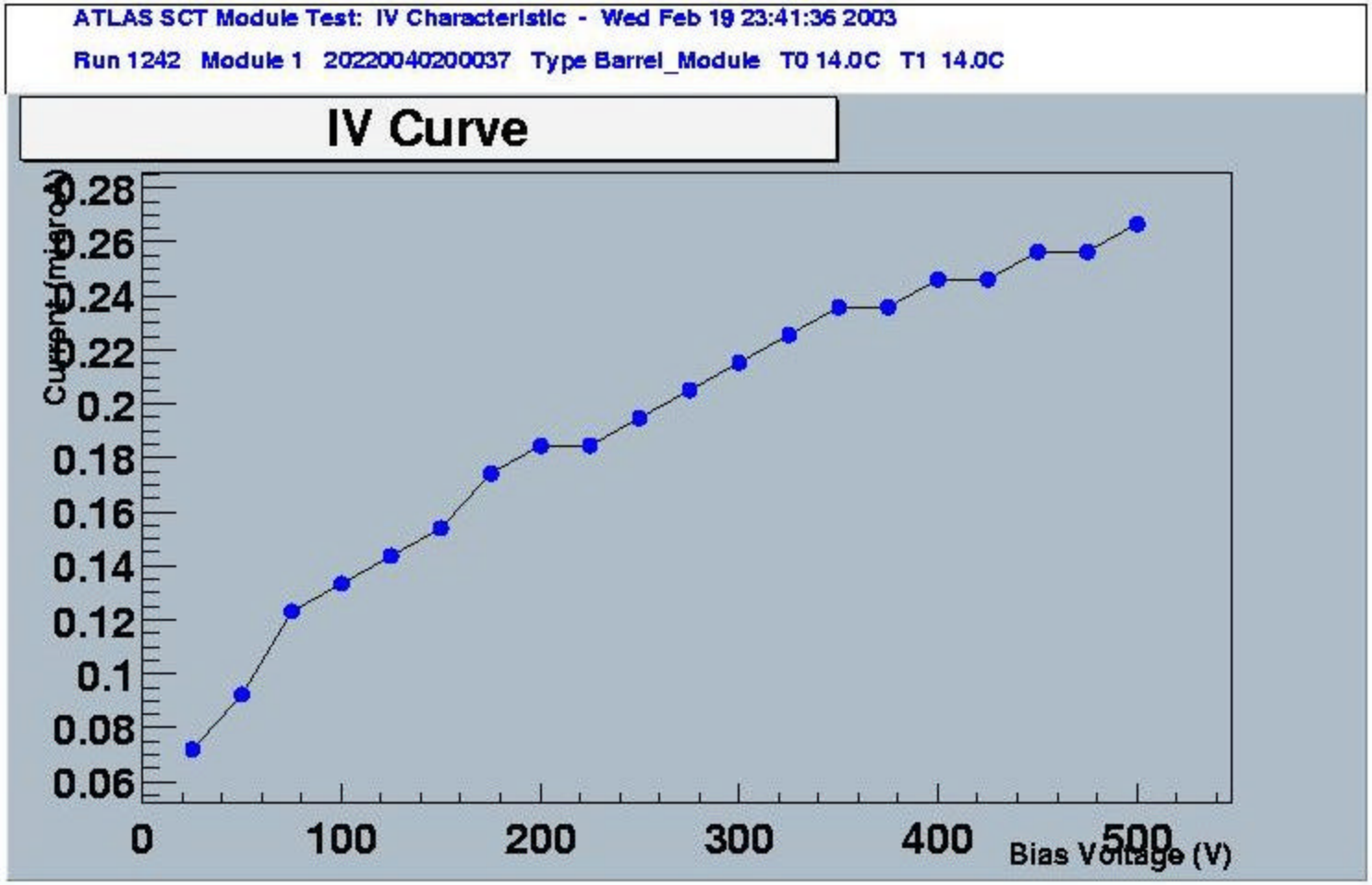
Module P12 (20220040200019) IV Curve

15^0 C



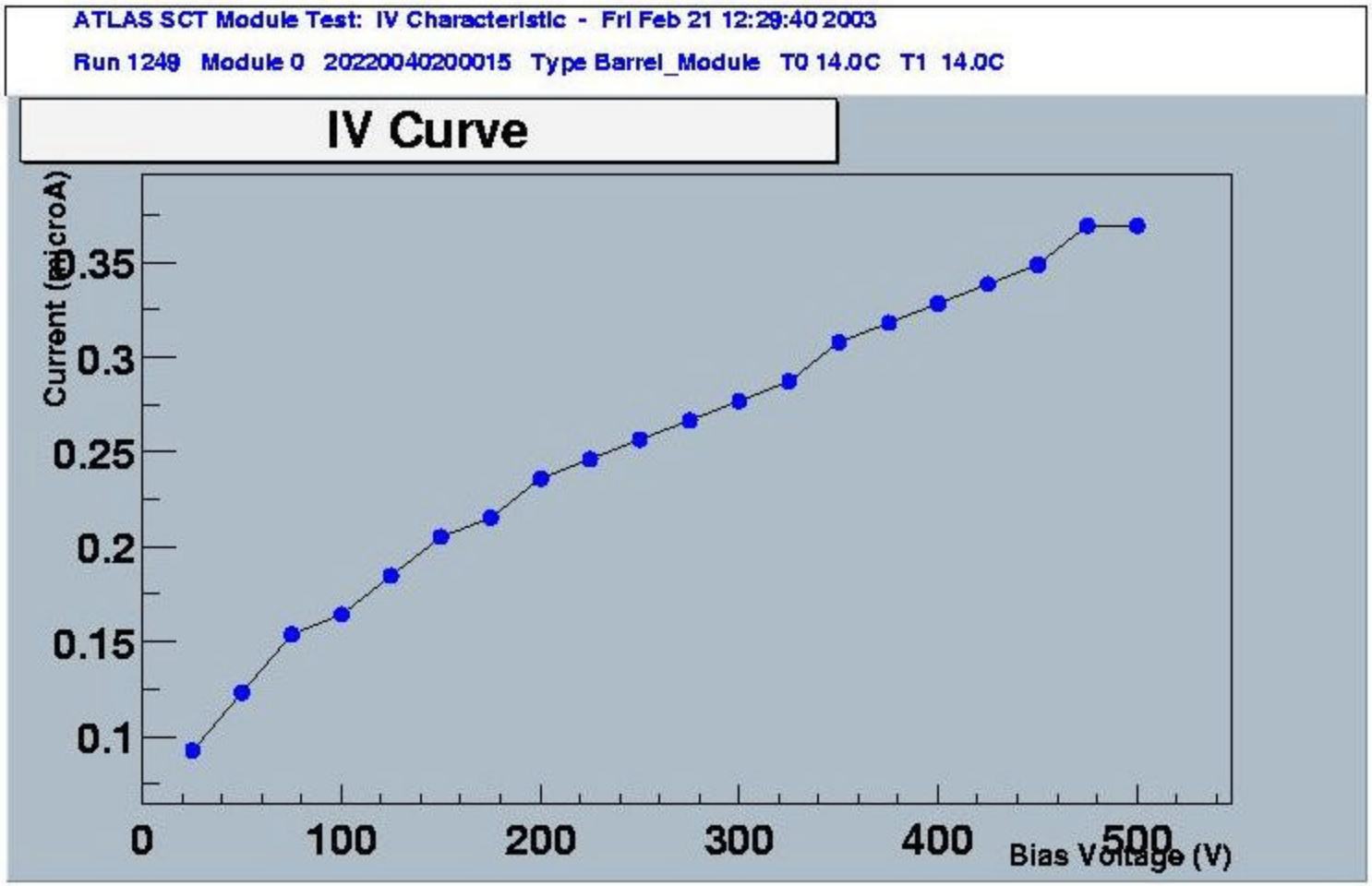
Module P16 (20220040200037) IV Curve

15^0 C

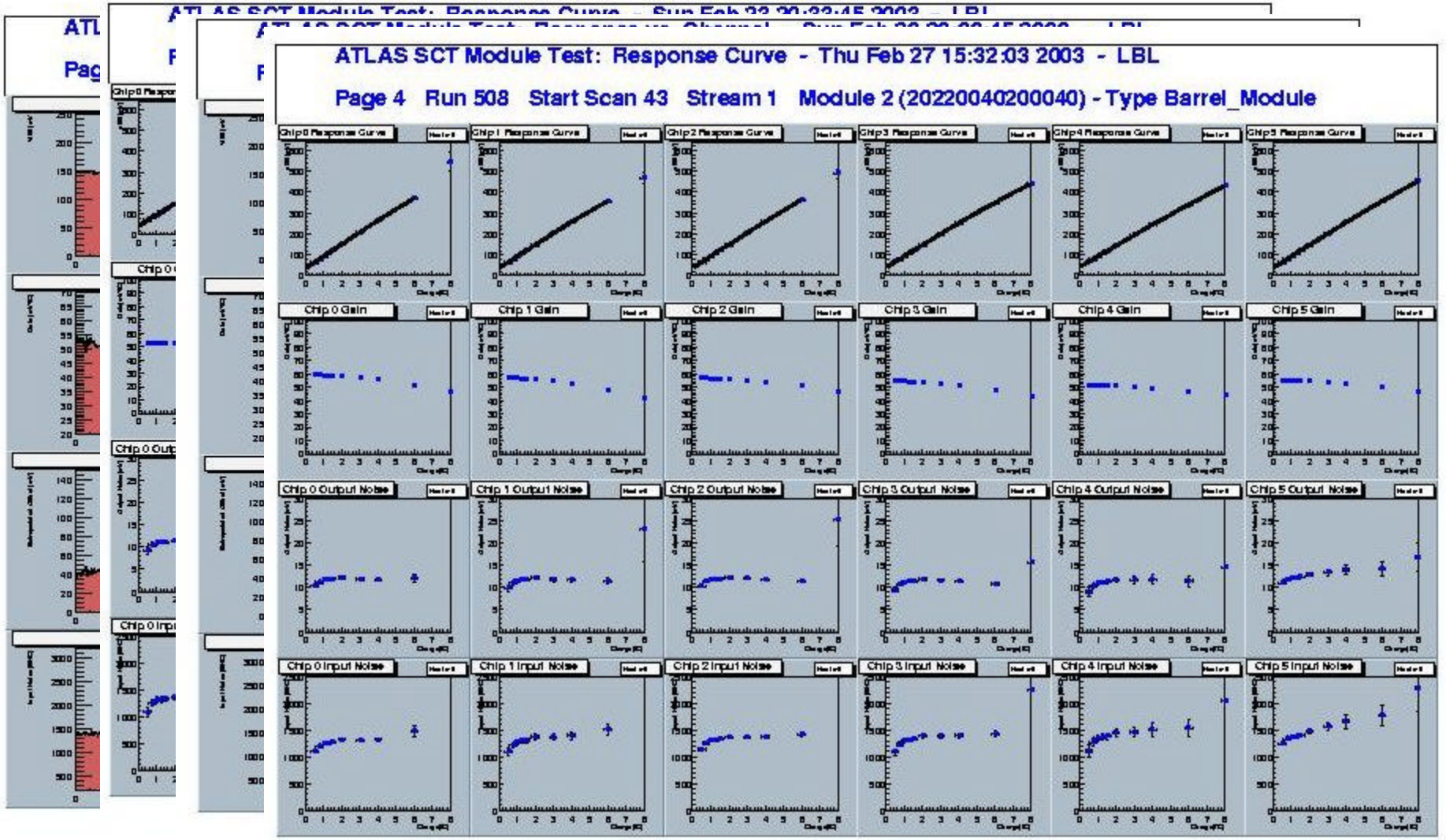


Module P14 (20220040200015) IV Curve

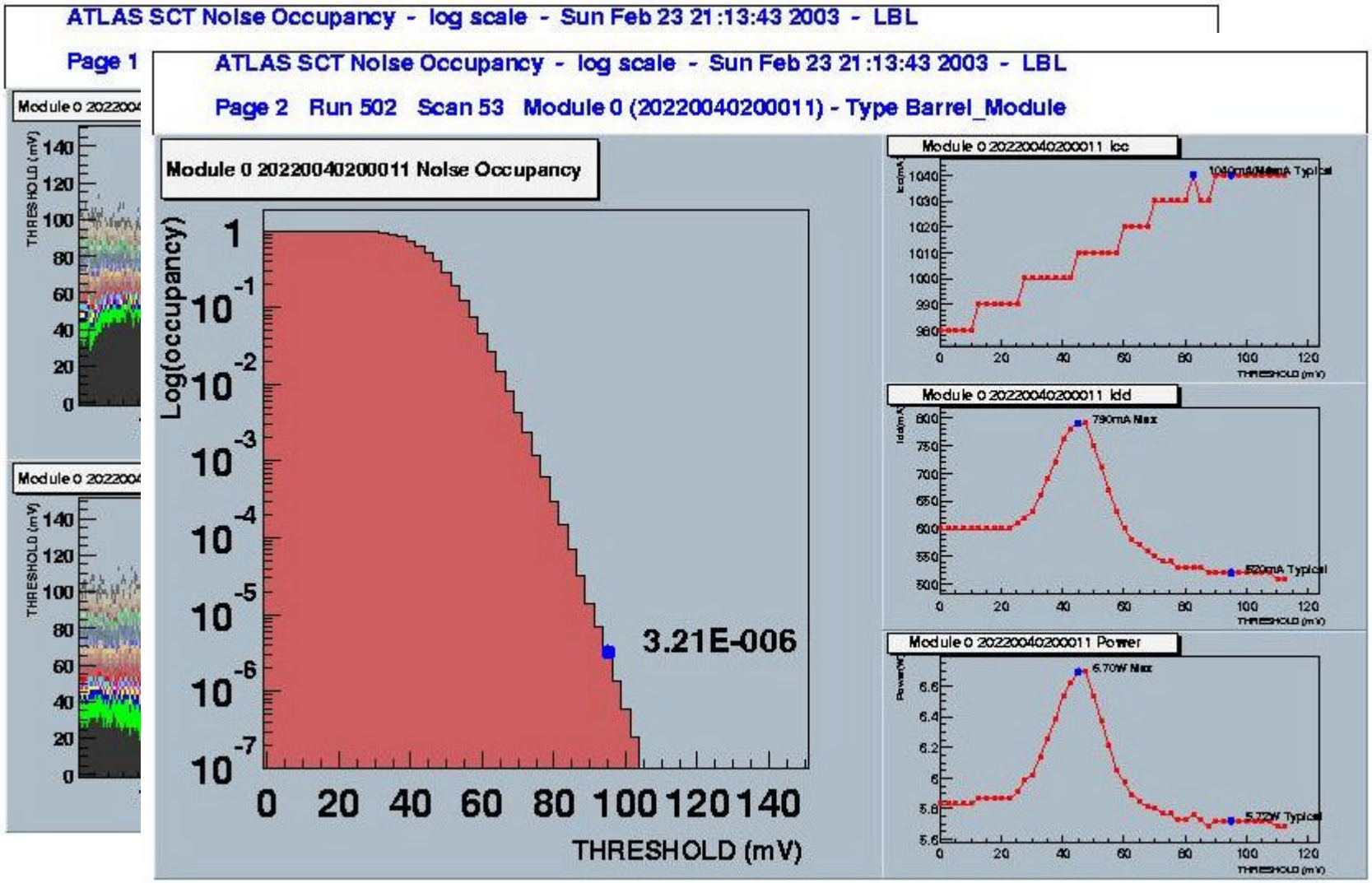
15^0 C



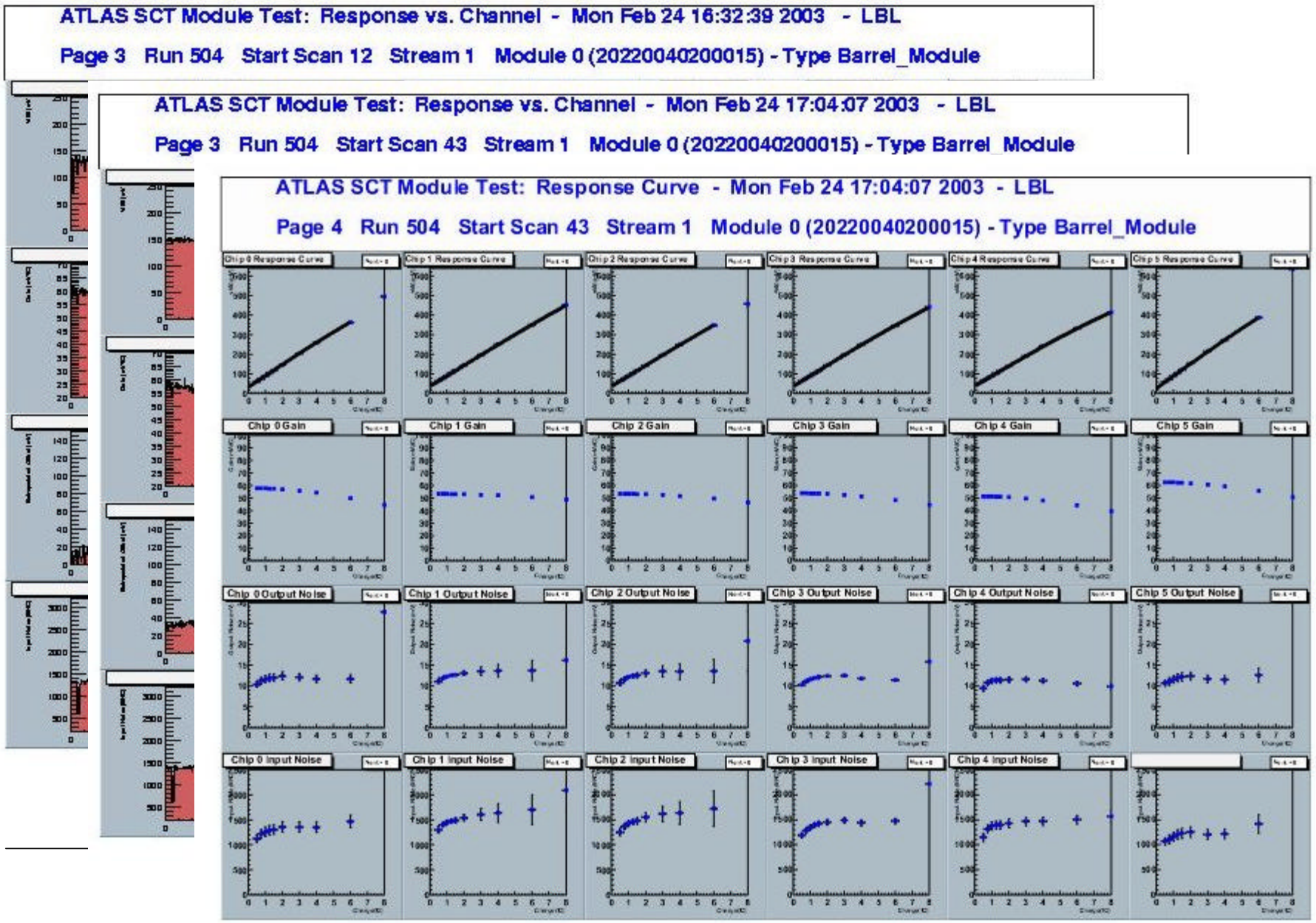
Module P6 (20220040200011) RC Plots



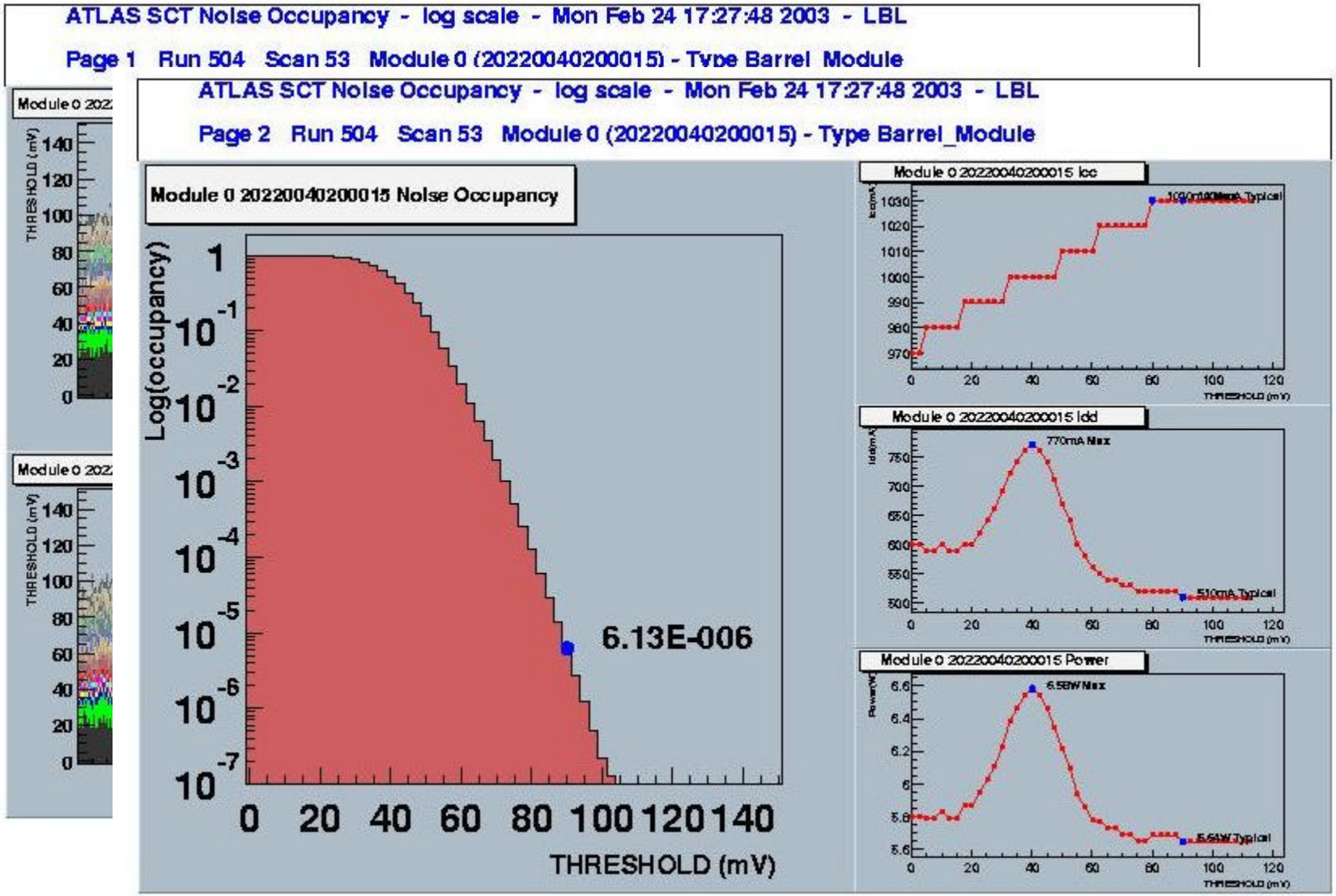
Module P6 (20220040200011) NO Plots



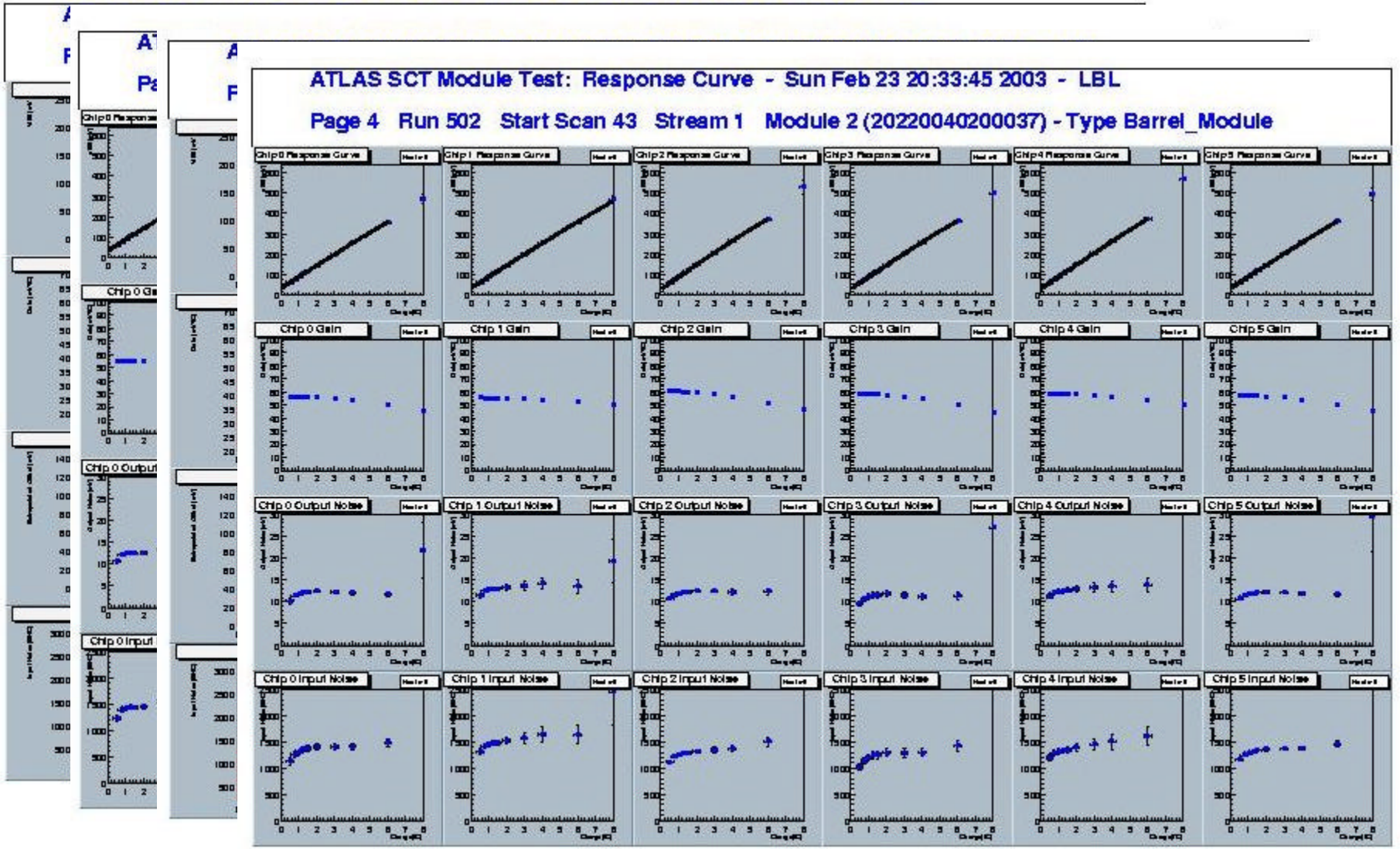
Module P14 (20220040200015) RC Plots



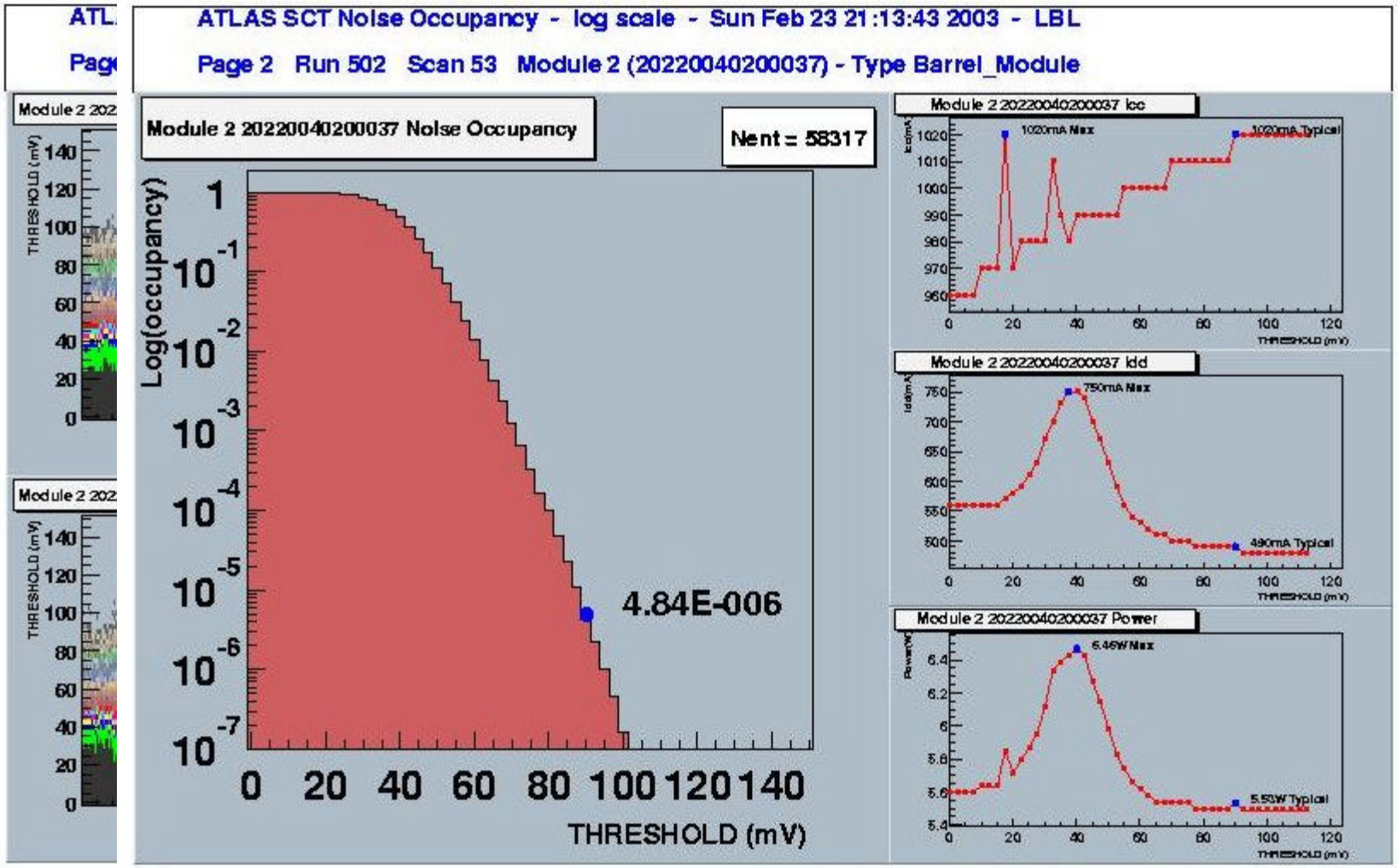
Module P14 (20220040200015) NO Plots



Module P16 (20220040200037) RC Plots

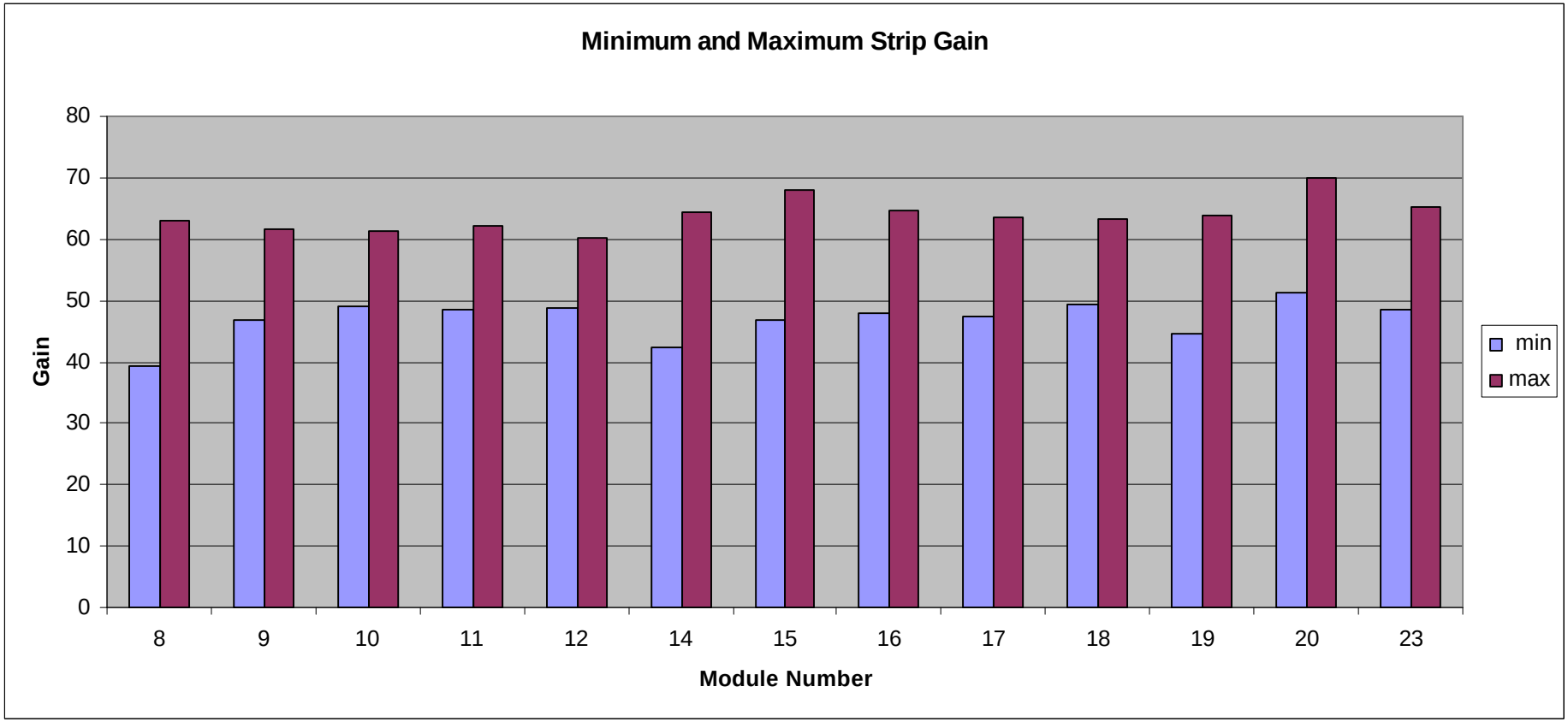


Module P16 (20220040200037) NO Plots

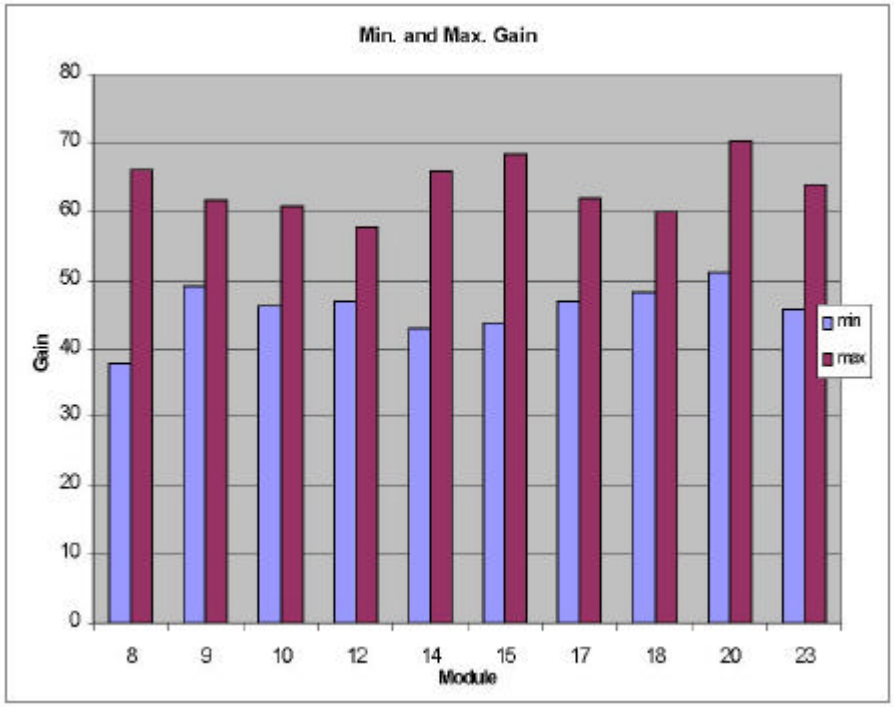


GAIN

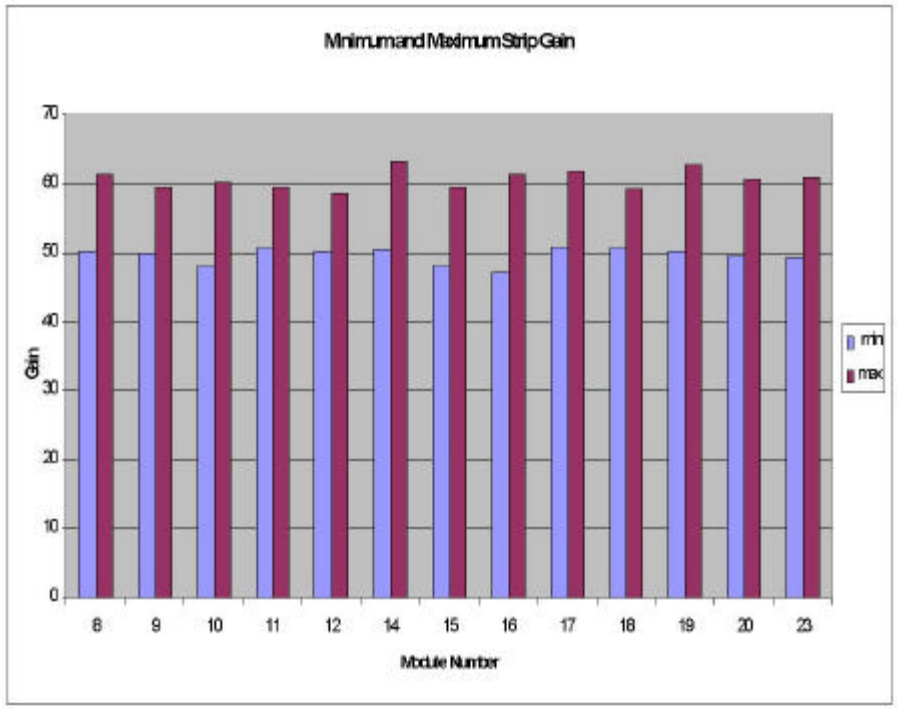
After trim



GAIN



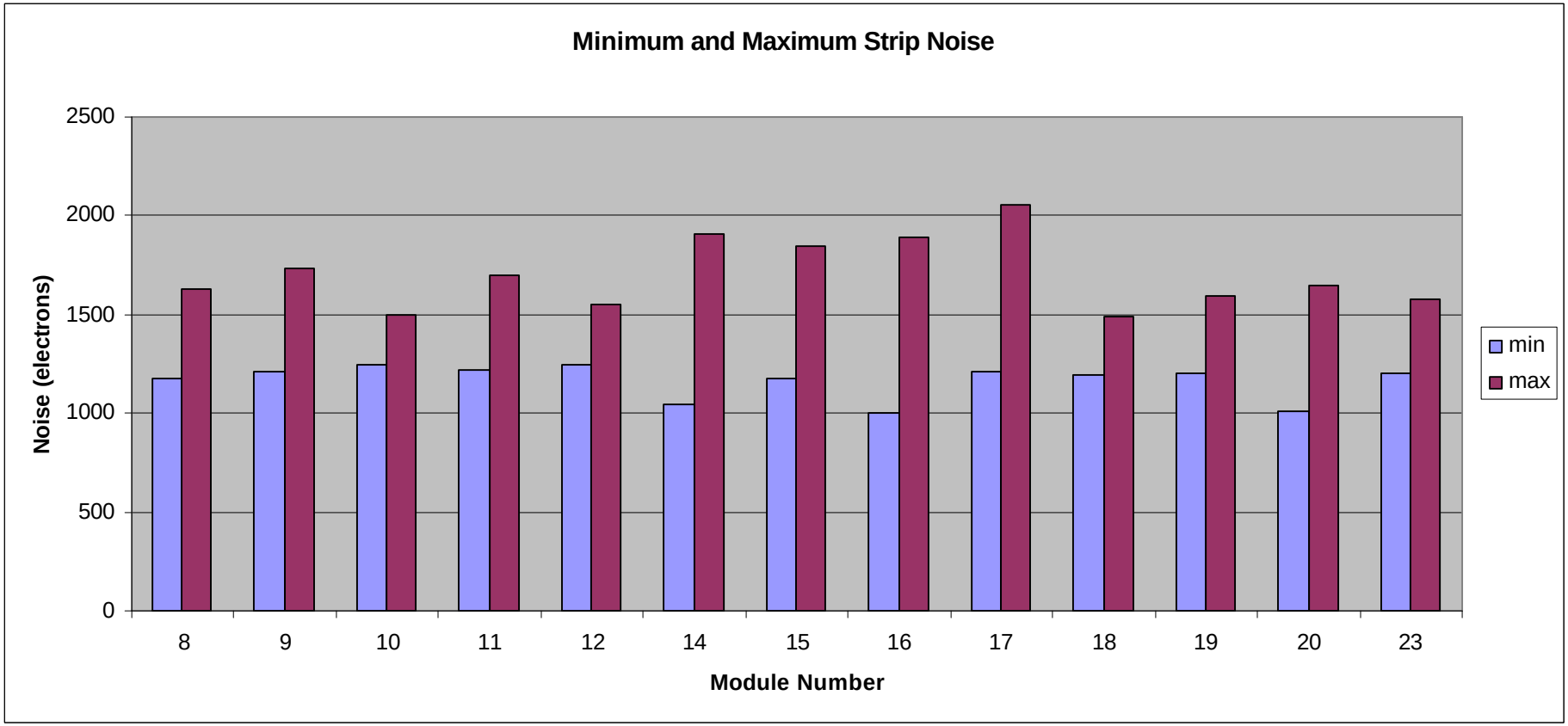
raw



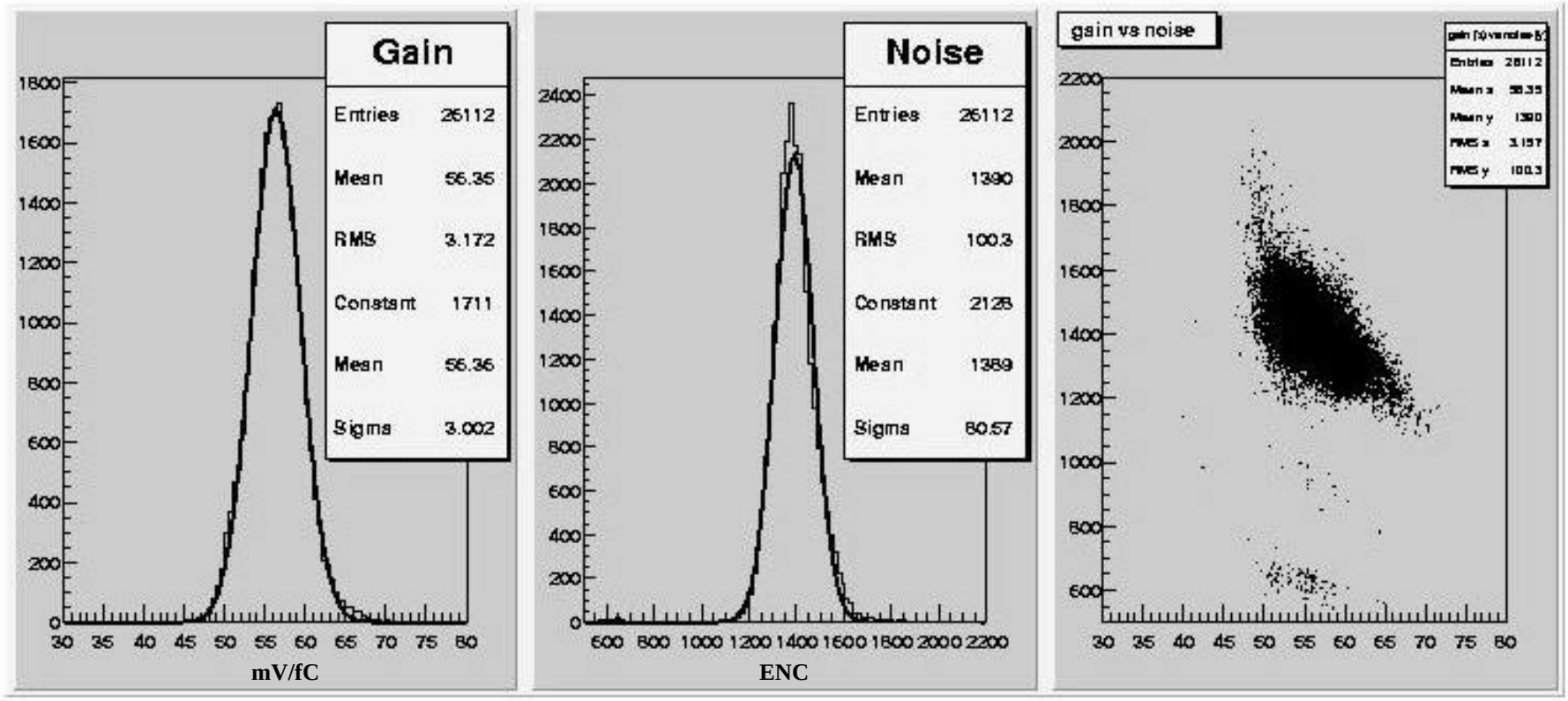
chip mean subtracted +55

NOISE

After trim

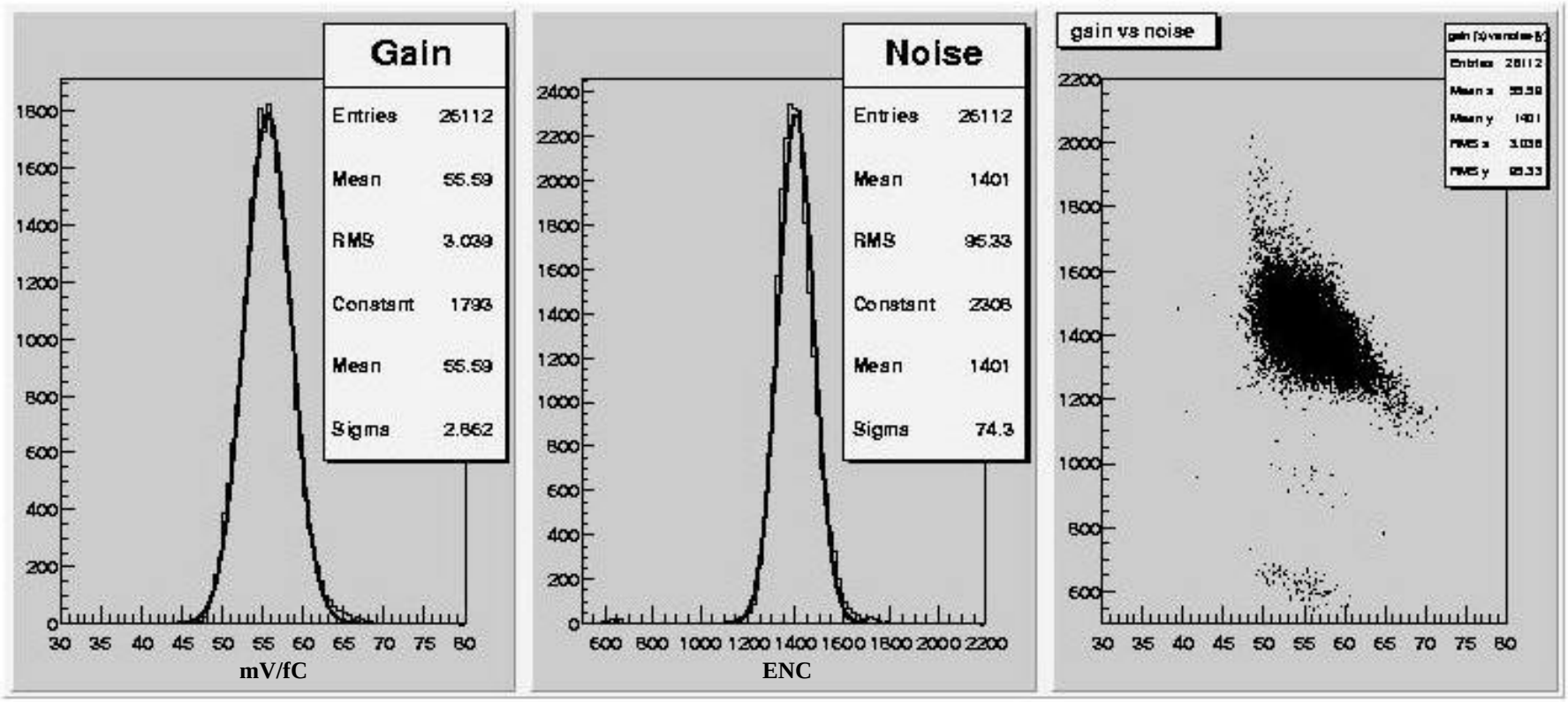


Gain vs NOISE



Before trim

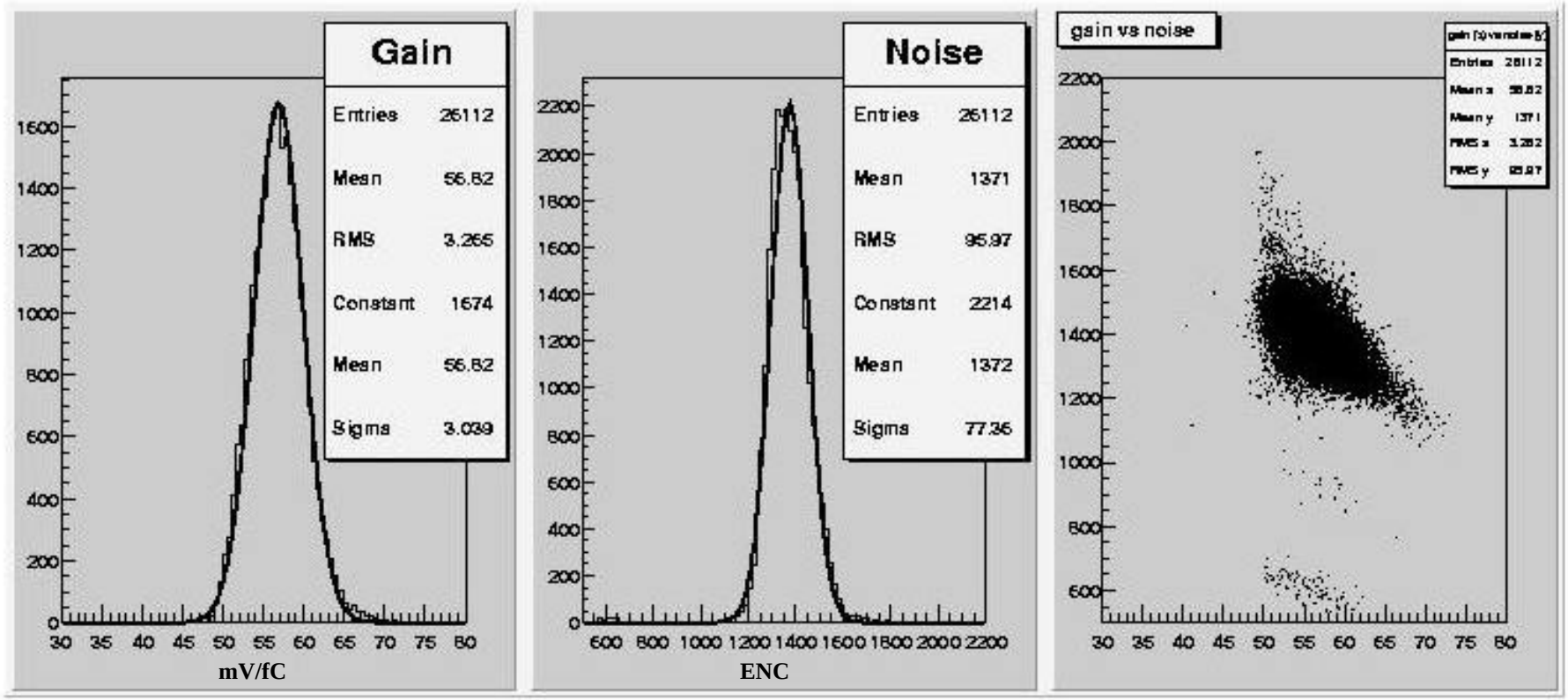
Gain vs NOISE



After trim

Gain vs NOISE

With Cap correction factors



Summary

HYBRIDS

- **Defective Chips**
  12 chips defective after electrical testing + **2** damaged (chipped)
  Gain(6) Token(1) TW (1) Strobe Delay (1) TrimDAC (2) High Offset (1)
- **Wafer/Hybrid comparison**
  - used regularly and especially when anomalies are present
  - effective tool for chip selection
- New features/cuts in the software helps with anomalous chip response
- **LT-Tests** show no time dependence for defects: time could well be reduced to a few hours

MODULES

- **19 modules built** as of Feb 27 **+ 2** just assembled
- 17 modules completed with testing + 2 in progress
- **PA defect** on first batch of 29 hybrids
  - 15 hybrids already used in modules (11 rebonded)
  - 9 modules with 8-14 final unbonded channels (50% channel regained)
  - 14 hybrid still to be used but fixing bonds during rebonding -> good yield
  - 4 new hybrids used in modules
- HV boards communication/protocol more stable after Peter's upgrade of the software
- **No additional defect found in modules through sequence of tests**