Second proposal of pin assignment for the bias voltages in the 0.05" through-hole type interface connector between the module and the power/DAT cable

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This proposal concerns the pin assignment of bias voltage lines in the interface connector and replaces the previous proposal[1].

The ATLAS SCT barrel module has a pig-tail Kapton cable from the hybrid in order to interface with the power and data transmission (DAT) cables. The pin assignment of the interface connector has been proposed, see e.g., C.Haber at SCT workshop at Santa Cruz, July 97.

In the original assignment , the negative bias high voltage was assigned to Pin#2. The positive bias (analog ground level) being assigned to Pins#1 and #3, and in case when the negative bias shall go in the same layer, it must go through the gap of Pins#1 and #3. This might be too tight for the high voltage such as 500 volts. The situation is true as long as we use the through-hole-pin type connector even if the negative bias line is in the different layer.

In the previous proposal, a new pin assignment was proposed, the Type1 in Fig. 1. The voltage assignment to the Pin#1 and #2 was swapped so that the ground level line could detour the high voltage pin. For this proposal, T. Smith and V. Cindro have commented the breakdown voltage of the connector and the traces on the PC board. Cindro tested the MOLEX ZIF connector with one pin floating could hold 1 kV.

After surveying the breakdown voltages of the Kapton/Cu cable, we've found:

1. There is data from a Kapton/Cu flex board/cable vendor. Trace with cover-film has very high breakdown voltage, about 1 kV in 0.1 mm gap. Trace without cover-film has much lower breakdown voltage. The breakdown voltage data without cover-film[2] is reproduced in Fig. 2. The measurement is in the room temperture and the room humidity. The minimum gap between the lands for the 1.27 mm pitch pins is 0.3 mm. The breakdown voltage of the gap of 0.3 mm is 300 volts with including a 50% safety factor.

According to the data, it is clear we have to skip one pin in order to hold more than 300 volts safely. New types of pin assignments we can think of are presented in Fig. 1: Type 2 and Type 3. The type 2 has extra pins for the ground level lines in order to sandwich the high voltage, and requires four pins more (or two rows more). Since the material

1. T. Kohriki, et al., "Proposal of proposal of pin assignment for the bias voltages in the interface connector between the module and the power/DAT cable", 97/10/19, (see "http://atlas.kek.jp/~unno/si_hybrid.html")
2. Data sheet of Mektec, Nippon Mektron Co. Ltd., 1-12-15 Shiba-Daimon, Minato-ku, Tokyo 105, Japan

reduction is the primary concern, since the same bias current is running both ground-level and high voltage, and since the high bvoltage pin is at the end of the connector, there seems no reason to have more connections in the ground-level.

The above arguments lead us to propose the Type 3 configuration:

1. Two pins for each bias line.
2. The high voltage is sandwiched with the ground-level line by extending the line as shown in the figure
3. No metal-plating in the pin-holes 3 and 4. It would be better to remove the pins 3 and 4 from the connector.
4. The traces on the Kapton is covered with cover-film.

For easy later referecing, the Type 3 configuration is reproduced in Fig. 3, by itself.

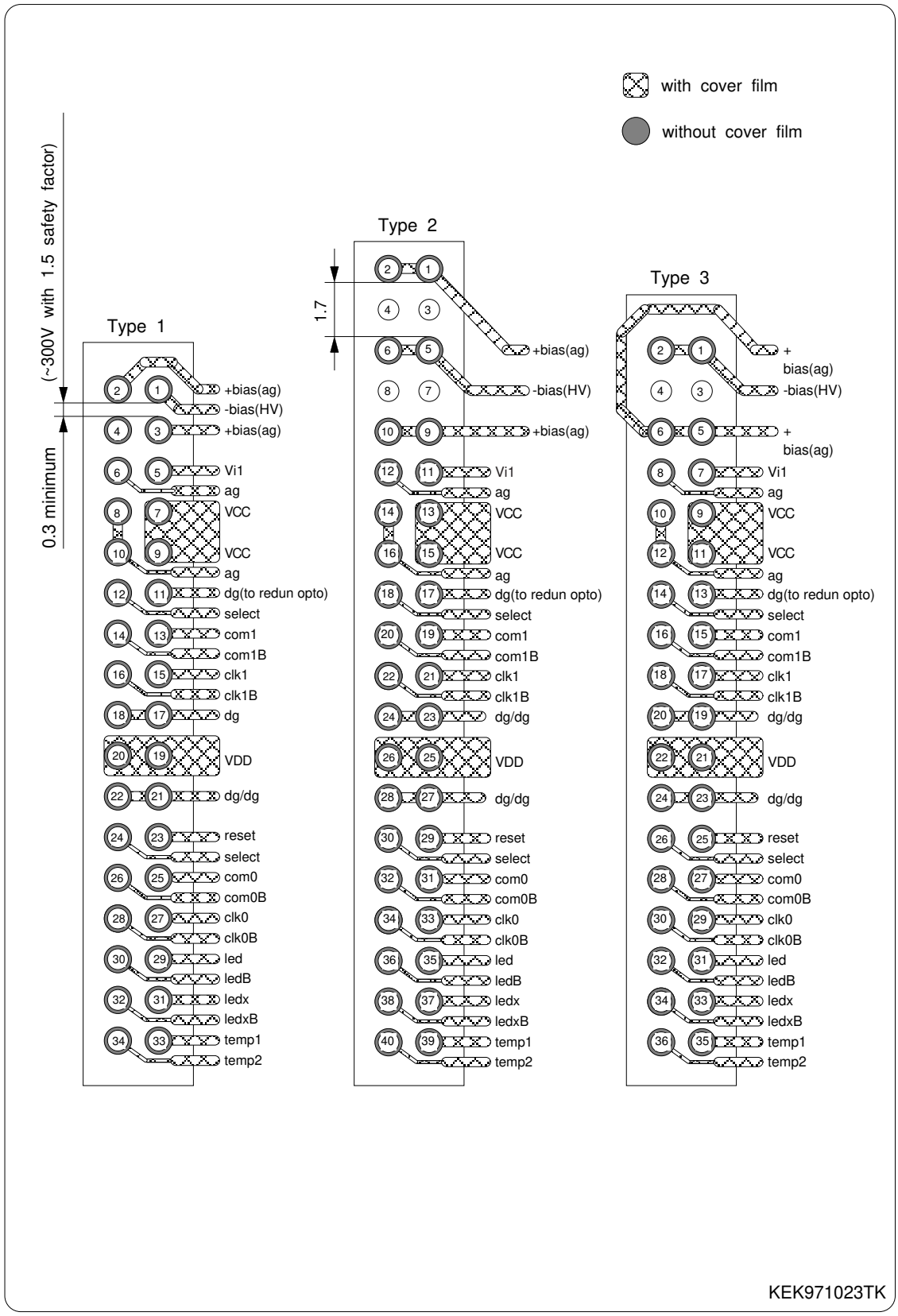

Fig. 1 Variations of pin assignment of high voltage lines

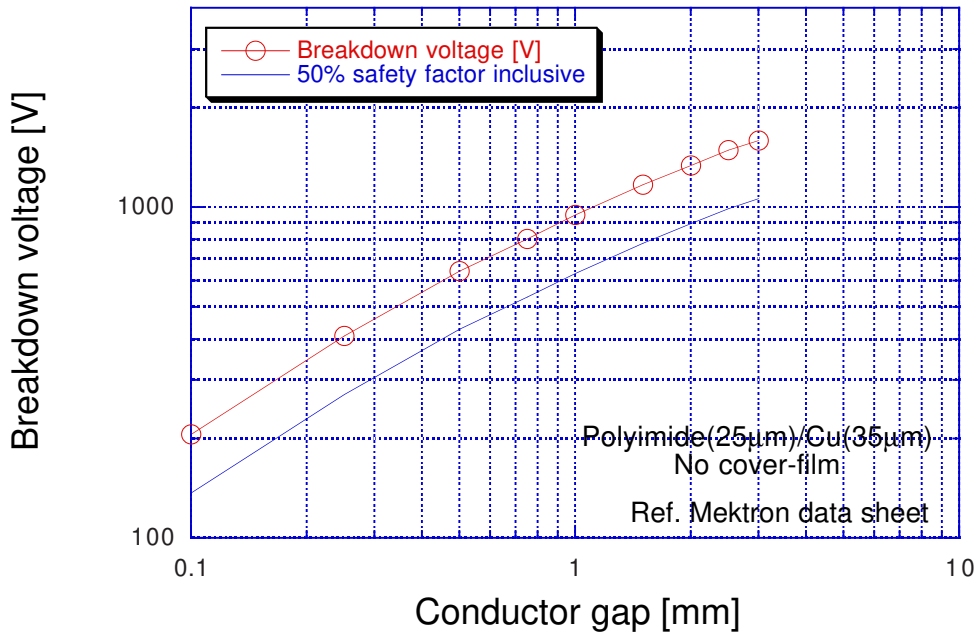

Fig. 2 Breakdown voltage of the Cu traces on Polyimide film

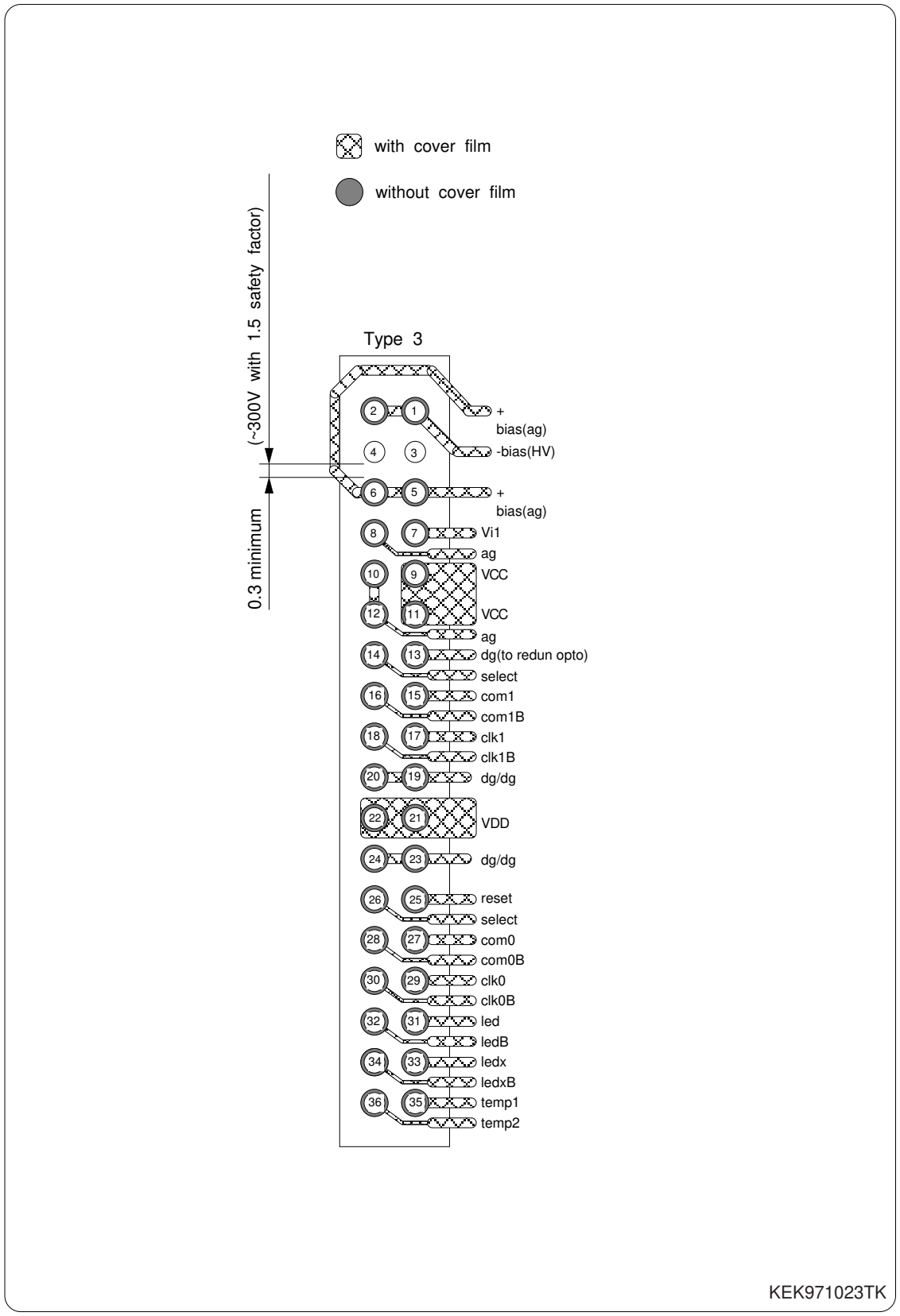

Fig. 3 Proposal for the pin assignment for high voltage lines