Hybrid and Electrical and Mechanical Modules at KEK

(Updates in May 00 SCT week)

Y. Unno, et al.

KEK and ATLAS-Japan SCT group

- Design documents
- A few reminders of the thermo-mechanical measurements
- Electrical modules
- Summary
Design documents

• “Design and fabrication of the ABCD Kapton Hybrid”, Sep. 30, 1998,
  - Text and figures are needed to be revised, however,
  - latest updates of figures and drawings are available from the web page

• A draft of the “stuffing and assembling into module” is also available
  - Simple and skeleton, but exits
  - Improvement is foreseen
Design and Fabrication of the ABCD Kapton Hybrid

September 30, 1998

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Abstract

A hybrid plane with polyimide (Kapton) multilayers is designed and fabricated in order to demonstrate its feasibility for the application to the ATLAS barrel SCT modules using the ABCD chips.

1. Motivation

We propose to use a multi-layered flexible printed circuit technology based on Polyimide (Kapton) base material for constructing the hybrid of the ATLAS microstrip silicon detector. We think there are several advantages in using this particular technology:

1. The technology has been widely used in commercial products such as printers, note-type computers, video/photographic-cameras, portable music players etc.

2. The hybrid can be easily folded and so all-in-one hybrid structure (see Figure 1) is possible including everything from connector, connector extension, top-hybrid, interconnection, and bottom hybrid. In comparison with separate-hybrid structure, this all-in-one structure significantly reduces number of parts needed and simplifies the labor/time-consuming connection/assembly works. It helps also in reducing troubles in electrical connections.

3. Radiation length of the material can be smaller.

4. Production cost could be much reduced.

2. Manufacturer

We have made a contact with a manufacturer, Mektec Corporation which has branches at Tokyo, San Jose, Singapore, Weinheim. This company has a dominant marketing share in Japan in the field of flexible printed circuit.
Hybrid stuffing and assembling into module

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I. INTRODUCTION
The ABCD kapton hybrid is distributed with
- Carbon-carbon bridges glued
- Glass pitch-adaptor glued.

The stuffing and assembling steps of the hybrid are
1. solder passive components: resistors, capacitors, connector
2. glue ASICs with silver-loaded conductive epoxy
3. wire-bond ASICs and AGND-DGND pads
4. glue the hybrid on the sensor-baseboard assembly
5. wire-bond channels and HV bias connections

The web page, http://atlas.kek.jp/~unno/si_hybrid.html shows,

Kapton hybrid designs:
- Component loading diagram (pdf) (1 page)
- Circuit diagram (pdf) (2 pages, shows wire-bond locations)
- Glass pitch adaptor (pdf) (1 page)

The component loading shows where components are physically stuffed. The circuit diagram shows details of electrical connections and wire-bondings. The glass pitch adaptor drawing shows the detail of the wire-bondings around the pitch adaptor. These drawings are appended in Figure 2, Figure 3, Figure 4, and Figure 5. The pin assignment of the hybrid connector is listed in Table 1, and the components in Table 2. Details of the hybrid design can be obtained from the web page, http://ccint1.kek.jp/People/kondo/scf/.

II. MOD0 FABRICATION
In the Mod0 fabrication, we did the following.

A. ASIC gluing:
1. Silver-loaded conductive epoxy. We think the conductive epoxy is important although the backside of the chips is not metalized. Glue full area. We use a room-temperature curing one and do post-curing at 50 °C for 2 hrs. The viscosity is relatively low. The epoxy is made by a domestic company.

B. wire-bondings
1. GND (D-, A-, ring-a, det-,...), Vcc, Vdd pads == at least 2 wires per pad if possible,
2. AGND-DGND stitching pads == as many wires as possible, mod0 = 5 wires/pad,
3. Detector bias connections == at least 2 wires per pad. There are four corners of the hybrid which can be used to connect to the detector strip and backplane bias. The strip bias connection is done at four corners. The backplane bias connection is done only on the top side two corners, since the baseboard has only those contacts.

C. Other technical recommendations
1. dry up the hybrid in a low humidity environment (<50% RH) before soldering
2. mask the wire-bonding pads when soldering in order not to contaminate the bonding surface
3. do not burn out the hybrid with a soldering iron. The spec is <10 sec at 260 deg.C. The higher the temperature, the shorter the time (than 10 sec).
4. when wire-bonding, keep in mind that the width of the pads on hybrid, which are mating with the output pads of the chip, is narrow
5. recommend to confirm the performance of the chips before wire-bonding between the chip and the pitch adaptor
6. keep the masking tape on the pitch adaptor until the wire-bondings between the chips and the pitch adaptor will occur.

III. ASIC REPLACEMENT
ASIC replacement has been tested. A jig of
- 8 mm x 8 mm x 12 mm Cu block
- trench of 6.5 mm width and 0.3 mm depth
- the Cu block attached to the tip of a soldering iron
- vacuum line for picking up the chip

was prepared. A photo of the jig is shown in Figure 1.

Figure 1: An IC heating and picking-up jig
Thermo-mechanical measurements

• KEK’s independent measurements
  - In addition to the common effort at RAL
  - A few reminders of the results

• Distortion of the hybrid in the module
  - Before and After (10 thermal cycles)
  - After (20 thermal cycles) was also measured
  - Temperature dependence: \( \sim 0.5 \, \mu m/°C \) sagitta
  - E.g., 20 \( \mu m \) from 20 °C to -20 °C

• Thermal fatigue in the module
  - 7.5 W power on-off in cold (-12 °C cooling water)
  - Before and After 100 cycles
  - No disintegration nor crack
  - No change in the temperature dependence of distortion of module
図 6.12: フルモジュールにしたときのカプトンハイブリッド基板の表側の熱サイクル前後での温度による変形率
Electrical modules

• Barrel module program
  - Proposed to the IB by Mike Tyndel in the Feb SCT week
  - Supported by the majority of the barrel clusters by e-mail correspondence

• “Mod0” to experts in other clusters
  - Sent to the US cluster, Santa Cruz
  - Set in the beamtest in May at CERN

• Identical modules in UK, US, and Nordic clusters
  - Hybrids were sent to the clusters in March
  - Reports from the clusters in this week (?)

• Investigation modules at KEK
  - E-mail correspondences among interested peoples
  - One module was built and tested by the SCT week
Barrel Module Program

- The barrel module program is in a difficult situation because of the limited number of ASICs (& other components available).

- There are a number of open technical issues and options which have not yet come to a mature conclusion. These concern the choice of hybrid technology, the electrical design of the module and assembly & rework issues.

- A special meeting was held of 1 representative/cluster to make a proposal on how best to proceed. There was a divergence of views within this group. Given the limited number of ASICs available & taking into account schedule, financial and political considerations, the following is proposed:

  1. Kapton hybrids are adopted immediately as the baseline technology.

  2. The first KEK Kapton module (Mod-0) is made available as soon as possible to experts within the other clusters to make measurements.

  3. Three more modules, identical to (Mod-0) are manufactured and tested in the UK, USA and Nordic clusters. These four modules will be sent to the system test for measurement.

  4. The stability margin will be investigated by building 3 (Mod-0) variants at KEK using existing variants of the hybrid. The details of what is to be built is to be agreed by the ASIC engineers. Experts from all clusters will participate in the measurement and understanding of these variants.

  5. In view of the potential benefits to be gained from the thin film hybrid, 2 modules are to be built.

  6. A detailed review of all measurements will be held in the May SCT week.

  7. Finally, it is anticipated that a final prototype hybrid will need to be designed and manufactured and 4 modules built by end 2000.
Mod0

• To remind you...

- This is an example of “stable” module
- Stable even after trimming: Trimmed at 2 fC = 200 mV

• S-curves

- Edge=off, Comp=X1X
- “Summed” displays
- Individual all channels per chip and cal lines
- All “clean”

• Trim characteristics

- Rather good (compared with the “End of March” distribution): 32 untrimmable channels
- Mod0 chip: wafer 30423
- Uniformity at trim threshold: 2.67 (front 6 chips) and 2.76 mV (back 6 chips), i.e., <3 mV
Module 0 Link 0 Run 236 Scan 1 - THRESHOLD (mV) from 30.00mV to 200.00mV in 5.00mV steps, total 35 points

scurves cal0

scurves cal1

scurves cal2

scurves cal3

Chip 0

Chip 1

Chip 2

Chip 3

Chip 4

Chip 5
Module 0 Link 1 Run 238 Scan 1 - THRESHOLD (mV) from 30.00mV to 200.00mV in 5.00mV steps, total 35 points

scurves cal0

scurves cal1

scurves cal2

scurves cal3
Target value to be 200 mV
This gives 1504 trimmable channels
ATLAS SCT Module Test
Run 238  Scan 4  Module 0  Stream 0  Scan type: THRESHOLD (mV)

Module 0  Stream 0 THRESHOLD (mV) Scan

Mean (mean) = 200.08, Sigma (mean) = 2.67, Nentries = 766

Fitted Sigma

Mean (sigma) = 13.24, Sigma (sigma) = 1.09, Nentries = 766

Chisq/NDF

Mean = 199.63
Sigma = 13.59
Max Eff. = 1.00

Efficiency, chip 0

Mean = 199.24
Sigma = 13.69
Max Eff. = 1.00

Efficiency, chip 1

Mean = 199.85
Sigma = 13.37
Max Eff. = 1.00

Efficiency, chip 2

Mean = 199.60
Sigma = 12.83
Max Eff. = 0.99

Efficiency, chip 3

Mean = 199.77
Sigma = 13.35
Max Eff. = 1.00

Efficiency, chip 4

Mean = 199.27
Sigma = 14.42
Max Eff. = 1.00

Efficiency, chip 5
ATLAS SCT Module Test
ATLAS SCT Module Test
Run 236 Trim Scans Module 0 Link 1

Target value to be 200 mV
This gives 1504 trimmable channels

TrimDAC characteristics, chip 6
TrimDAC characteristics, chip 7
TrimDAC characteristics, chip 8
TrimDAC characteristics, chip 9
TrimDAC characteristics, chip 10
TrimDAC characteristics, chip 11

Trim Setting - Trimmable Channels
h_tr
Nent = 746

Trim Setting - Untrimmable Channels
h_utr
Nent = 22
<table>
<thead>
<tr>
<th>Module name</th>
<th>k3104mod</th>
<th>k3103</th>
</tr>
</thead>
<tbody>
<tr>
<td>Strip sensors:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Top</td>
<td>ATLAS98 narrow-m</td>
<td>285 um</td>
</tr>
<tr>
<td>Bottom</td>
<td>ATLAS98 wide-poly</td>
<td>285 um</td>
</tr>
<tr>
<td>Baseboard id.</td>
<td></td>
<td>???</td>
</tr>
<tr>
<td>ASICs:</td>
<td>Type</td>
<td>Lot</td>
</tr>
<tr>
<td>M0-E13</td>
<td>ABCD2T</td>
<td>30423</td>
</tr>
<tr>
<td>Hybrid:</td>
<td>Substrate</td>
<td>Substrate Surface finish</td>
</tr>
<tr>
<td>Kapton</td>
<td>ABCD v3</td>
<td>Carbon-carbon</td>
</tr>
<tr>
<td>Capacitors:</td>
<td>C [nF]</td>
<td>Type</td>
</tr>
<tr>
<td>Vcc, Vdd</td>
<td>100</td>
<td>GRM39-X7R-104-K-25</td>
</tr>
<tr>
<td>Common Vcc, Vdd</td>
<td>330</td>
<td>GRM42-6-X7R-334-K-25</td>
</tr>
<tr>
<td>HV decoupling</td>
<td>10</td>
<td>GHM1530-B-103-K-630</td>
</tr>
<tr>
<td>HV connections:</td>
<td>No. locations</td>
<td>No. bonds/location</td>
</tr>
<tr>
<td>Strip</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>Backplane</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>AGND-DGND connections:</td>
<td>14</td>
<td>5</td>
</tr>
<tr>
<td>Bias [V]</td>
<td>Leak current [uA]:</td>
<td>Env. temp [deg.C]</td>
</tr>
<tr>
<td>100</td>
<td>~0.8?</td>
<td>18?</td>
</tr>
<tr>
<td>ASIC currents [A]:</td>
<td>V(sense) [V]</td>
<td>Vth&gt;offset+200 mV</td>
</tr>
<tr>
<td>Vcc</td>
<td>3.5</td>
<td>0.92</td>
</tr>
<tr>
<td>Vdd</td>
<td>4</td>
<td>0.48</td>
</tr>
<tr>
<td>Trimming:</td>
<td>Chage [fC]</td>
<td>Threshold [mV]</td>
</tr>
<tr>
<td>2</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>Threshold uniformity [mV] at trim threshold</td>
<td>Edge=off</td>
<td>Edge=on</td>
</tr>
<tr>
<td>link0</td>
<td>link1</td>
<td>link0</td>
</tr>
<tr>
<td>Offset threshold [mV]:</td>
<td>Edge=off</td>
<td>(2~8fC, 2nd-poly)</td>
</tr>
<tr>
<td>Chips</td>
<td>Vt50</td>
<td>Intercept</td>
</tr>
<tr>
<td>link0 average</td>
<td>102.4</td>
<td>81.8</td>
</tr>
<tr>
<td>link1 average</td>
<td>104.8</td>
<td>83.2</td>
</tr>
<tr>
<td>Gain (@2fC) [mV/fC]:</td>
<td>Edge=off</td>
<td>Edge=on</td>
</tr>
<tr>
<td>Chips</td>
<td>Linear(0,2,3fC)</td>
<td>2nd poly(2~8fC)</td>
</tr>
<tr>
<td>link0 average</td>
<td>50.4</td>
<td>55.8</td>
</tr>
<tr>
<td>link1 average</td>
<td>49.3</td>
<td>55</td>
</tr>
<tr>
<td>Noise (@2fC) [e]:</td>
<td>Edge=off</td>
<td>Edge=on</td>
</tr>
<tr>
<td>Chips</td>
<td>Linear(0,2,3fC)</td>
<td>2nd poly(2~8fC)</td>
</tr>
<tr>
<td>link0 average</td>
<td>1590</td>
<td>1437</td>
</tr>
<tr>
<td>link1 average</td>
<td>1637</td>
<td>1465</td>
</tr>
<tr>
<td>Instability thresholds:</td>
<td>Edge=off</td>
<td>Edge=on</td>
</tr>
<tr>
<td>Chips</td>
<td>Lower [mV]</td>
<td>Upper [mV]</td>
</tr>
<tr>
<td>link0</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>link1</td>
<td>none</td>
<td>none</td>
</tr>
</tbody>
</table>
k3111

- First of the 3 “investigation” modules at KEK

- After correspondences regarding the “investigation” modules,
  
  - Same latest hybrid version, i.e., version 3
  - No “meshed ground” variant was available for the version
  
  - “Split ground” version was recommended, leaving options how tightly connect the AGND and DGND
  
  - Leaving only a choice on the bridge material
  
  - Polymer-coated Carbon-carbon bridge, Insulated surface in increasing the resistivity of bridge
  
  - Electrical contact to the carbon-carbon through openings on the insulator at the chip pads
k3111 cont’d

• ABCD2T chips
  - Wafer 29476
  - Greater variation in the trim stage

• Trim characteristics
  - Trim at 2 fC=200 mV, leaving 75 untrimmable channels
  - Threshold uniformity: 2.94 (Front 6) and 2.91 (Back 6) mV, i.e., <3 mV

• Stability
  - Noise scan with Edge=on, Comp=01X
  - Stable, no global instability
  
  - Noise scan with Edge=off, Comp=X1X
  - Clean, no difference in upward or downward noise scans
  
  - Individual s-curves: clean, but
  
  - Chip5 (E5) of front 6 had “discontinuity” in the curves, similarly Chip4 (S12) of back 6 had “discontinuity”
Target value to be 200 mV
This gives 1461 trimmable channels

TrimDAC characteristics, chip 0

TrimDAC characteristics, chip 1

TrimDAC characteristics, chip 2

TrimDAC characteristics, chip 3

TrimDAC characteristics, chip 4

TrimDAC characteristics, chip 5

Trim Settling - Trimmable Channels

Trim DAC value

50%-points (mV)

Nent = 730

Trim Settling - Untrimmable Channels

Trim DAC value

50%-points (mV)

Nent = 38
Target value to be 200 mV
This gives 1461 trimmable channels
ATLAS SCT Module Test - Thu May 18 14:17:31 2000
Run 1442 Scan 12 Module 0 Stream 0 Scan type: THRESHOLD (mV)

Module 0 Stream 0 THRESHOLD (mV) Scan

Efficiency, chip 0

Efficiency, chip 1

Efficiency, chip 2

Efficiency, chip 3

Efficiency, chip 4

Efficiency, chip 5

Mean (mean) = 199.67, Sigma (mean) = 2.94, Nentries = 762

Mean (sigma) = 13.33, Sigma (sigma) = 0.97, Nentries = 762

Chisq/NDF
Module 0 Link 1 Run 1438 Scan 2 - THRESHOLD (mV) from 0.00mV to 200.00mV in 2.50mV steps, total 81 points
ATLAS SCT Module Response Curve - ABCD2T - Polynomial fit

Run 1476   Scans 12 - 37   Charges 2.00 - 8.00 fC   Module 0   Stream 0

Response Curve chip 0

Response Curve chip 1

Response Curve chip 2

Gain chip 0

Gain chip 1

Gain chip 2

Response Curve chip 3

Response Curve chip 4

Response Curve chip 5

Input Noise chip 0

Input Noise chip 1

Input Noise chip 2

Output Noise chip 3

Output Noise chip 4

Output Noise chip 5

Input Noise chip 3

Input Noise chip 4

Input Noise chip 5
k3111 cont’d

• “Offset” (or I call “Noise pedestal”)

(1) 50% point of s-curves with Edge=off
(2) Peak with Edge=on
(3) Intercept from the high threshold scans, 2 ~ 8 fC, with 2nd order polynomial fit, with Edge=off

(1) 91 mV, 87 mV, link average, i.e., front 6 and back 6
(2) 92 mV, 88 mV
(3) 81 mV, 80 mV

• Gain and noise (at 2 fC threshold)

(1) Linear fit of 0, 2, 3 fC threshold scans, Edge=off
(2) 2nd-order polynomial fit to high thresholds, 2~8 fC, Edge=off
(3) ditto, but Edge=on

- Gain per (1), (2), (3) ~54, ~55, ~65 mV/fC
- Input noise ~1430, ~1384, ~1240 e

- Why the gains differed in (2) and (3)?
- The responses were different in higher threshold with Edge=off and on. Why?
Summary sheet

- One sheet summary of critical items
<table>
<thead>
<tr>
<th>Module name</th>
<th>k3111</th>
<th>k3111</th>
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### Strip sensors:

<table>
<thead>
<tr>
<th>Type</th>
<th>Thickness [um]</th>
<th>Vendor</th>
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<tbody>
<tr>
<td>Top ATLAS98 narrow-m</td>
<td>285 um</td>
<td>Hamamatsu</td>
</tr>
<tr>
<td>Bottom ATLAS98 narrow-m</td>
<td>285 um</td>
<td>Hamamatsu</td>
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</table>

### Baseboard id.

| ?? |

### ASICs:

<table>
<thead>
<tr>
<th>Type</th>
<th>Batch</th>
<th>Wafer</th>
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</thead>
<tbody>
<tr>
<td>M0-E13</td>
<td>ABCD2T</td>
<td>29476</td>
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</table>

### Hybrid:

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Substrate Surface finish</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kapton</td>
<td>Carbon-carbon polymer-coated</td>
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</tbody>
</table>

### Capacitors:

<table>
<thead>
<tr>
<th>C [nF]</th>
<th>Type</th>
<th>Reso freq [MHz]</th>
<th>Vendor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc, Vdd</td>
<td>100</td>
<td>GRM39-X7R-104-K-25</td>
<td>~26</td>
</tr>
<tr>
<td>Common Vcc, Vdd</td>
<td>330</td>
<td>GRM42-6-X7R-334-K-25</td>
<td>~15</td>
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<tr>
<td>HV decoupling</td>
<td>10</td>
<td>GHM1530-B-103-K-630</td>
<td>~70</td>
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### HV connections:

<table>
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<th>No. locations</th>
<th>No. bonds/location</th>
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</thead>
<tbody>
<tr>
<td>Strip</td>
<td>4</td>
</tr>
<tr>
<td>Backplane</td>
<td>2</td>
</tr>
<tr>
<td>AGND-DGND connections:</td>
<td>14</td>
</tr>
</tbody>
</table>

### Bias [V]

<table>
<thead>
<tr>
<th>Leakage current [uA]</th>
<th>Env. temp [deg.C]</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>~0.8</td>
<td>18</td>
</tr>
</tbody>
</table>

### ASIC currents [A]:

<table>
<thead>
<tr>
<th>V(sense) [V]</th>
<th>Vth&gt;offset+200 mV</th>
<th>Vth=offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
<td>3.5</td>
<td>0.89</td>
</tr>
<tr>
<td>Vdd</td>
<td>4</td>
<td>0.47</td>
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### Trimming:

<table>
<thead>
<tr>
<th>Charge [fC]</th>
<th>Threshold [mV]</th>
<th>Trimamble ch</th>
<th>Untrimmable ch</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>200</td>
<td>1461</td>
<td>75</td>
</tr>
</tbody>
</table>

### Threshold uniformity [mV]:

<table>
<thead>
<tr>
<th>Edge=off</th>
<th>Edge=on</th>
</tr>
</thead>
<tbody>
<tr>
<td>link0</td>
<td>2.94</td>
</tr>
<tr>
<td>link1</td>
<td>2.91</td>
</tr>
</tbody>
</table>

### Offset threshold [mV]:

<table>
<thead>
<tr>
<th>Edge=off</th>
<th>(2~8fC, 2nd-poly)</th>
<th>Edge=on</th>
<th>(2~8fC, 2nd-poly)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chips</td>
<td>Vt50</td>
<td>Intercept</td>
<td>Peak</td>
</tr>
<tr>
<td>link0 average</td>
<td>91.3</td>
<td>80.5</td>
<td>91.6</td>
</tr>
<tr>
<td>link1 average</td>
<td>87.1</td>
<td>80.1</td>
<td>87.9</td>
</tr>
</tbody>
</table>

### Gain (@2fC) [mV/fC]:

<table>
<thead>
<tr>
<th>Edge=off</th>
<th>Edge=on</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chips</td>
<td>Linear(0,2,3fC)</td>
</tr>
<tr>
<td>link0 average</td>
<td>53.1</td>
</tr>
<tr>
<td>link1 average</td>
<td>54</td>
</tr>
</tbody>
</table>

### Noise (@2fC) [e]:

<table>
<thead>
<tr>
<th>Edge=off</th>
<th>Edge=on</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chips</td>
<td>Linear(0,2,3fC)</td>
</tr>
<tr>
<td>link0 average</td>
<td>1437</td>
</tr>
<tr>
<td>link1 average</td>
<td>1409</td>
</tr>
</tbody>
</table>

### Instability thresholds:

<table>
<thead>
<tr>
<th>Edge=off</th>
<th>Edge=on</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chips</td>
<td>Lower [mV]</td>
</tr>
<tr>
<td>link0 E5</td>
<td>77.5</td>
</tr>
<tr>
<td>link1 S12</td>
<td>77.5</td>
</tr>
</tbody>
</table>
Timewalk

• Measured at
  - Threshold = 1fC
  - Strobe delay scan for the calibration charges of 1.5, 2.0, 4.0, 6.0, 8.0, 16.0 fC

  - Extract the strobe time of 50% efficiency
  - (No fundamental reason to take the 50% point, just a technical easiness to extract a timing)

• Reasonable fit with “inverse square root” function

  - $f(q) = p_0 + \frac{p_1}{\sqrt{q - p_2}}$

  - In average,
    - $p_1 \sim 10 \text{ ns}$
    - $p_2 \sim 1 \text{ fC}$

  - What does this mean?
Story of “Mod2”

• Mod2 was built at the same time of Mod0, however,

• It was built with temporary sensor-baseboard
  - Due to the lack of the same TPG baseboard as of Mod0, used early prototype TPG baseboard (with AlN facings)
  - Replacing the sensor-baseboard unit in future, in mind, used ATLAS97 design sensors
  - Hybrid was “screwed” on to the baseboard, instead of gluing, to be able to dismounted

• The module performed inferior to the Mod0
  - Larger leakage current of a few mA at around 100 V, not too large but significantly larger than that of Mod0 of <1 mA
  - One chips was sick in trimming, an order larger trim step
  - And, showed global instability on one of the 6 chip hybrid, when Edge=on, depending on the location of the backplane bias connection
Story of Mod2 cont’d

• In the struggling in trying to identify the source of instability,
  
  - One chip died, due to insufficient cooling when the hybrid was probed

  - Sensor leakage current increased, time by time, to about 40 $\mu$A around 100 V at the end

  - The trim-sick chip was replaced, did not cure the problem

• After these poor conditions, Mod2 was sent to major surgery, dismounting the hybrid and building into a new module with a latest sensor-baseboard assembly

  - Gambled to use one of the 3 latest TPG baseboards
  - ATLAS98 sensors
  - Replacing the dead chip; in total 3 chips were replaced, one sick chip, one dead chip, and one normal chip because of mistake (located the wrong “sick chip”)

Y. Unno 1/6/0
Return of “Mod2mod”

- After the surgery, named as “Mod2 modified”, or “Mod2mod”, returned on Friday last week, and the module was

   REVIVED!!

- No sign of instability, as stable as Mod0

  - Noise scans with Edge=on, off

  - S-curves, no hint of instability nor “discontinuity”

  - Trim characteristics was as good as Mod0 (of course, the same wafer, 32423

  - Due to repeating the trim scan for the module, the measurements were done with the trim file of hybrid, trim at 2 fC= 200 mV
Target value to be 200 mV
This gives 1518 trimmable channels

TrimDAC characteristics, chip 0

TrimDAC characteristics, chip 1

TrimDAC characteristics, chip 2

TrimDAC characteristics, chip 3

TrimDAC characteristics, chip 4

TrimDAC characteristics, chip 5

Trim DAC value

50%-points (mV)

Target value (mV)

Trim DAC value

50%-points (mV)

Trim DAC value

50%-points (mV)

Trim DAC value

50%-points (mV)

Trim DAC value

50%-points (mV)
ATLAS SCT Module Test
Run 1407 Trim Scans Module 0 Link 1

Target value to be 200 mV
This gives 1518 trimmable channels

TrimDAC characteristics, chip 6
TrimDAC characteristics, chip 7
TrimDAC characteristics, chip 8
TrimDAC characteristics, chip 9
TrimDAC characteristics, chip 10
TrimDAC characteristics, chip 11

Trim Setting - Trimmable Channels
Trim Setting - Untrimmable Channels
ATLAS SCT Scan Comparison - log scale
Run 1490  Scan 1  Module 0  Stream 0 (Projection of ch 0 to ch 767) vs
Run 1490  Scan 1  Module 0  Stream 1 (Projection of ch 0 to ch 767)

Module 0  Stream 0 THRESHOLD (mV) Scan

Module 0  Stream 1 THRESHOLD (mV) Scan

Constant = 177.5 ± 5.199
Mean = 100.4 ± 0.2451
Sigma = 10.46 ± 0.1907

Constant = 175.4 ± 4.88
Mean = 102.5 ± 0.2612
Sigma = 11.69 ± 0.2019
ATLAS SCT Scan Comparison - log scale
Run 1490  Scan 3  Module 0  Stream 0 (Projection of ch 0 to ch 767) vs
Run 1490  Scan 3  Module 0  Stream 1 (Projection of ch 0 to ch 767)
Module 0 Link 0 Run 1490 Scan 3 - THRESHOLD (mV) from 0.00mV to 250.00mV in 2.50mV steps, total 101 points
Module 0 Link 1 Run 1490 Scan 3 - THRESHOLD (mV) from 0.00mV to 250.00mV in 2.50mV steps, total 101 points
ATLAS SCT Module Response Curve - ABCD2T - Linear fit
Run 1493 Scans 3 - 18 Charges 0.00 - 3.00 fC Module 0 Stream 0

Gain chip 0
Gain chip 1
Gain chip 2
Gain chip 3
Gain chip 4
Gain chip 5

Output Noise chip 0
Output Noise chip 1
Output Noise chip 2
Output Noise chip 3
Output Noise chip 4
Output Noise chip 5

Input Noise chip 0
Input Noise chip 1
Input Noise chip 2
Input Noise chip 3
Input Noise chip 4
Input Noise chip 5
ATLAS SCT Module Response Curve - ABCD2T - Polynomial fit
Run 1493  Scans 12 - 37  Charges 2.00 - 8.00 fC  Module 0  Stream 0
Mod2mod

• Offset (Noise pedestal)

(1) 50% point with Edge=off 102, 104 mV
(2) Peak with Edge=on 100, 103 mV
(3) Intercept of 2nd-order poly with Edge=off91, 98 mV
(4) Intercept of 2nd-order poly with Edge=on76, 79 mV

• Gain and noise (at 2 fC)

(1) Linear fit at 0, 2, 3 fC with Edge=off
(2) 2nd-order poly (2~8 fC) with Edge=off
(3) 2nd-order poly (2~8 fC) with Edge=on

- Gains ~54, ~51, ~60 mV/fC
- Input noises ~1420, ~1520, ~1360 e

- These were consistent with Mod0, but differed from k3111
<table>
<thead>
<tr>
<th>Module name</th>
<th>k3104mod</th>
<th>k3104mod</th>
</tr>
</thead>
<tbody>
<tr>
<td>Strip sensors:</td>
<td>Type</td>
<td>Thickness [um]</td>
</tr>
<tr>
<td>Top</td>
<td>ATLAS98 narrow-m</td>
<td>285 um</td>
</tr>
<tr>
<td>Bottom</td>
<td>ATLAS98 wide-poly</td>
<td>285 um</td>
</tr>
<tr>
<td>Baseboard id.</td>
<td>???</td>
<td></td>
</tr>
<tr>
<td>ASICs:</td>
<td>Type</td>
<td>Batch</td>
</tr>
<tr>
<td>M0-E13</td>
<td>ABCD2T</td>
<td>30423</td>
</tr>
<tr>
<td>Hybrid:</td>
<td>Substrate</td>
<td>Substrate Surface finish</td>
</tr>
<tr>
<td>Kapton</td>
<td>ABCD v3</td>
<td>Carbon-carbon</td>
</tr>
<tr>
<td>Capacitors:</td>
<td>C [nF]</td>
<td>Type</td>
</tr>
<tr>
<td>Vcc, Vdd</td>
<td>100</td>
<td>GRM39-X7R-104-K-25</td>
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<tr>
<td>Common Vcc, Vdd</td>
<td>330</td>
<td>GRM42-6-X7R-334-K-25</td>
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<td>HV decoupling</td>
<td>10</td>
<td>GHM1530-B-103-K-630</td>
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<tr>
<td>HV connections:</td>
<td>No. locations</td>
<td>No. bonds/location</td>
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<tr>
<td>Strip</td>
<td>4</td>
<td>2</td>
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<tr>
<td>Backplane</td>
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<tr>
<td>AGnd-DGND connections:</td>
<td>14</td>
<td>5</td>
</tr>
<tr>
<td>Bias [V]</td>
<td>Leak current [uA]</td>
<td>Env. temp [deg.C]</td>
</tr>
<tr>
<td>100</td>
<td>~0.8</td>
<td>18</td>
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<tr>
<td>ASIC currents [A]:</td>
<td>V(sense) [V]</td>
<td>Vth&gt;offset+200 mV</td>
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<tr>
<td>Vcc</td>
<td>3.5</td>
<td>0.93</td>
</tr>
<tr>
<td>Vdd</td>
<td>4</td>
<td>0.5</td>
</tr>
<tr>
<td>Trimming:</td>
<td>Chage [fC]</td>
<td>Threshold [mV]</td>
</tr>
<tr>
<td>(using hybrid data)</td>
<td>2</td>
<td>200</td>
</tr>
<tr>
<td>Threshold uniformity [mV]</td>
<td>Edge=off</td>
<td>link0</td>
</tr>
<tr>
<td>at trim threshold</td>
<td>3.47</td>
<td>3.33</td>
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<tr>
<td>Offset threshold [mV]:</td>
<td>Edge=off</td>
<td>(2~8fC, 2nd-poly)</td>
</tr>
<tr>
<td>Chips</td>
<td>Vt50</td>
<td>Intercept</td>
</tr>
<tr>
<td>link0 average</td>
<td>102.2</td>
<td>91.4</td>
</tr>
<tr>
<td>link1 average</td>
<td>104</td>
<td>98.3</td>
</tr>
<tr>
<td>Gain (@2fC) [mV/fC]:</td>
<td>Edge=off</td>
<td>Linear(0,2,3fC)</td>
</tr>
<tr>
<td>Chips</td>
<td>link0 average</td>
<td>53.1</td>
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<tr>
<td>link1 average</td>
<td>54</td>
<td>49.6</td>
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<tr>
<td>Noise (@2fC) [e]:</td>
<td>Edge=off</td>
<td>Linear(0,2,3fC)</td>
</tr>
<tr>
<td>Chips</td>
<td>link0 average</td>
<td>1437</td>
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<tr>
<td>link1 average</td>
<td>1409</td>
<td>1557</td>
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<tr>
<td>Instability thresholds:</td>
<td>Edge=off</td>
<td>Lower [mV]</td>
</tr>
<tr>
<td>Chips</td>
<td>link0</td>
<td>none</td>
</tr>
<tr>
<td>link1</td>
<td>none</td>
<td>none</td>
</tr>
</tbody>
</table>
Summary

• All three modules built at KEK are now all stable
  - Mod0, Mod2mod -- ABCD2T wafer 30423
  - k3111 -- ABCD2T wafer 27496

• ABCD2T wafers, 30423 and 27496, showed different performance in module
  - 27496 chips were more sensitive to instability, or ???
  - Although small and evident in 12 cm strips and 12 chips, the “discontinuity” looked similar behaviour in the ABCD1

• We have more statistics, and looking forward to the discussion of differences in the summary sheets