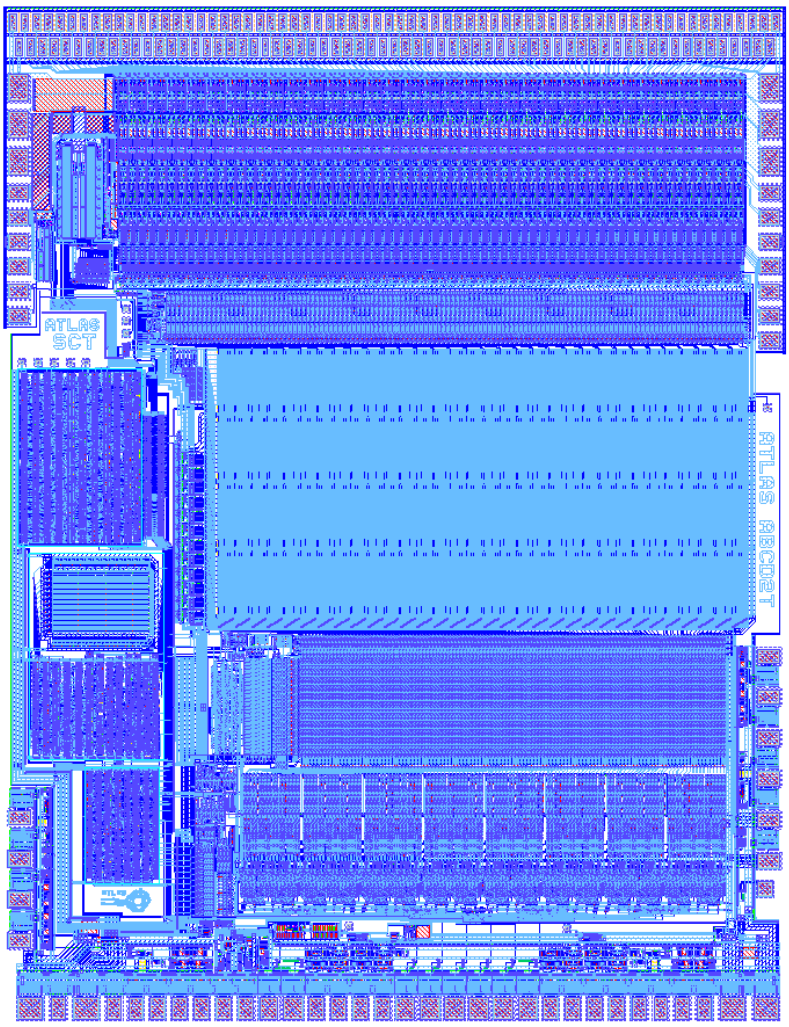
ABCD3T specification



3.2.26 Physical Requirements

The die size of the ABCD3T chip is 6550 μm x 8400 μm.

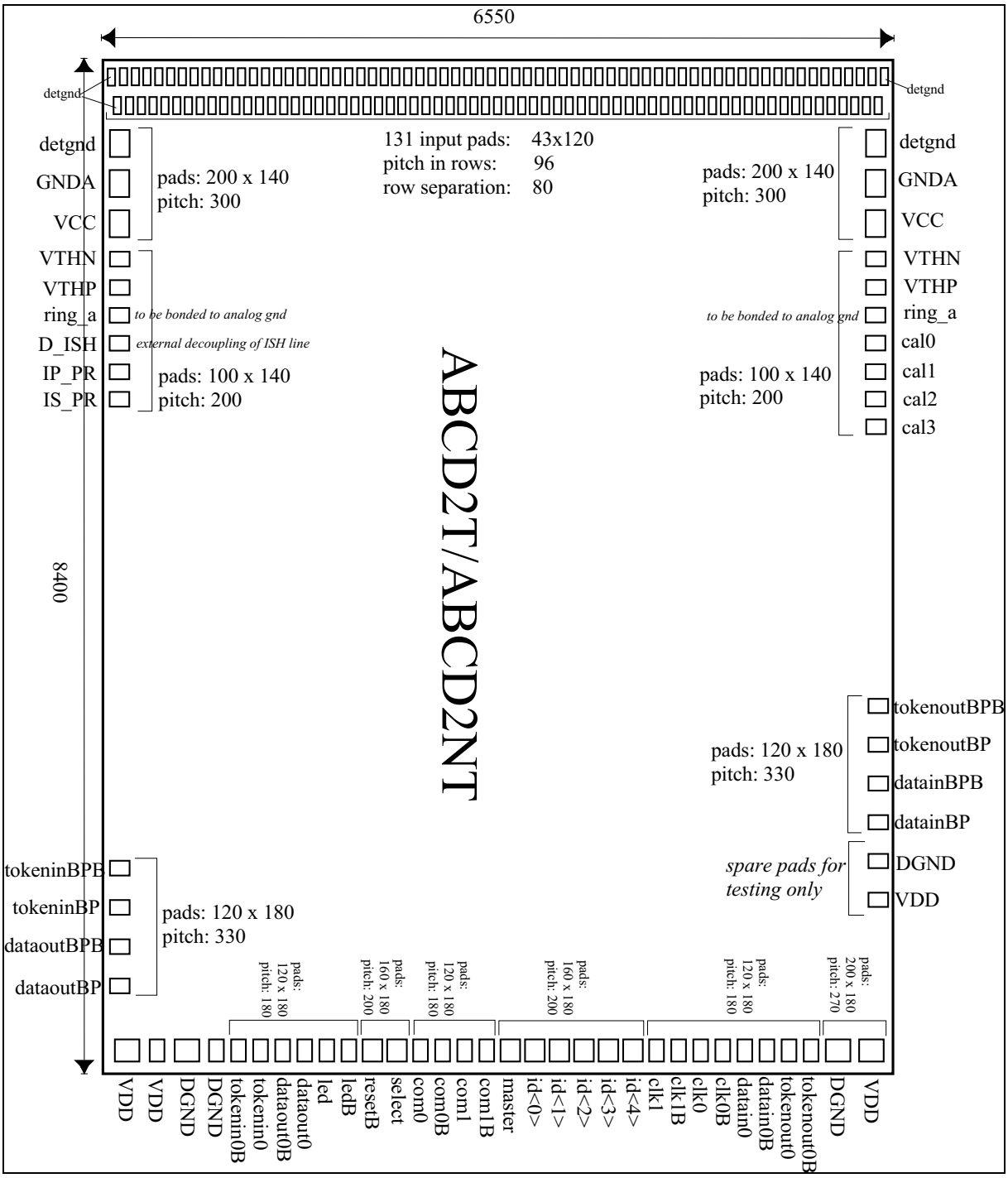


Figure 3.19. ABCD3T Pad Layout

3. TECHNICAL ASPECTS

3.1 Requirements

3.1.1 General

The chip must provide all functions required for processing of signal from 128 strips of a silicon strip detector in the ATLAS experiment employing the binary readout architecture. The simplified block diagram of the chip is shown in figure 3.1. The main functional blocks are: front-end, input register, pipeline, derandomizing buffer, command decoder, readout logic, threshold&calibration control.

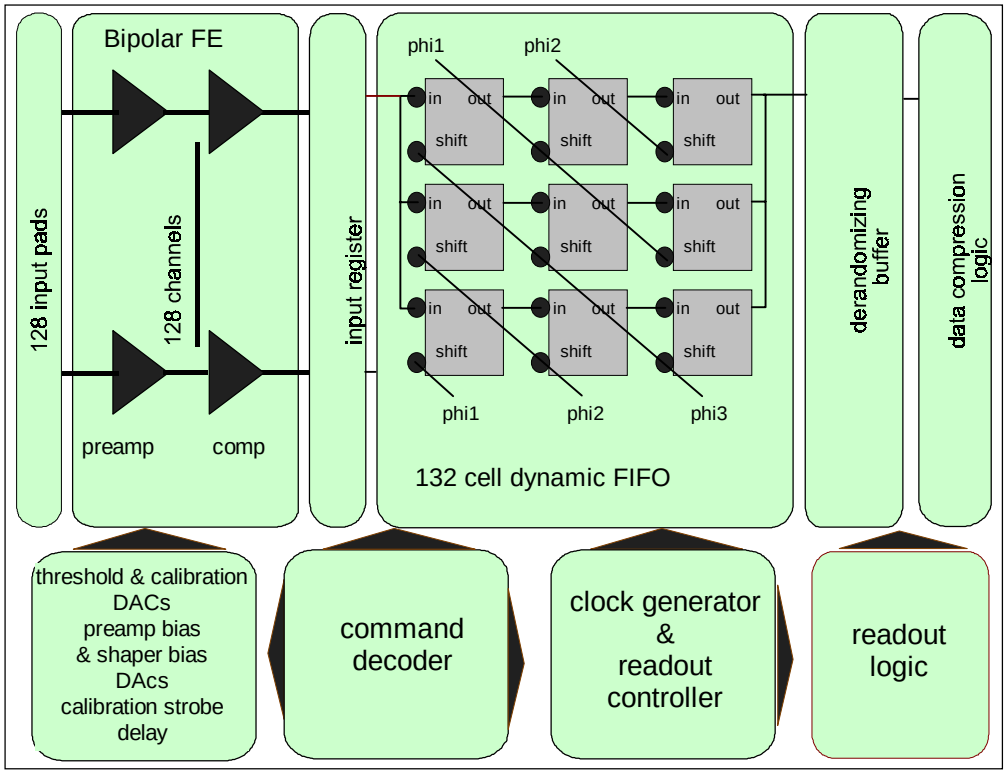


Figure 3.1. Block diagram of the ABCD chip.

3.1.2 Signal processing.

The chip must contain following functions:

1. Charge integration
2. Pulse shaping
3. Amplitude discrimination. The threshold value for the amplitude discrimination is provided as a differential voltage either from internal programmable DAC or from an external source.
4. The outputs of the discriminators must be latched either in the edge sensing mode or in the level sensing mode.
5. At the start of each clock cycle the chip must sample the outputs from the discriminators and store these values in a pipeline until a decision can be made whether to keep the data.
6. Upon receipt of a L1 Trigger signal the corresponding set of values together with it's neighbours are to be copied into the readout buffer serving as a derandomizing buffer.
7. The data written into the readout buffer is to be compressed before being transmitted off the chip.
8. Transmission of data from the chip will be by means of token passing and must be compatible with the ATLAS protocol.
9. The chip is required to provide reporting of some of the errors that occur:
    a) Attempt to read out data from the chip when no data is available.

b) Readout Buffer Overflow: The readout buffer is full and data from the oldest event(s) has been overwritten.

c) Readout Buffer Error: The readout buffer is no longer able to keep track of the data held in it. (Chip reset required).

d) Configuration error (ChipID sent).

10. The chip shall incorporate features that will enable the system to continue operating in the event of a single chip failure.

11. It is a system requirement that the fraction of data which is lost due to the readout buffer on the chip being full is less than 1%. This assumes that on average only 1% of the silicon strip detectors are hit during any particular beam crossing.

3.1.3 Calibration and testability.

Each channel has an internal Calibration Capacitor connected to its input for purposes of simulating a "hit" strip. The Calibration Capacitors are charged by an internal chopper circuit which is triggered by a command. Every fourth channel can be tested simultaneously with group selection determined by two binary coded Calibration Address inputs (CALD0, CALD1). The strobe and the address signals are delivered from the control circuitry. The voltage applied to the Calibration Capacitors by the chopper is determined by an internal DAC. The four calibration bus lines, each of which connects the calibration capacitors of every fourth channel, are also brought out to pads which can be directly driven with an AC coupled voltage step. This is intended for use during IC testing. A tuneable delay of the calibration strobe with respect to the clock phase covering at least two clock periods must be provided. The chip must incorporate such features that will enable to test and calibrate it either on the wafer level or in situ.

3.1.4 Compatibility

The design of the ABCD3T chip must be functionally and electrically compatible with the ABCD2T prototype. It is required that the physical dimesions and the pad layout must be identical with the ABCD2T design.

3.2 Specification

3.2.1 Detector parameters

The parameters of the analogue front-end part are specified for the electrical parameters of 12.8 cm long p-type silicon strip detector. The assumed detector parameters are listed in Table 3.1.

Table 3.1: Assumed detector electrical parameters.

	Unirradiated	Irradiated
Coupling type to amplifier	AC	AC
Coupling capacitance to amp Total for 12 cm strips	20 pF/cm 240 pF	20 pF/cm 240 pF
Capacitance of strip to all neighbour strips	1.03 pF/cm	1.40 pF/cm
Capacitance of strip to backplane	0.30 pF/cm	0.30 pF/cm
Metal strip resistance	15 Ω/cm	15 Ω/cm
Bias Resistor	0.75 MΩ	0.75 MΩ
Max leakage current per strip for shot noise	2.0 nA	2.0 μA
Charge collection time	< 10 ns	< 10 ns

3.2.2 Front-end

3.2.2.1 Electrical Requirements:

Note that notation convention for currents used in the entire specification is "+" for current going into (sunk by) the chip and "-" for current going out of (sourced from) the chip.

3.2.2.2 Input Characteristics:

Input Signal Polarity:	Positive signals from p-type strips.
Crosstalk:	< 5% (via detector interstrip capacitance)
Input Protection:	Must sustain voltage step of 450 V of either polarity with a cumulative charge of 5 nC in 25 ns.
Open Inputs:	Any signal input can be open without affecting performance of other channels.
Max Parasitic Leakage Current:	100 nA DC per channel with < 10 % change in gain at 1 fC input charge.

3.2.2.3 Preamplifier-Shaper Characteristics

Gain at the discriminator input:	50 mV/fC for the nominal shaper current of 20 μA and the nominal process parameters
Linearity:	better than 5% in the range 0 - 4 fC
Peaking time:	20 ns
Noise:	Maximum rms noise for nominal components as measured on fully populated modules
	<= 1500 electrons rms for unirradiated module
	<= 1800 electrons rms for irradiated module

Gain Sensitivity to VCC for 1 fC signal: 1%/100mV

Power Supply Rejection Ratio at:
(not design targets but simulation results of the circuit)

10 Hz - 100 Hz	60 dB
10 kHz - 100 kHz	20 dB
10 MHz - 60 MHz	-14 dB

3.2.2.4 Comparator Stage:

A threshold is applied as a differential voltage offset to the comparator stage. This threshold voltage is applied from an internal DAC in the normal oparation mode or can be applied from the external pads for test purposes.

Threshold setting range:	0 fC to 12.8 fC , nominal setting at 1 fC
Threshold setting step:	0.05 fC of input charge around nominal threshold of 1 fC
Threshold variation at 1 fC:	(1 sigma) channel to channel matching within one chip vs Range Set of TrimDACs by 2 bits in the Configuration Register (See Table 3.1a
	min (00) 2.5%
	x2 (01) 5.0%
	x3 (10) 7.5%
	x4 (11) 10%

3.2.2.5 Timing Requirements:

Timewalk:	<= 16 ns. This specification depends on the precision of the digital acquisition latch edge. Good alignment, 1 or 2 ns over a common clocked array of channels implies a longer timewalk assignment to the rising edge of the shaped signal.
Timewalk defined:	The maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 to 10 fC, with the comparator threshold set to 1 fC.
Double Pulse Resolution:	<= 50 ns for a 3.5 fC signal followed by a 3.5 fC signal

Max recovery time for a 3.5 fC signal following a 80 fC signal: 1 μs

3.2.2.6 Threshold Generation Circuit

Differential voltage for the discriminator threshold is generated by an internal DAC circuit (Threshold DAC). The threshold voltages generated by the internal circuit are applied to the same pads VTHP and VTHN to which the external threshold is applied. When the external threshold is not applied the internal threshold voltage can be measured at pads VTHP and VTHN.

Range:	0 - 640 mV
Step value:	2.5 mV
Absolute accuracy:	1%

3.2.2.7 Calibration Circuit Characteristics

Calibration signal can be applied to one of the four calibration lines via the external pads or from the internal calibration circuit. In the later case the address of the calibration line, the amplitude of the calibration signal and its delay is set via the control logic.

Calibration Capacitors:	100 fF ±20% (3 sigma) over full production skew ±2% (3 sigma) within one chip.		
Calibration signal:			
amplitude range:	0 - 160 mV	(charge range:	0 - 16 fC)
amplitude step:	0.625 mV	(charge step:	0.0625 fC)
Absolute accuracy of amplitude:	5% (full process skew)		
Relative accuracy of amplitude:	< 2 % (for known values of calibration capacitors, amplitude range 0.8 to 4 fC, across one chip, including switching pickup, etc.)		
Relative accuracy of amplitude:	< 10 % (for known values of calibration capacitors, amplitude range 0.8 to 8 fC, across one chip, including switching pickup, etc.)		

Calibration Strobe signal pickup at comparator should be less than 0.1 fC equivalent sensor input.

For test purposes, a voltage step can be applied directly to any one of the four groups of calibration capacitor via the input pads (CAL0, CAL1, CAL2, CAL3). When not used, these four pads must be left floating.

3.2.2.8 Threshold Correction Circuit

In order to compensate channel-to-channel variation of the discriminator offset each channel is provided with a trim DAC of 4-bit resulution. Each channel can be addressed individually and the threshold correction can be applied channel by channel. The range of the trim DAC can be selected with two bits in the configuration register (see Table 3.10b). This is to cover the offset spread which is expected to increase after irradiation.

Range of the trim DAC:	four selectable ranges (see Table 3.1a)
Step value:	see Table 3.1a.
Absolute accuracy:	10%

Table 3.1a: Trim DAC range selection

Trim DAC range Bit 1	**Trim DAC range Bit 0**	**Trim DAC range**	**Trim DAC step**
0	0	0 mV - 60 mV	4 mV
0	1	0mV -120 mV	8 mV
1	0	0mV -180 mV	12 mV
1	1	0mV -240 mV	16 mV

3.2.3.2 Edge Detection Circuitry

The function of this block is to detect a high to low transition in the data entering the pipeline, and for each of such transition found the circuit generates a pulse of duration 1 clock cycle irrespective of the length of the incoming pulse. The effect of this block is that only a single '1' is written into the pipeline for every hit detected regardless of the response time of the discriminator. This circuitry can be turned on or off by setting the appropriate bit in the configuration register.

3.2.6 Data compression logic

It is anticipated that on any event very few channels will contain hits. This fact can be used to reduce the number of bits of data that have to be read out of the chip for each event. The data compression logic works by examining in turn the 3 bits of data that make up the hit pattern for each channel. Each group of 3 bits is compared against one of 4 selectable criteria. If the pattern meets the criteria, then the hit pattern from that channel is sent to the readout circuitry for transmission, if not, no data is sent from that channel and the hit pattern from the next channel is examined. This process is repeated until the hit patterns from all 128 channels have been examined. The following table shows the 4 selection criteria (currently there are only plans to use 3, the 4th is for chip testing only).

Table 3.6a: Data Compression Criteria.

mode(1:0)	**Name of Selection Criteria**	**Hit Pattern (Oldest data bit 1st)**	**Usage**
00	Hit	1XX or X1X or XX1	Detector alignment
01	Level	X1X	Normal Data Taking
10	Edge	01X	Normal Data Taking
11	Test	XXX	Test Mode

N.B. X = Don't care state.

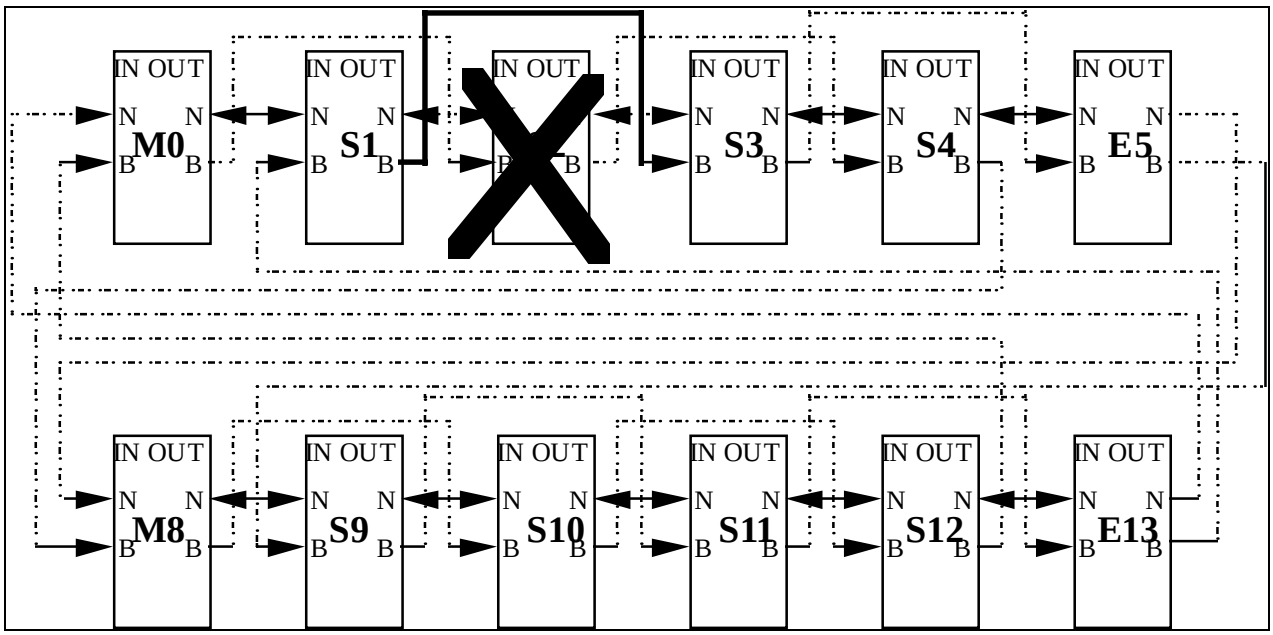


Figure 3.18d. Diagram Showing the flow of Tokens and Data in the event of the failure of a Slave ABCD chip.

Table 3.22a: Input Signals.

Name	**Function**	**Type**
clk0 & clk1	Clock input	LVDS
clk0B & clk1B	Complement of above signal	LVDS
com0 & com1	Command Input	LVDS
com0B & com1B	Complement of above signal	LVDS
tokin0 & tokin1	Token Input	Current Mode
tokin0B & tokin1B	Complement of above signal	Current Mode
din0 & din1	Data Input	Current Mode
din0B & din1B	Complement of above signal	Current Mode
id<5:0>	Geographical address of chip	CMOS
masterB	Sets chip default to master	CMOS
select	Selects clock/command inputs	CMOS
resetB	Resets Chip	CMOS

Table 3.22b: Default settings of CMOS input signals

Name	**Function**	**Default setting**
id<4>	Geographical address of chip	Low, pull-down with 300 kOhm
id<3:0>	Geographical address of chip	High, pull-up with 100 kOhm
masterB	Sets chip default to master	High, pull-up with 100 kOhm
select	Selects clock/command inputs	Low, pull-down with 300 kOhm
resetB	Resets Chip	High, pull-up with 300 kOhm

Table 3.22c: Output Signals.

Name	**Function**	**Type**
tkout0 tkout1	Token Output	Current Mode
tkout0B tkout1B	Complement of above	Current Mode
dout0 dout1	Data Output	Current Mode
dout0B dout1B	Complement of above	Current Mode
ledout	Data Output to LED driver	LVDS
ledoutB	Complement of above	LVDS

3.2.26 DC Supply and Control Characteristics:

Table 3.23: DC supply voltages.

	Pad Name	**Min**	**Nominal**	**Max**	**Absolute Max**
Analogue Supply	VCC	3.3 V	3.5 V	3.7 V	0 to 6.5 V
Analogue Ground	GNDA		0 V		
Input transistor current	set from internal DAC	100 μA	200 μA	300 μA	
Input transistor current monitor	IP_PR	$V_{ip} = I_p$ x 250 Ω			
Shaper current	set from internal DAC	10 μA	15 μA	30 μA	
Shaper current monitor	IS_PR	$V_{is} = I_{sh}$ x 10 kΩ			
Discriminator threshold	VTHP	3.4 V	3.5 V	3.6 V	VCC
Discriminator threshold	VTHN		3.4 V		VCC
(Vthp - Vthn)			0.1 V	0.9 V	0 to 2 V
Digital Supply *	VDD	3.6 V	4.0 V	4.4 V	0 to 6.5 V
Digital Ground	DGND		0 V		

* For the on chip power-up reset to operate correctly the VDD power supply must be ramped up to 90% of its final value in less than 10 ms.

The current draw at each DC input is as follows.

Table 3.24: DC supply currents.

		Min	Nominal	Max
Analogue Supply	VCC		70 mA	
Analogue Ground	GNDA		-70 mA	
Digital Supply*	VDD		35 mA	
Digital Ground	DGND		-35 mA	
Discriminator threshold**	VTHP		30 μA	
Discriminator threshold**	VTHN		30 μA	

*In the Master chip the current draw at VDD power supply will be approximately 50 mA.

** If threshold voltages applied from external pads.

3.2.26.1 Power Consumption

Expected average power consumption for nominal bias power supply voltages and bias currents: 3.0 mW/channel (for the Master chip: 3.5 mW/channel)

3.2.26.2 Input/Output Levels

Table 3.25a: Input Levels for LVDS Inputs (Clock, Control).

Parameter	**Conditions**	**Minimum**	**Maximum**
Input Voltage Range V_i	$V_{gpd} \leq 950mV$	0 mV	2400 mV
InputVoltage Common mode V_{icm}	$V_{gpd} \leq 950mV$	50 mV	2350 mV
Differential high input threshold $+V_{idth}$	$V_{gpd} \leq 950mV$		100 mV
Differential high input threshold $-V_{idth}$	R_{load} =100Ω ±1%	-100 mV	
Threshold hysteresis	(+Vid) - (Vid)	25 mV	
Receiver input impedance		100 kΩ	

N.B. No internal terminating resistor is built into these inputs and consequently an external resistor terminated resistor is required.

Table 3.25b: Input Levels for Token and Data Inputs (Token_in, Data_in).

Parameter	**Minimum**	**Typical**	**Maximum**
Low Level Input Voltage V_{IL}		VDD/2 - 100mV	
High Level Input Voltage V_{IH}		VDD/2 + 100mV	
Receiver input impedance		120 Ω	

Table 3.25c: Output Levels for Token and Data Outputs (Token_Out, Data_out)

Parameter	**Conditions**	**Minimum**	**Typical**	**Maximum**
Output Voltage Low V_{OL}	C_L=50pF R_{load}=125Ω		VDD/2 - 100mV	
Output Voltage High V_{OH}	C_L=50pF R_{load}=125Ω		VDD/2 - 100mV	
Output Differential Voltage	C_L=50pF R_{load}=125Ω		200mV	

Table 3.25d: Output Levels for LED Outputs.

Parameter		**Minimum**	**Maximum**
Output Voltage low V_{OL}	R_{load} =100Ω ±1%	1000 mV	
Output Voltage High V_{OH}	R_{load} =100Ω ±1%		1400 mV
Output offset Voltage	R_{load} =100Ω ±1%	1125 mV	1275 mV
Output Differential Voltage	R_{load} =100Ω ±1%	250 mV	400 mV
Output impedance	I_{load} =2mA to 3mA	40 Ω	280 Ω