		Internal Design Review of the ATLAS SCT Barrel Hybrids	
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REPORT

INTERNAL DESIGN REVIEW

Of the

SCT Barrel Hybrids

This paper is the review report on the internal Design Review (DR) for the barrel hybrids of the ATLAS SCT held at CERN on 22 June 2000.

Prepared by :	***Checked by :***	***Approved by :***
M. Tyndel		**Review Panel**

	for information, you can contact :				

Distribution: SCT

1. Purpose of the Review

The purpose of the internal DR was to critically review the design and specification of the "Cu/polyimide" barrel SCT hybrid before placing the order for a pre-series batch of 60 pieces. The production of the pre-series on a realistic time-scale is seen as a necessary step to demonstrate the viability of the technology for the full production series. The pre-series hybrids will be equipped with the pre-series ABCD3 ASICs and detectors and then used to build 'module-0's.

The background to the review was that prototype "Cu/polyimide" hybrids have already been built into modules and the electrical performance measured. In general the required performance has been demonstrated but there is still not a full understanding of the parameters which determine the electrical stability.

The mechanical properties and thermal performance have been measured on prototypes and one of the aims of the review was to agree the requirements and specifications.

An important goal of this review was to finalise specifications in preparation for the industrial large-scale production and to define the tests to qualify the materials and the process.

Finally, more detailed information on the production method, cost and schedule was requested.

2. Members of the Review Committee

M. Tyndel, Chair
A. Carter
W. Dabrowski
O. Dorholt
A. Grillo
C. Haber
N. Spencer
R. de Oliveira (CERN)

3. Scope of the Review

A critical assessment of the hybrid taking into account electrical, mechanical/ thermal and fabrication issues. In addition quality control, procurement and financial aspects of the project to be considered. The review should address the usual issues listed for an ATLAS FDR/PRR (although the formal review will not be held until after the results of the pre-series are available):

- Are all functional requirements completely and consistently defined and are they satisfactorily met by the proposed design.
- Has the required performance been satisfactorily demonstrated on prototypes.
- Are design risks adequately considered.
- Are the proposed solutions supported by calculations in terms of performance and safety?
- Are material and technological choices adequate, tolerances and clearances reasonable and acceptable?
- Are QA plans for procurement, production and assembly outlined.*
- Are assembly and qualification test procedures defined and understood.*
- Are all integration issues (neighboring elements) satisfactorily covered?
- Are long-term operation and maintenance aspects taken into account.*
- Are procurement plans and schedules feasible, are manpower and space requirements clear.*

*) as far as available

This review should be based on the documentation made available prior to the review. This should generate questions and discussions which will be answered prior and during the review.

4 Agenda

Thursday 22 June morning is reserved for preliminary technical discussions.

Thursday 22 June 2000 at CERN in B40-4-01 (14:00 – 22:00)

1. 14:00 Introduction & goals of the review — M. Tyndel
2. 14:15 Specification of the "Cu/polyimide" circuit — N. Unno
   - Summary of performance results
     - Electrical
     - Mechanical & thermal
     - Irradiation
   - Schematic
   - Electrical layout
   - Thermistors, connectors
   - Fan-ins

   15:00 Discussion & summary

3. 15:30 Specification of the carbon bridges — S. Terada
4. 15:45 Hybrid sub-assembly fabrication — S. Terada

   16:15 Discussion & summary

5. 16:45 Acceptance measurements for hybrid sub-assembly — R. Apsimon

   17:30 Discussion & summary

6. 18:00 Dinner/Breakfast break?

7. 18:45 Production, Schedule & Cost. — N. Unno

   19:15 Discussion & summary

8. 19:45 Overall summary

   22:00 End of video link

5 Available documentation

General background information can be found in the Inner Detector TDR

Documentation is available on the web :

`http://atlas.kek.jp/~unno/si_hybrid.html`

`under ""“Cu/polyimide” hybrid designs:".`

including

1. Summary of electrical performance results(see Jun 00 SCT week?)
2. Summary of mechanical/thermal results(see Sep 99 SCT week?)
3. Specification of the hybrid layout and construction
4. Specification of the carbon-carbon bridge and fan-ins
5. Specification of fabrication process
6. Specification of the ‘qualification of the materials and fabrication process
7. Specification of user acceptance tests for hybrid assemblies
8. Costs and production schedules
9. Thermal FEA of the SCT barrel module ...
10. Summary of electrical performance ...
11. Irradiation tests of flex circuit
12. Radiation length estimation of ...
13. Specification of the carbon bridges
14. Quality assurance of flex circuits ...
15. Hybrid fabrication in the SCT barrel hybrid ...
16. Quality assurance of the SCT barrel ...

6 Reviewers report

General comments:

The reviewers appreciated the work put in by the speakers in preparing the documentation for the review. The comments and conclusion of the reviewers in this report refer specifically to the design presented by N. Unno and his KEK colleagues.

As only a small number of stable, low noise modules have been produced, the aim of the review was to critically examine this design (not to consider possible alternative options) in order to be able to produce a pre-series of 60 hybrids to allow an improved understanding of electrical properties and production issues. The industrial production of the pre-series will answer questions related to the viability of the proposed fabrication method, the QC and QA and allow the validation and optimisation of the cost.

On the electrical design, the reviewers recommendation is to avoid making significant changes from the current design which has separate analogue and digital grounds. A few specific changes are recommended where there was a clear consensus that the change would bring a 'quantifiable' improvement.

The reviewer's report is divided into 4 sections :

(a) Recommendations for specific design changes to be implemented immediately for the next submission of the hybrid.

(b) Recommendations and questions to be answered before the full series production. These should be addressed by the time of the Oct. SCT week in order to allow necessary changes to be implemented.

(c) An additional list of technical concerns raised during the review is included as 'Grey area'. These consist of suggestions aimed at improving the performance but where either the requirement was not well specified or where the experts could not quantify the performance gain.

(d) A list of points to note as they will impact on other elements of the system design.

(a) Specific recommendations for the pre-series60:

1. Reduce the sizes of alignment holes and move either closer to the split between analogue and digital buses or closer to the other vias so as to minimize the resistance of the buses through that region. The aim is to minimise the AGND impedance

2. Rearrange the split between the analogue and digital grounds to ensure that the vias currently on the 'divide' are fully located in the analogue grounds

3. Keep the current 36-pin connector and minimise the number of changes to the current pin assignment. Remove the unused pins. Referring to M. Morrissey's Fig 1. add the following connections on the hybrid side (The motivation is to keep open the option to minimise the power line impedance's and the impedance between the shunt shield and the analog supply).

   pin14 to AGND (to allow up to 4 AGND connections)

   pin13 to VCC

   pin7 to remain unallocated as a potential temperature return line (see below) .

4. Provide a jumper (bond pads) between ID4 and Vdd. As ID4 has a pull-down resistor inside the ABCD no jumper to DGnd is required to set the low state. The jumper between ID4 and Select on the hybrid should also be kept.

5. Ensure that any layout changes do not compromise the HV operation of the hybrid. No issues were identified with the HV circuit which is designed for 500volts except possibly the value of the filter resistor. The detector attachment points are OK.

6. The option should be pursued to increase the values by 2 of the VCC/VDD bypass capacitors in case the large in variations in digital current cause problems. There might also be gains to be realised from choosing capacitors with an optimised frequency response (it was claimed that X5R range has higher values?). Provision should be made for adding extra capacitors if it can be done without compromising the layout. At the same time as the design is submitted the availability of components should be verified and sufficient pieces ordered to avoid possible later delays.

7. Temperature sensing. In order to maximise the sensitivity of the temperature measurement, a separate trace should connect the reference side of both thermistors to DGnd as close to the hybrid connector as possible as outlined in Martin Morrissey's write-up of 16-Jun-2000 and shown in his figure 4. This scheme should be implemented provided it does not compromise the power busses. The sensitivity in mV/deg should be confirmed for the Semitec 10K thermistor at the SCT operating temperature. (It should also be confirmed that it is rad-hard as a fall-back to a Pt1K could change the conclusion)

8. Electrical specification. A number of electrical parameters should be added to the hybrid specification. The nominal values should be taken from the existing hybrids. The line width spec should be used to set the tolerance. This specification needs to be approved by the SCT electronics co-ordinator.

    i. DC Resistance from connector to each chip position for Vcc, Vdd, AGnd, DGnd. This should be listed as Min and Max for each chip position so we can calculate a worst case voltage spread.

    ii. DC resistance, the capacitance to GND, the capacitance to its pair as measured at the connector of each of the following lines These can be quoted as Max only: CLK0/CLK0B, CLK1/CLK1B, COM0/COM0B, COM1/COM1B, LED/LEDB, LEDX/LEDXB, RESET, SELECT (the last two have no pair so there is only one capacitance).

    iii. DC resistance of each of the following lines as well as the capacitance to GND and to its pair as measured at one IC pad. These can be quoted as Max only: the longest Token0/Token0B and Data0/Data0B, the longest Token1/Token1B and Data1/Data1B.

    iv. DC resistance of each of the following lines as measured at the connector. These can be quoted as Max only: Temp1, Temp2.

9. The acceptable variations on widths of fine pitch bond pads should be specified as 125 μm line, 75 μm gap with a tolerance of 25 μm (or agreed with vendors & C. Haber)

10. The acceptable bow and twist on the substrates should be specified as < 75 μm over the length and <50 μm across the width at 25deg C.

11. The fiducials required on the hybrids and fan-ins by the module builders (Ref M. Gibson) and wire-bonders (ref D. Carlton) should be added.

12. The official ATLAS part number should be added.

13. Before submission of the hybrid design the electrical and mechanical interfaces should be approved by the electronics co-ordinator and the barrel project engineer

14. The reviewers strongly emphasise the importance of using the same production techniques for the pre-series as will be used for the final series production.

(b) Recommendations & questions to be answered before series production :

The reviewers recognised the need to proceed rapidly to provide the hybrids for ABCD3T and for Module-0. However a number of questions were raised concerning the full series production. These should be addressed by the time of the Oct. SCT week in order to allow any necessary changes to be implemented.

The points are divided into 3 separate categories –

i) Issues concerning the hybrid-assembly manufacture and long term reliability;
ii) Issues concerned with work at the module assembly sites;
iii) Procurement and cost issues.

i) Hybrid-assembly manufacture and long term reliability

1. The quality control of the "Cu/polyimide flex "/substrate gluing step is a concern. A specific concern is the risk of trapping air bubbles and compromising the wire bonding and thermal performance. The reported problems encountered by D0 (ref Mike Matulik (Matulik@FNAL.gov)) need to be followed up within 2 weeks of the report and if relevant acted on. The reviewers request to be provided with details of how the quality of the gluing will be controlled and assured.

2. The manual soldering of SM components is a concern. Specific concerns are possible damage to the glue interface due to local heating caused by soldering and possible long-term corrosion. In addition there are concerns that there could be a variation in quality depending on the individual carrying out the work. The reviewers request that they be provided with details of how these problems will be identified should they occur.

   The reviewers also recommend that alternatives (e.g. the use of conductive glues to attach surface components) be investigated to see if this brings any advantages (delamination, corrosion, and reproducibility).

3. The long term reliability of the Al wire bonds was raised as a concern during the review. Following the review, more information was supplied by one of the reviewers :

   "Two known effects when Al wire is bonded to and Gold pads:

   1. Wide range temperature cycling (-30C to +100C) can weaken both the wire and the bond by annealing the wire and by forming an intermetallic reaction at the bond foot. Annealing removes damage and defects induced in the wire during the low temperature part of the thermal cycle by recrystallization, and grain growth occurs during the high temperature part of the cycle. The larger grains then reduce the strength and fatigue resistance of the wire.

   2. An intermetallic reaction takes place when two dissimilar metals are directly interfaced and diffuse into each other at different rates, leaving behind a supersaturation of vacancies on the

side of the fast diffusing metal. These vacancies coalesce into voids, known as Kirkendahl voids, which concentrate stress and reduce the fatigue resistance of the bond. The two metals may also react with one another to form one or more intermetallic phases. In the case of Al-Au interfaces the intermetallic formation process is governed by the diffusion of gold into aluminium ,with Au5Al2 forming first followed by AuAl2. These phases, with complex crystal structures are brittle and more susceptible to flexing fatigue damage than the pure metals. This can result in bond failure when the structure is exposed to differential thermal expansion stresses in temperature cycling. The temperature dependence of this effect is governed by the quality of the intial bond, with good bonds being typified as those with the minimum number of grain boundaries, vacancies, and dislocations.

4. Long term ageing and humidity effects related to the use of Al wirebonds to Au/Ni/Cu bond-pads are a concern. The advice from one of the reviewers is that –

   " Corrosive effects of voltaic cell structures can occur at wire-bond junctions or any interface where a current is passed across bi-metal junctions, such as Al-Au/Ni/Cu. It is necessary to ensure that no liquid phase is encountered at the junction. i.e. only the vapour and solid phases of H_2O can exist. 6000ppm of water is the maximum level that can be tolerated at 0C. Empirical evidence is available and gives between hours/days/years as the bond lifetime at such junctions, depending upon the metals concerned and inter-surface details if the 6000ppm condition is violated. With the large temperature excursions foreseen for the SCT it will be difficult to avoid violating the condition especially as there will not be a perfectly sealed enclosure."

   These effects need to be more fully understood and tests done. These tests should be according to some official test procedure as defined for industry/military applications for die bonded to flex circuits. Advice should be sought from potential vendors.

   If an encapsulant is foreseen it should be specified.

   It could be wise to study possible alternative solutions where only Al/Al bond interfaces are needed and see if this eliminates or reduces metallurgical problems.

5. A stiffener may be needed in the area of the connector. Advice should be asked for from the vendor. The reliability needs to be vigorously tested on the pre-series.

6. All the quality assurance tests proposed by R. Apsimon should be made before the launch of full scale production & documented. It should be clarified where the tests will be carried out.

7. The level of testing of individual hybrid-subassemblies after surface mounting and before shipping should be specified in detail

ii) Issues concerned with work at the module assembly sites.

1. The required level of testing of individual hybrid-subassemblies on receipt at module assembly sites should be specified in detail

2. All fixtures needed for assembly after the parts reach the sites (chip attach, bonding etc.) need to be completely specified and drawings provided.

3. All processes which are required before wire-bonding need to be defined (e.g. oven/pump to drive out moisture, solvent cleaning, plasma cleaning)

4. The rework procedure needs to be specified. If this is carried out at assembly sites the design of rework tooling should be provided.

5. The documentation should be made complete. Include all materials used, particularly adhesives and include data sheets and suggested procedures. (Avoid non-universal fonts; make versions of documents for both A4 and US Letter format to avoid missing lines at the bottom on US machines.

iii) Procurement and cost issues.

1. The yield tables need to be updated and compared with recent experience in large-scale experiments (CDF-II, D0, Zeus, Hera-B).

2. An agreement needs to be reached with the procurement group related to tendering procedures. It is ATLAS policy that all components should have a second source.

3. Vendor quotes are required to backup the estimates of manpower costs.

(c) (Grey area) technical concerns :

A list of technical concerns raised during the review is classified as 'Grey area'. These consist of recommendations aimed at improving the performance but where either the requirement was not well specified or where the experts could not quantify the performance gain.

1. The exact design aspect differentiating stable modules from non-stable ones is not known but some experts believe that the amount of metal used in the ground layers of the module hybrid is the most likely cause.

    i. Should the power planes of layer 4 be solid copper rather than meshed. There were divergent views as to whether this would help. New information from the module program could be relevant. The technical feasibility of making such a change should be clarified to understand how much the impedance would change; for a given amount of metal is solid or grid better?.

    ii. Should the analogue ground on layer one, especially in the region nearest the detector contacts under the fan-ins be solid copper rather than mesh. This will lower the AGND impedance. However it will increase the current flow underneath the fan-ins. There is no agreement by the experts as to whether this would be beneficial, neutral or detrimental.

    The reviewers do not recommend making changes to the power/ground planes as the risk vs. benefit of any change could not be established.

2. There was discussion about the bypass connections with two master chips and the fact that the present design does not allow all 12 chips to feed data to one fibre should the other fibre become non-functional. This is basically a limitation of the number of traces that can be run across the full length of the hybrid and the drive capability of the readout chip to drive long lines. The "normal" token and data drivers could have been designed to drive a long line from one side of the hybrid to the other but this would increase the power dissipation of all 12 chips (quantify?). One of the two missing bypass lines could be added which is a much shorter run but this would add 4 traces (0.8mm width) to either layer 2 or 3 going through the wrap-around section. This should not be considered, as adding these 4 traces would reduce the width of the power or ground buses in the wrap-around region.

3. There was discussion about bringing the 4 sense wires (VccSense, VddSense, AGndSense, DGndSense) onto the hybrid to improve the voltage regulation of the module system by allowing the sensing to take place mid-way through the voltage drops across the length of the hybrid. The current draw is not completely stable. Icc is very dependent upon the 4 DAC settings and Idd is dependent upon occupancy and trigger rate. Idd will change by a substantial amount if the clock is lost and then restarted. The reason not to add the sense lines is the trade-off between adding the lines and reducing the width of the power bussing in the pigtail region versus keeping the power bus widths as is.

4. There was discussion on the thermal performance of the hybrid and module. The large temperature difference between the ASICS and the silicon (~23degress) is a concern but as the impact of this high temperature is not currently understood it is not recommended to make any changes. However, the reviewers would urge that the following questions are answered as soon as possible

a) What is the specification on the ASIC operation temperature after irradiation? The ABCD2 is known to have very little margin and this should be investigated for the ABCD3 (where it is not expected to be a problem)

b) What is the correlation between ASIC surface temperature and the average silicon temperature?

c) What is the effect of ASIC temperature on the module run-away point?

(d) Points affecting the System design:

1. It is noted that there is no bypassing or filtering of Reset or Select on the hybrid. Select is a DC control signal and Reset is a quasi-DC control signal. Both are single-ended and therefore prone to provide a pick-up path to the module. Since they can accommodate very slow rise-time signals, filtering is planned to minimize this pick-up. The filtering is planned for the dogleg or PP1 (probably the latter).

2. The Shunt Shield proposed by Ned and shown in tests to reduce possible noise from the cooling pipes by a factor of 100 does not have any connection point to AGnd on the hybrid. Provision needs to be made to make a connection on the dogleg close to the hybrid connector.

3. Temperature sensing. The thermistors will be referenced to DGnd on the hybrid. At the time of the review, the sensitivity of the temperature measurement was estimated to be 120mv/deg (subsequently checked and documented by N. Unno). The variations in Idd will contribute to uncertainty in the temperature measurement.

iii. The specification of the voltage on the FE chips is $\pm$5% of Vcc and Vdd at the chip pads. Originally, this allowance was given to the power supply designers as their regulation specification. All of the variations across the hybrid including variations due to the un-sensed variations due to current variations must be subtracted from this allowance given to the power supply designers. It would be good to see these numbers listed but that requires understanding power dissipation of the ICs.