
Liverpool BeO Forward Hybrid with ABCD2-P

Preliminary Results (with no detector)

Introduction

A Liverpool BeO Forward Hybrid is presently being populated with ABCD2-P (thinned) to one side only. The chips are mounted onto individual Aluminium foil substrates using conductive glue. A wire bond connection can then be made/broken from the foil substrate to either AGND or DGND to see how the chip(s) perform with different backplane connections.

All results presented are with Edge Detect enabled and using Edge Data Compression.
40MHz clock mark-space ratio set to 1:1.
Nominal values of VCC = 3.5V and VDD = 4.0V (measured on hybrid).
Single trigger data collection.

Performance of Single Master Chip as a function of Front-end Bias (AGND + DGND linked to foil substrate)

A threshold scan has been performed (0mV - 600mV) for different values of input charge-injection (1fC - 4fC), this was repeated for a broad range of Front-end bias (184uA - 257.6uA). The mean values for Gain, Threshold and Input Noise (of all 128 channels) is derived from the threshold scans and then plotted as a function of Front-end bias.

* Gain as function of Front-end bias.
* Threshold as function of Front-end bias.
* Input noise as function of Front-end bias.

Whereas the previous ABCD1s had a very narrow operating range w.r.t. the F.E.bias, the ABCD2 has a much wider operating range, the Gain and Threshold
remain virtually constant for F.E.bias in the range of 211.6uA to 257.6uA. The Input noise is different in that it does not stabilise until F.E.bias is
230uA or greater. It is for this reason that the F.E.bias is set to 230uA, which is in close agreement with the design specification of 220.8uA.

Performance of Single Master Chip as a function of Shaper Bias (AGND + DGND linked to foil substrate)

A similar threshold scan was performed, as outlined above, but this time repeated for a broad range of Shaper-bias (15.6uA - 25.2uA). The mean values
for Gain, Threshold and Input Noise (of all 128 channels) is derived from the threshold scans and then plotted as a function of Shaper bias.

* Gain as function of Shaper bias.
* Threshold as function of Shaper bias.
* Input noise as function of Shaper bias.

Again there is a broad operating range for the Shaper-bias, Gain and

Threshold are constant in the range of 16.8uA to 20.4uA. The noise is a bit more difficult to interpretate, there is a significant spread in the input noise as the bias changes, but this could also be linked to the 'Time-walk' associated with different injected charges. The Shaper-bias is set to a nominal value of 18uA, which is less than the design specification of 20.4uA.

Results

Using the experimentally derived settings for F.E.bias and Shaper-bias, the following results have been obtained for single-chip and dual chip operation
with also different foil substrate connections to AGND+DGND and AGND only.

Single-chip operation (substrate connected to AGND+DGND and AGND only)	Dual chip operation (subtrate connected to AGND+DGND and AGND only)
Gain (mV/fC) for 2fC, 3fC and 4fC charge injection	Gain (mV/fC) for 2fC, 3fC and 4fC charge injection
Threshold (mV) for 2fC, 3fC and 4fC charge injection	Threshold (mV) for 2fC, 3fC and 4fC charge injection
Input Noise (fC) for 2fC, 3fC and 4fC charge injection	Input Noise (fC) for 2fC, 3fC and 4fC charge injection

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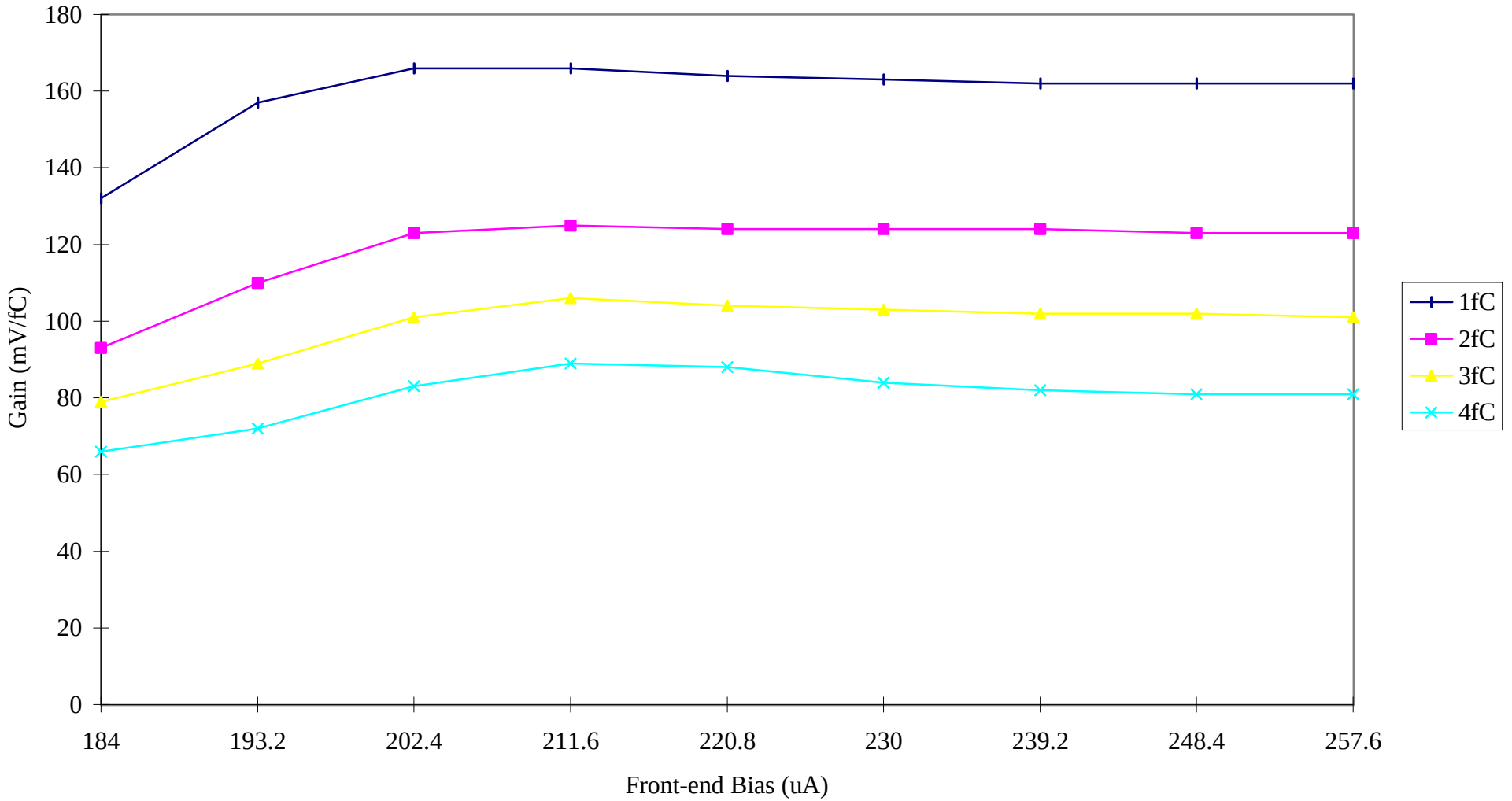
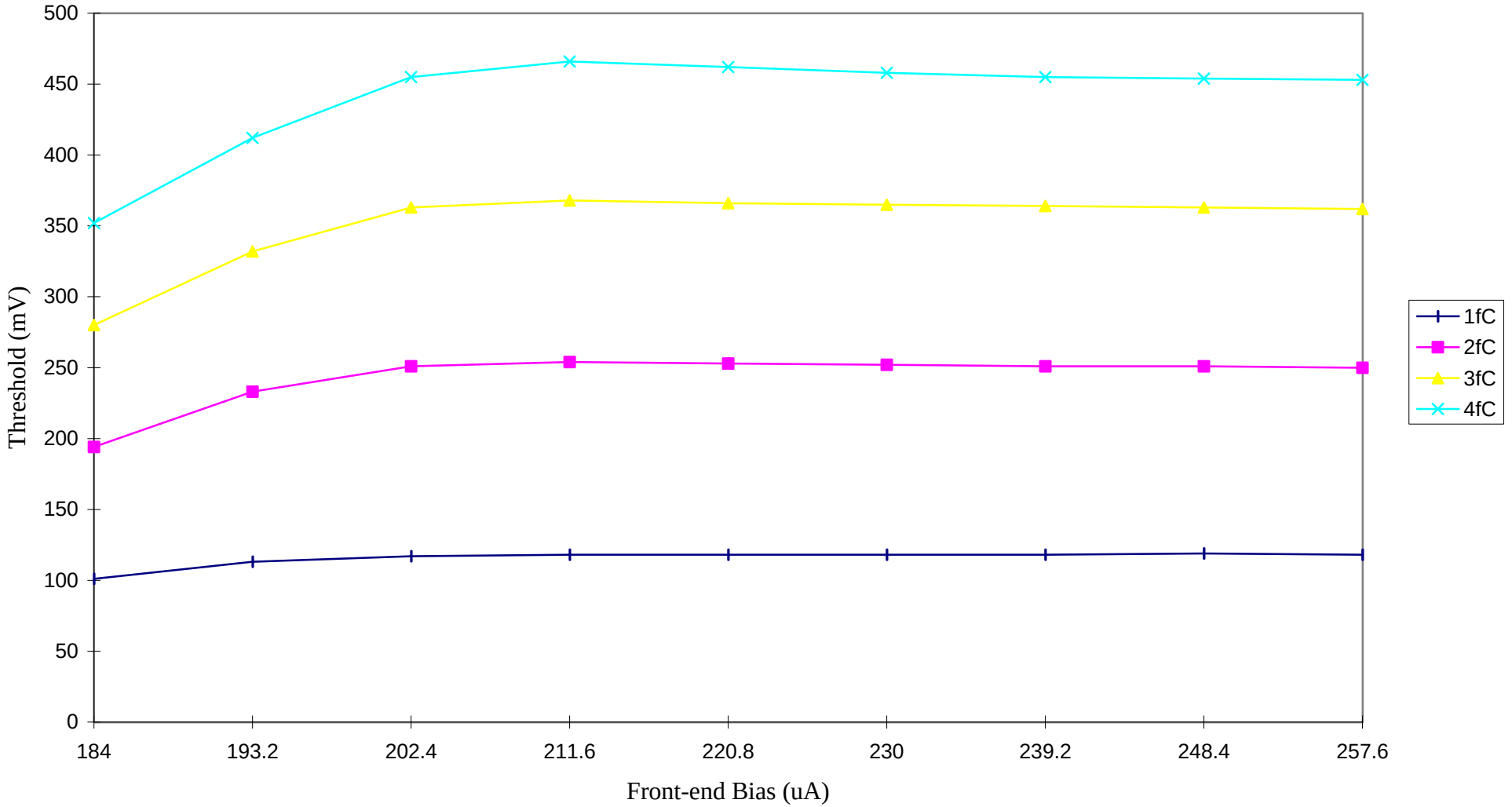
Conclusions and Observations

* Performance is much better than the original ABCD1, the chip has a much wider range of bias settings.
* Able to resolve calibration signals of 1fC (or less!). Threshold scan for 1fC calibration showing the first 8 channels (Edge mode).
* No evidence of oscillation at low thresholds, though there is a residue noise component (Pedestal?) upto a threshold of 80mV.
* Initial results indicate that the chip backplane connection should be made to AGND only.
* As I add/enable more chips the value of threshold with which the s-curves start to fall off is actually decreasing. This can be seen quite clearly on the following S-curves for 1fC calibration (channels 0 - 1 on Master) for one, two and three chips enabled. For the three chips so far tested for each additional chip enabled the VT50 value (on the three chips) falls by approx. 22mV (for nominal injected charge), this value appears to be independent of injected charge. I have tried adjusting the power supplies VCC and VDD plus F.E.bias, Shaper-bias and Strobe delay to see if the s-curves will recover to their original state (single chip operation) but to no avail.

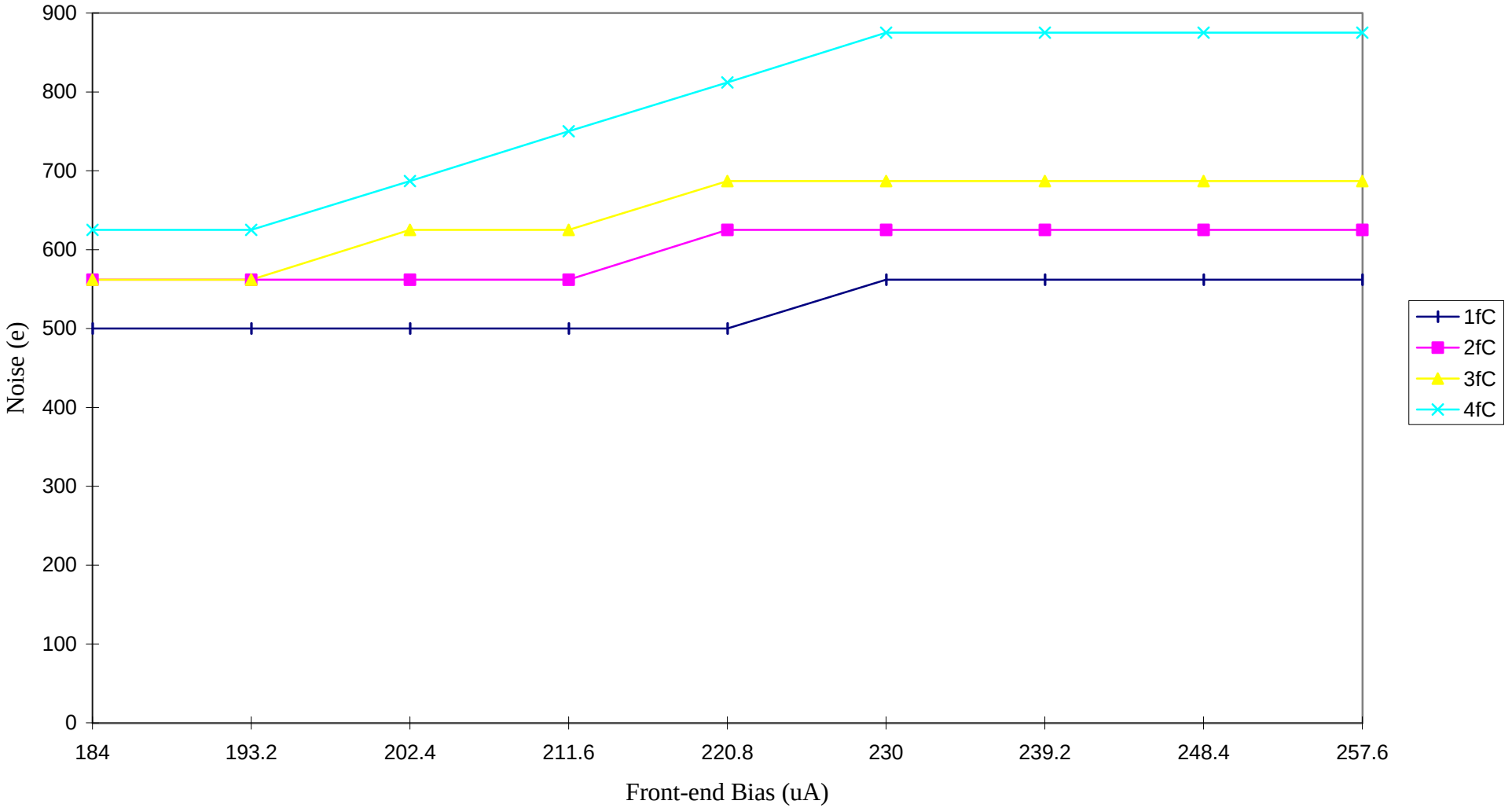
ABCD2 (Thinned) Master Chip only
Gain (mV/fC) as a function of Front-end Bias for 1fC - 4fC calibration



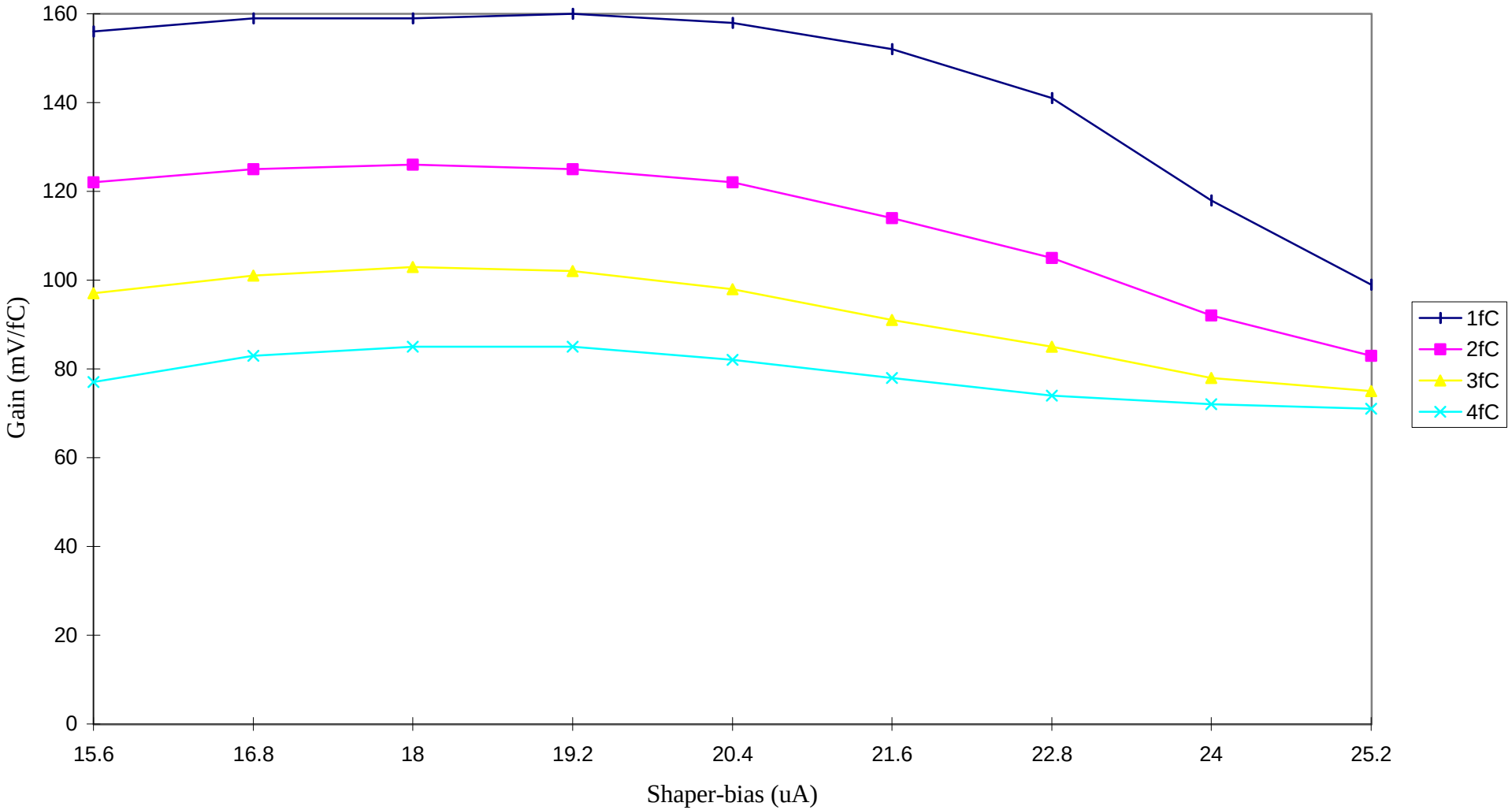
ABCD2 (Thinned) Master Chip only
Threshold (VT50) as a function of Front-end Bias for 1fC - 4fC calibration



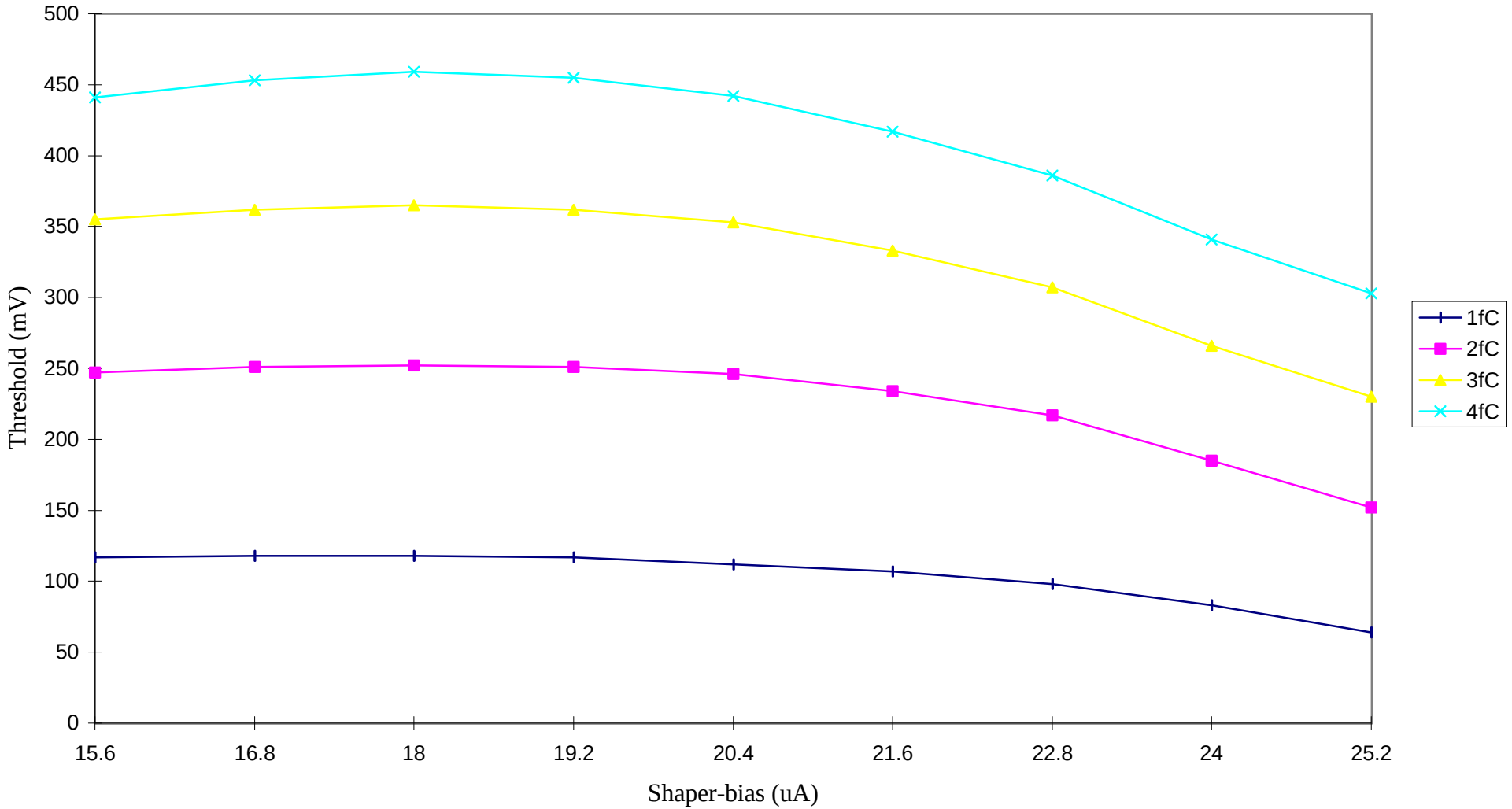
ABCD2 (Thinned) Master Chip only
Input Noise as a function of Front-end Bias for 1fC - 4fC calibration



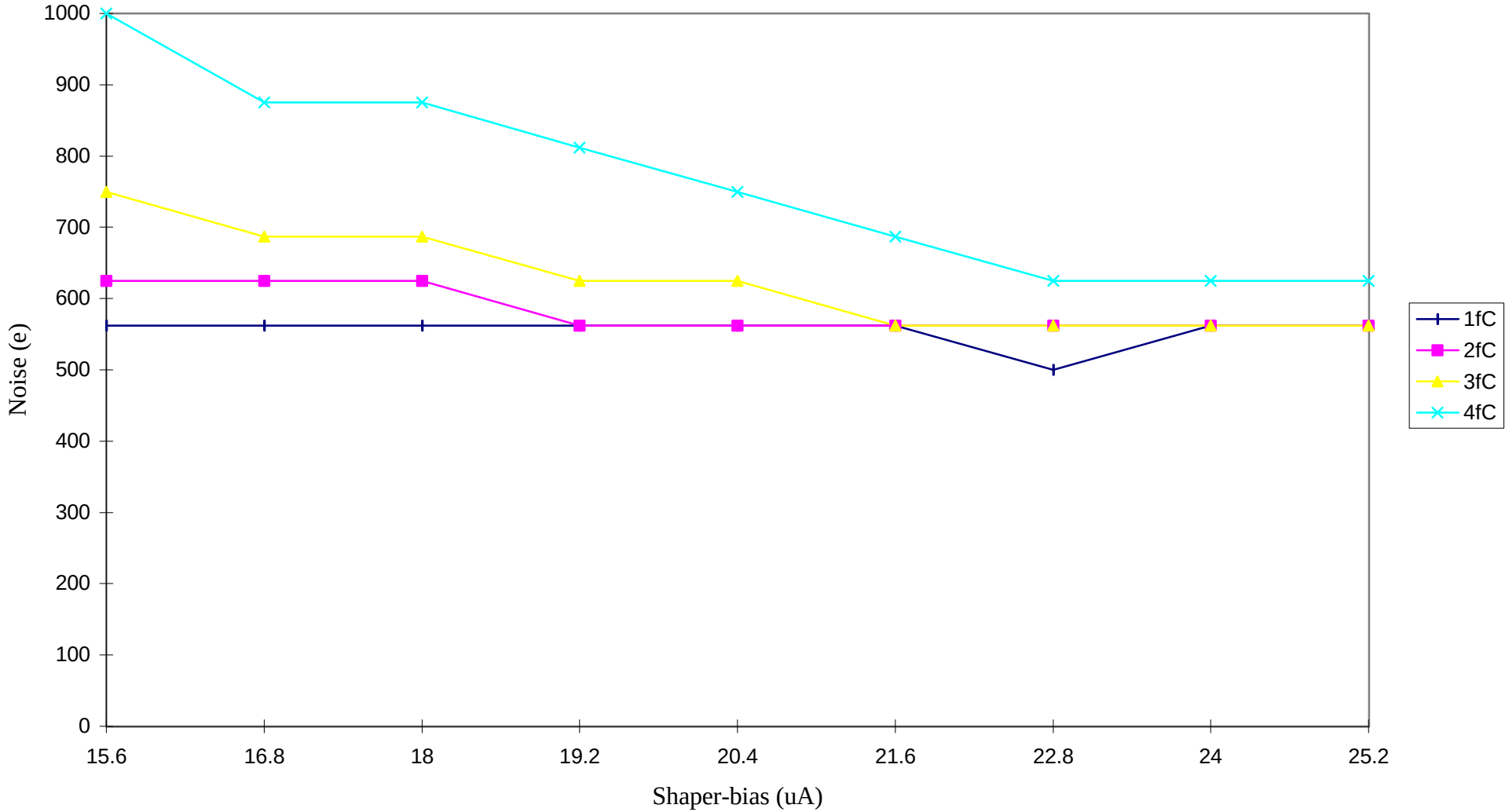
ABCD2 (Thinned) Master Chip only
Gain (mV/fC) as a function of Shaper-bias for 1fC - 4fC calibration

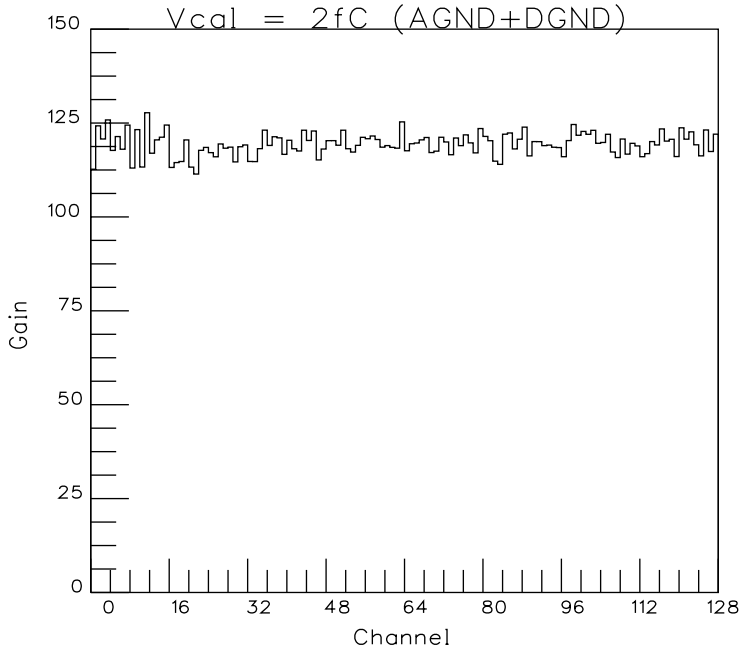


ABCD2 (Thinned) Master Chip only
Threshold (VT50) as a function of Shaper-bias for 1fC - 4fC calibration



ABCD2 (Thinned) Master Chip only
Input Noise as a function of Shaper-bias for 1fC - 4fC calibration




Vcal = 2fC (AGND+DGND)
Gain
Channel
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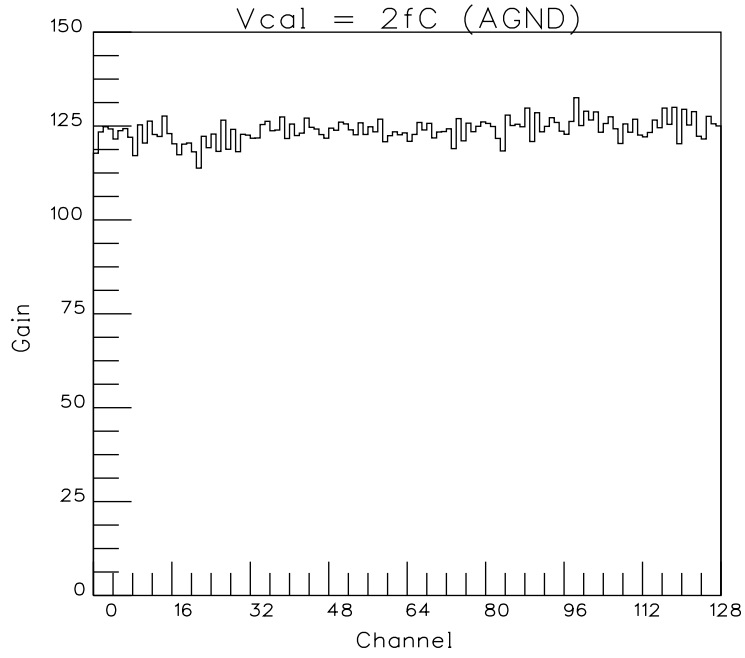
Vcal = 2fC (AGND)
Gain
Channel
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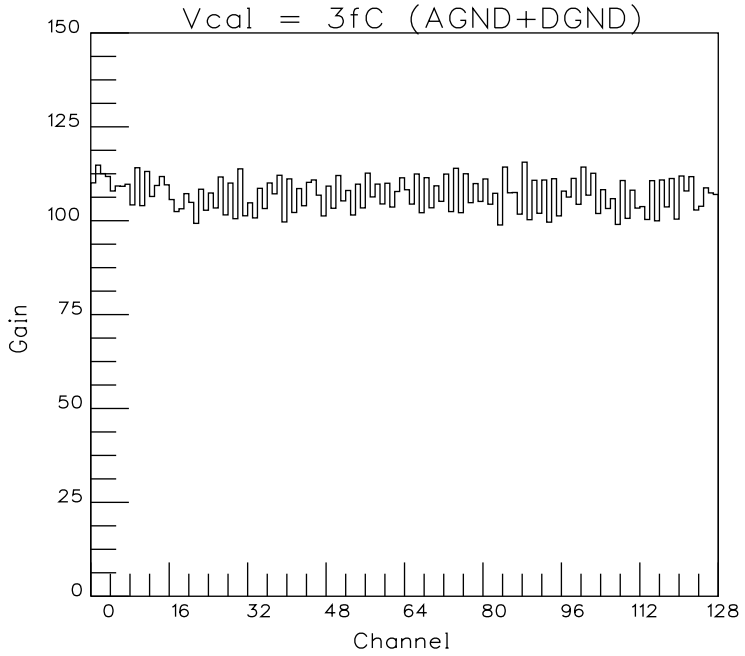
Vcal = 3fC (AGND+DGND)
Gain
Channel
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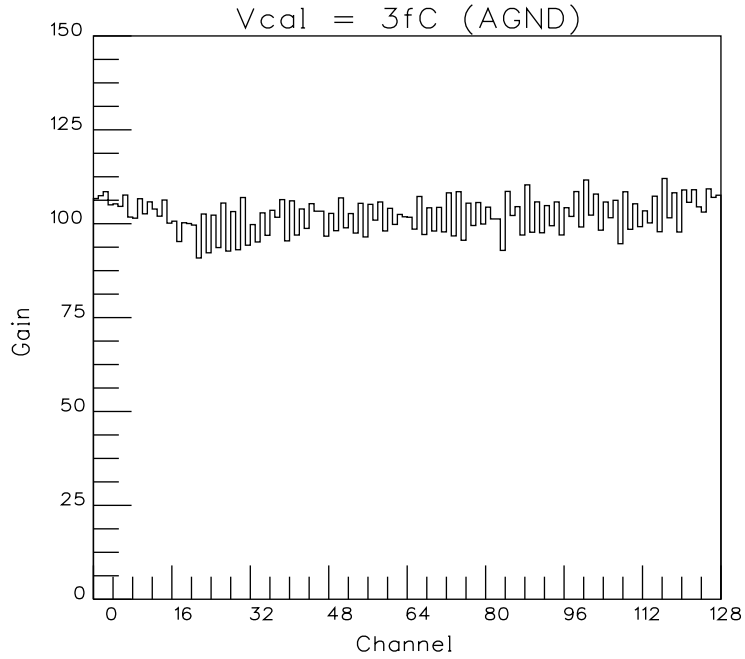
Vcal = 3fC (AGND)
Gain
Channel
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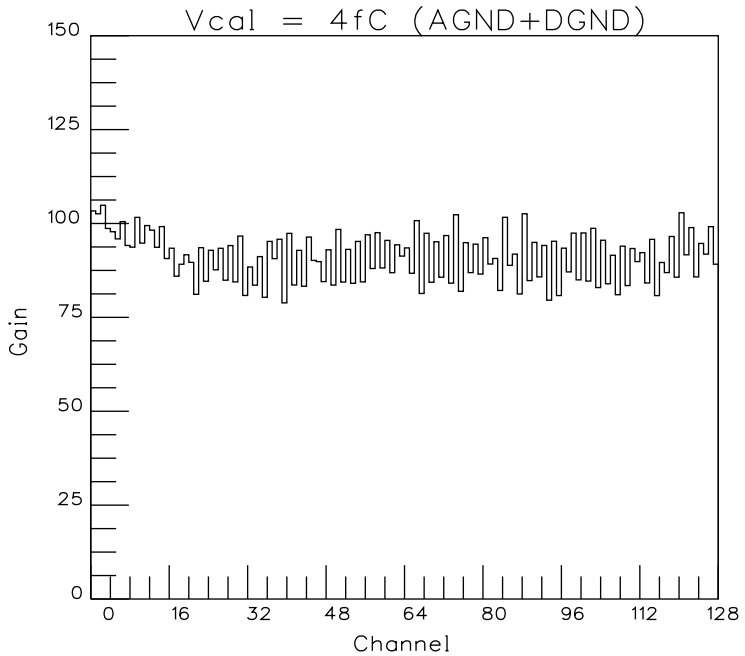
Vcal = 4fC (AGND+DGND)
Gain
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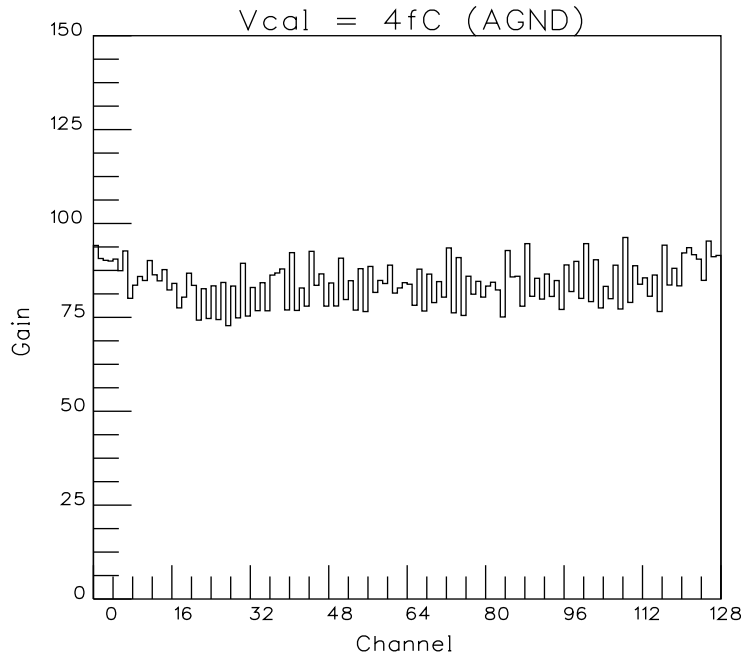
Vcal = 4fC (AGND)
Gain
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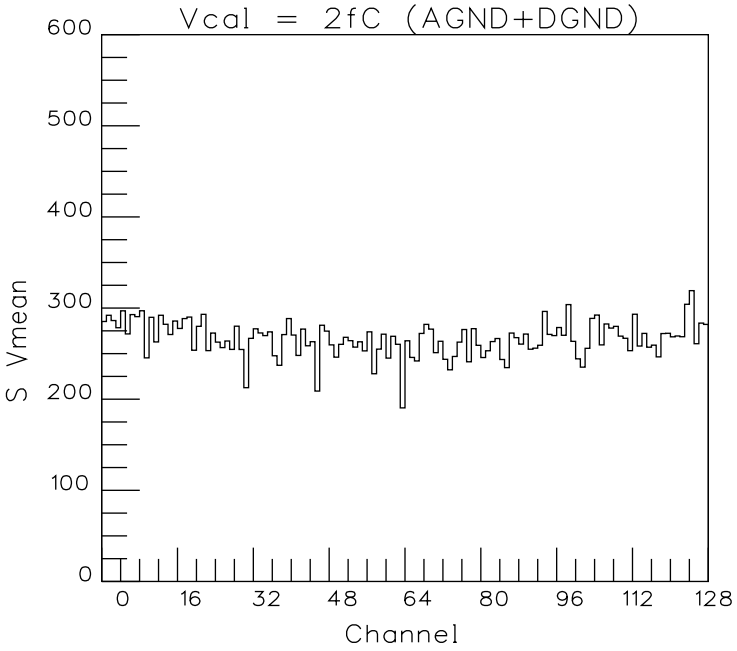
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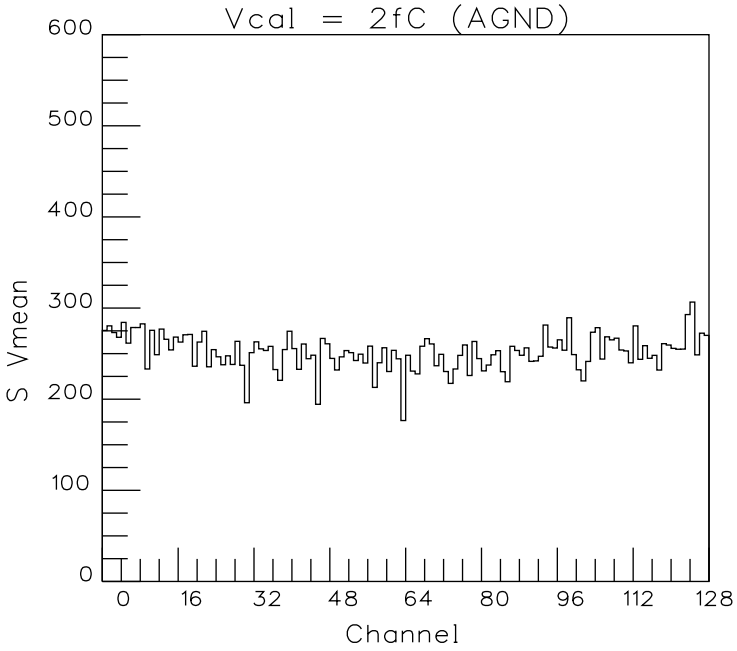
Vcal = 2fC (AGND)
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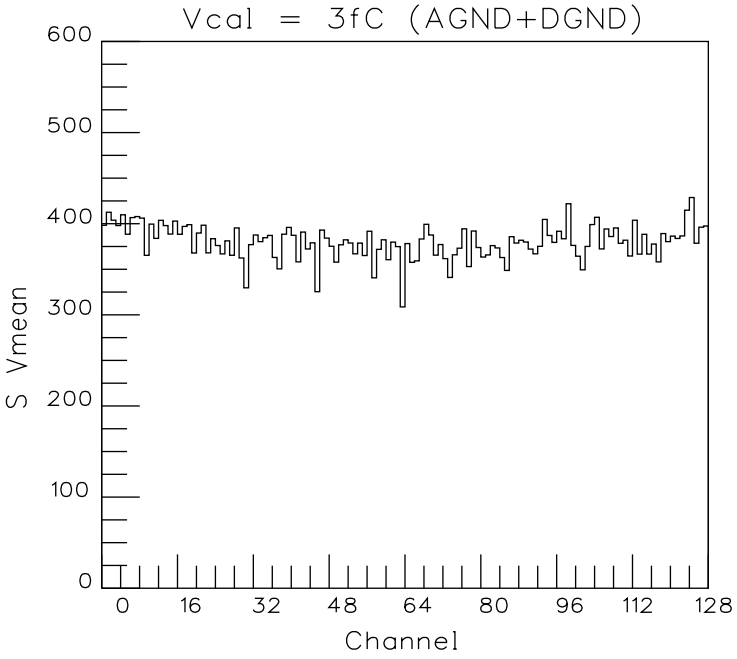
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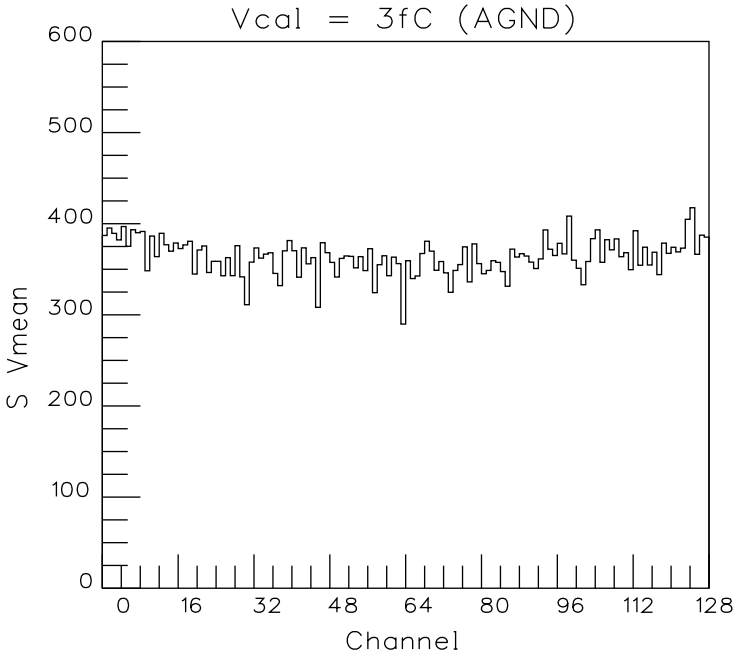
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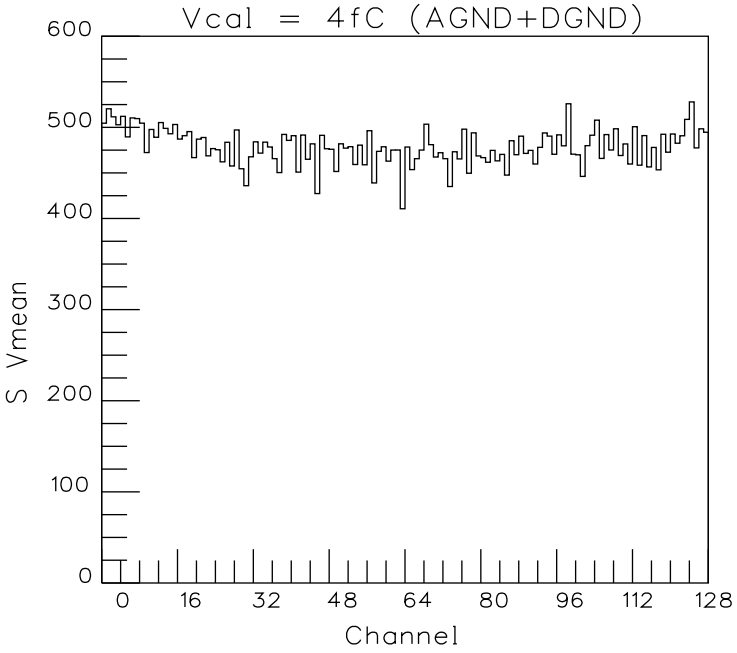
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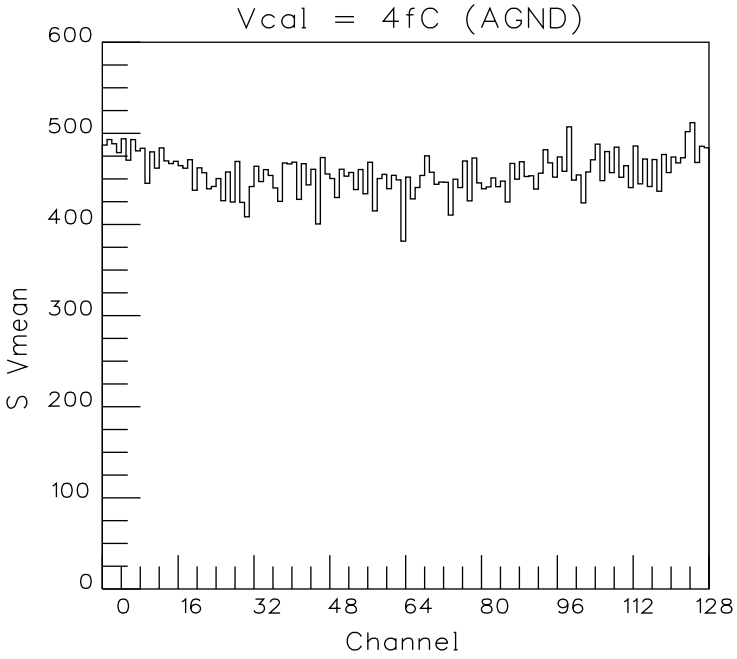
Vcal = 4fC (AGND)
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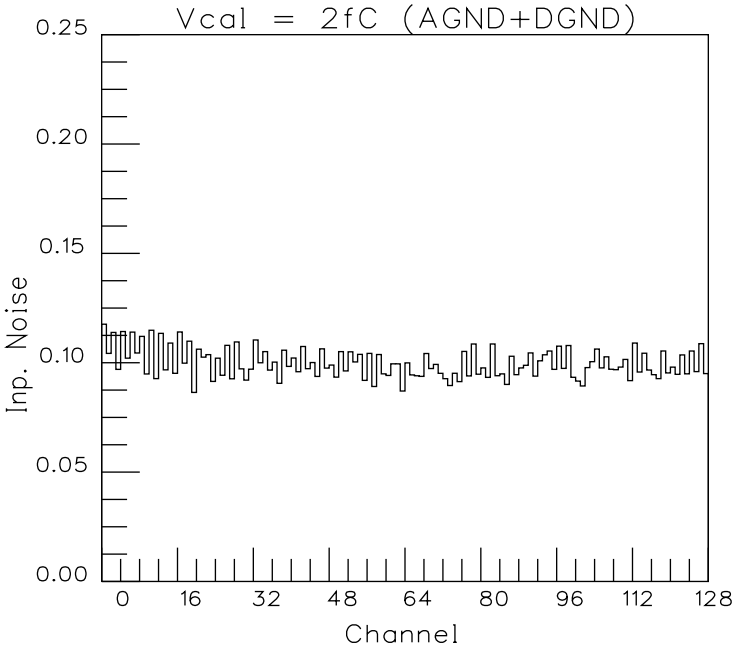
Vcal = 2fC (AGND+DGND)
Inp. Noise
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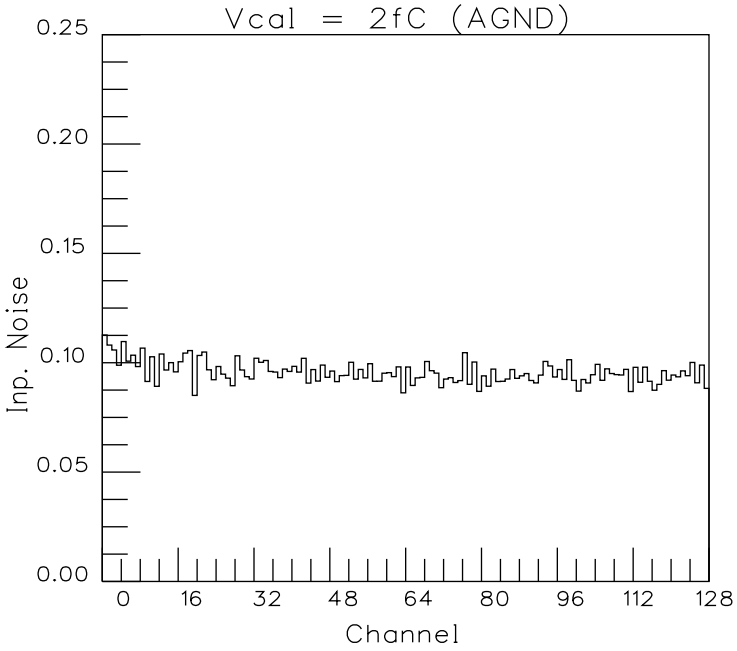
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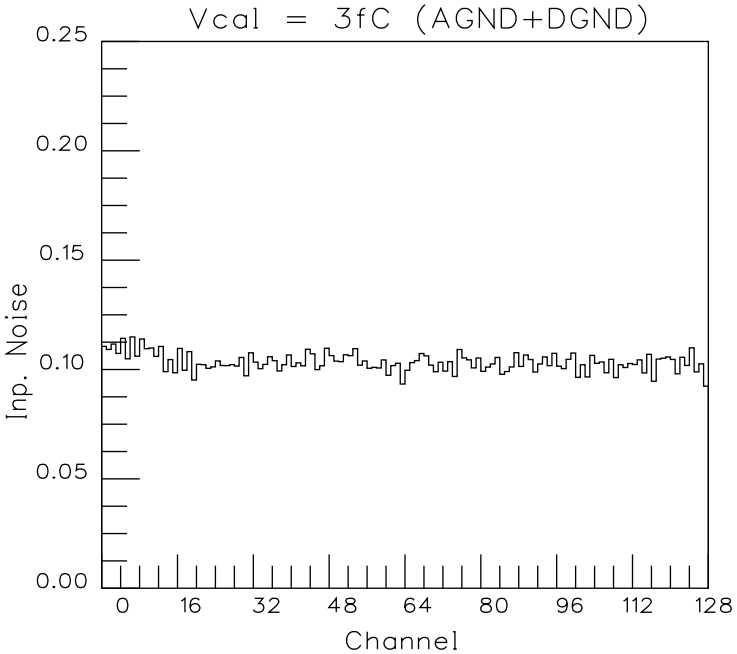
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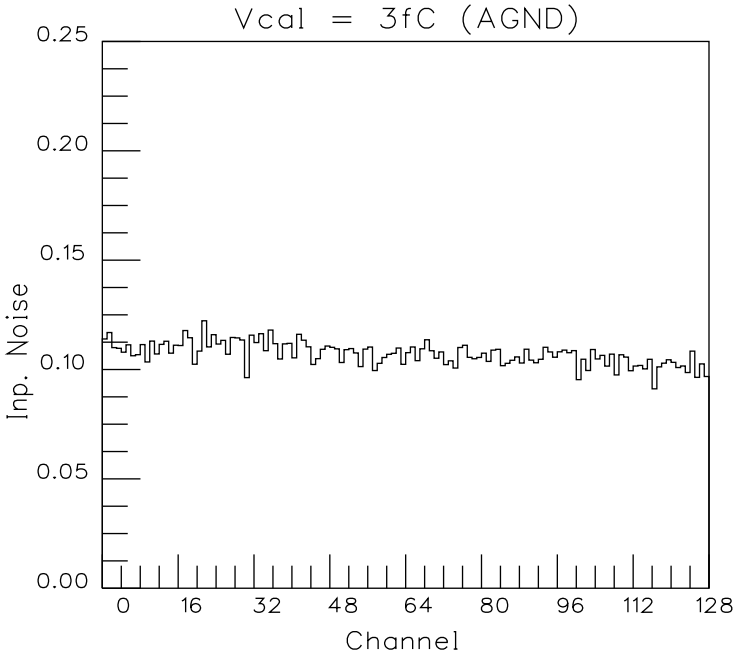
Vcal = 3fC (AGND)
Inp. Noise
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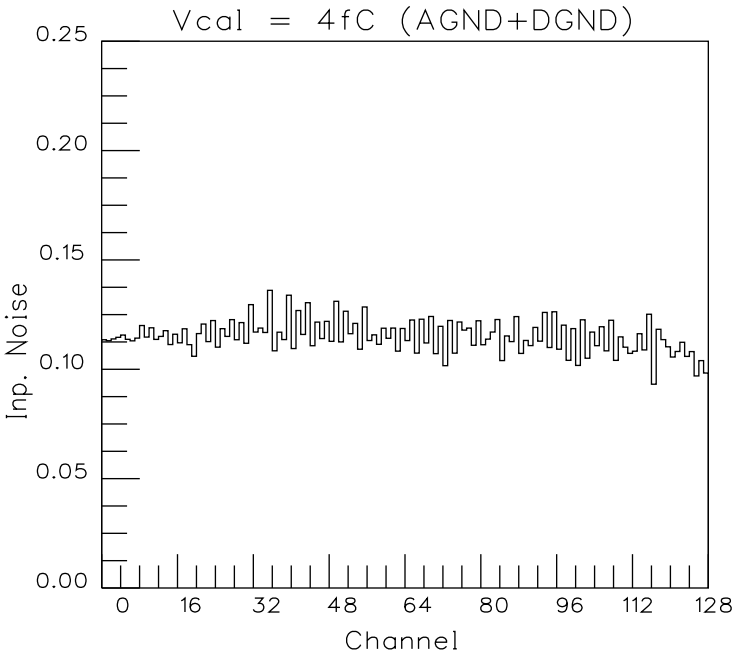
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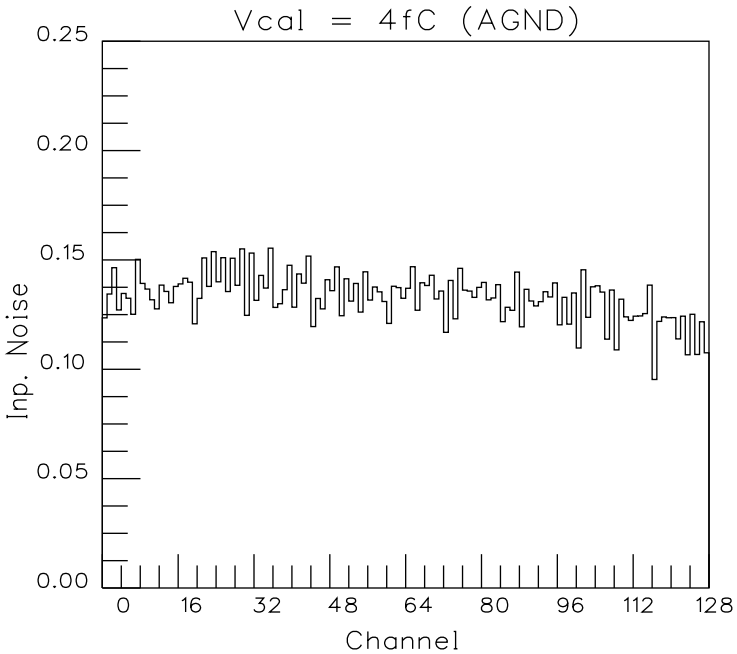
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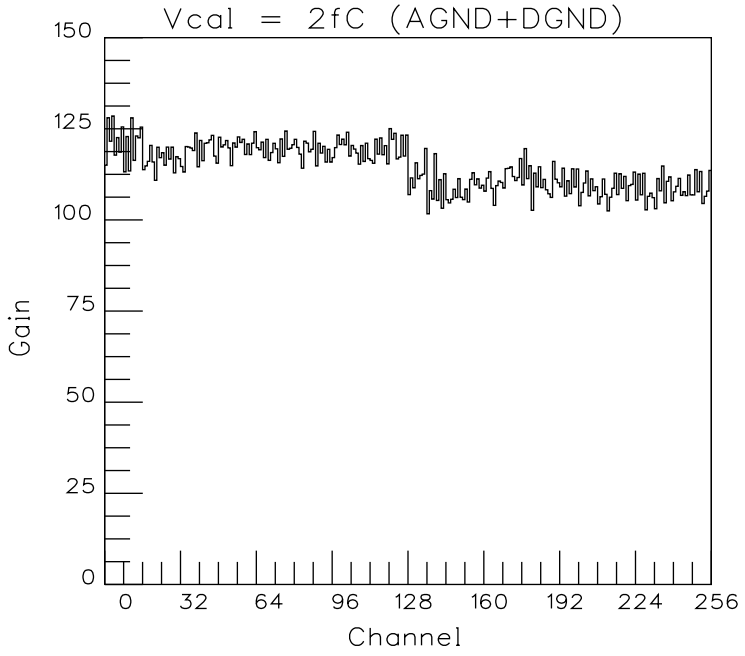
Vcal = 2fC (AGND+DGND)
Gain
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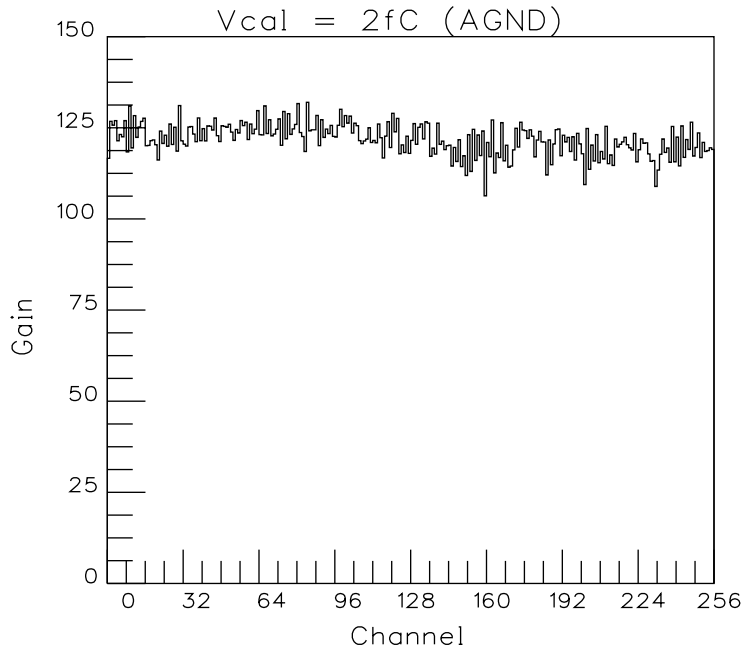
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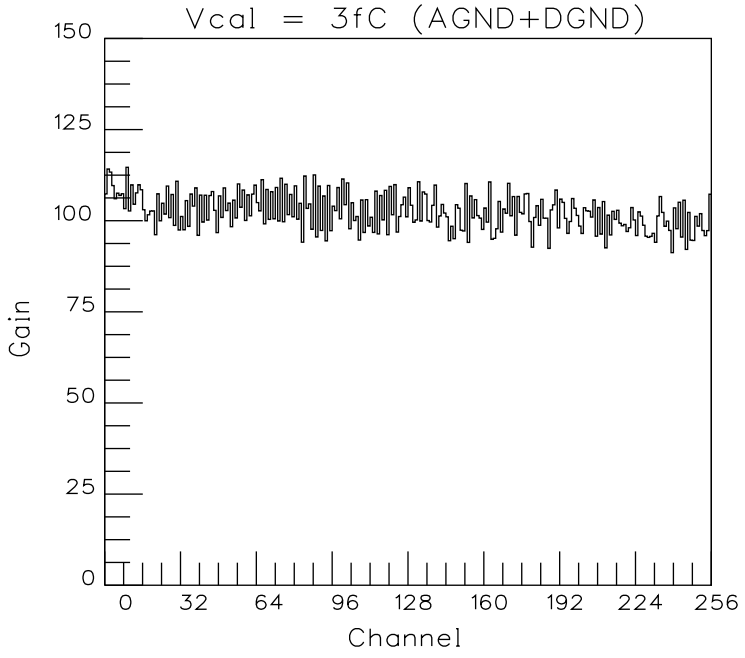
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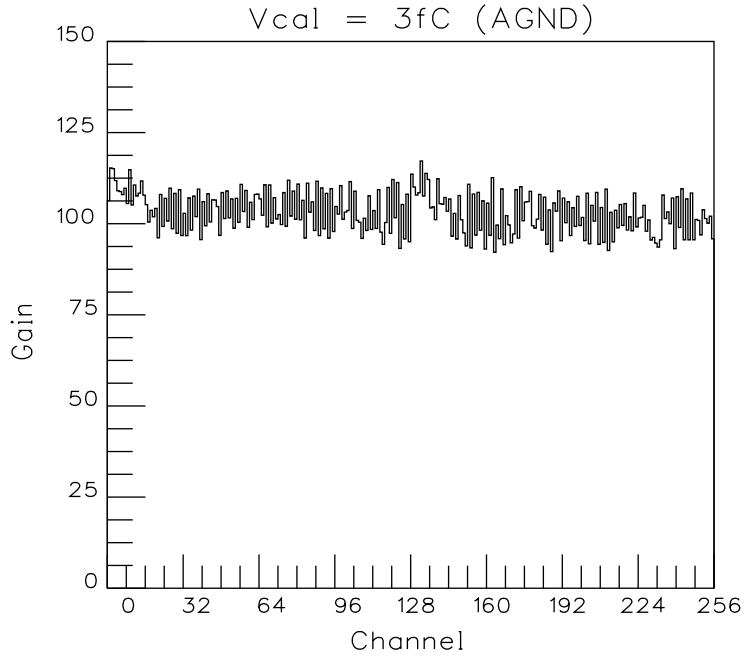
Vcal = 3fC (AGND)
Gain
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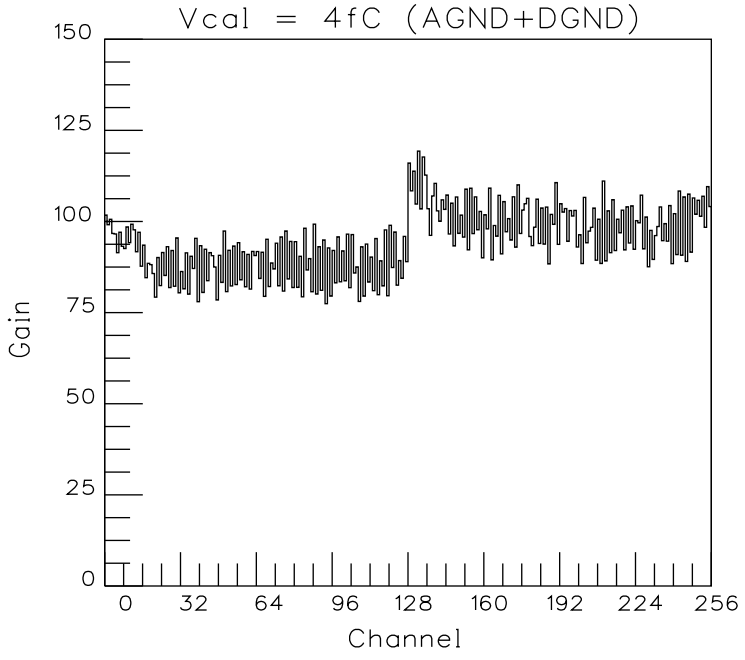
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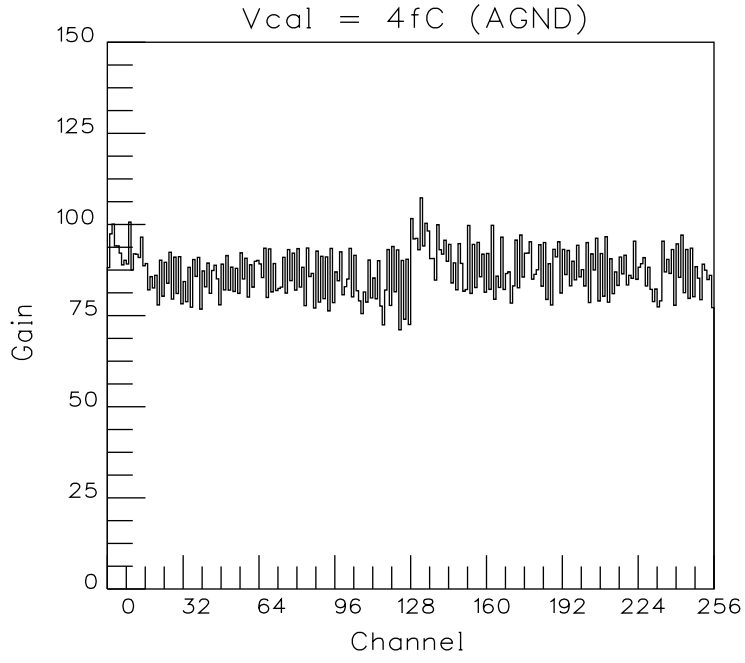
Vcal = 4fC (AGND)
Gain
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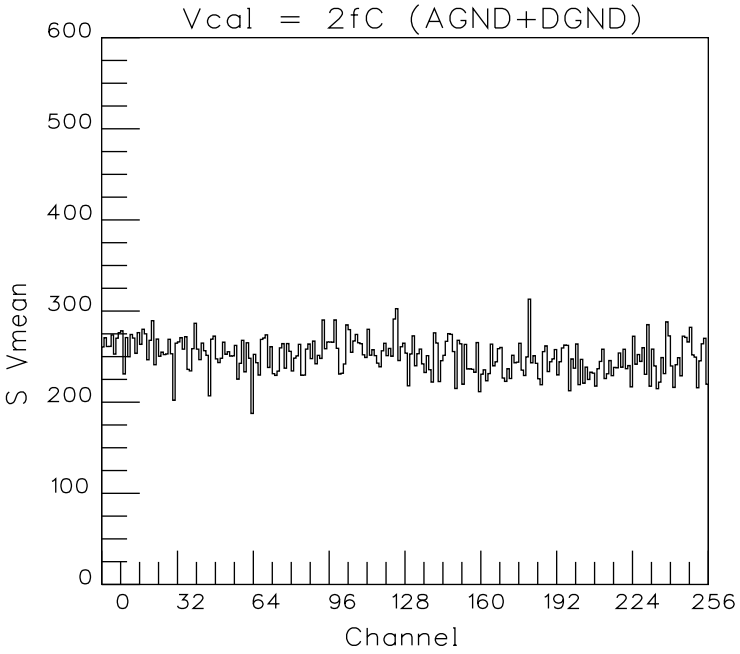
Vcal = 2fC (AGND+DGND)
S Vmean
Channel
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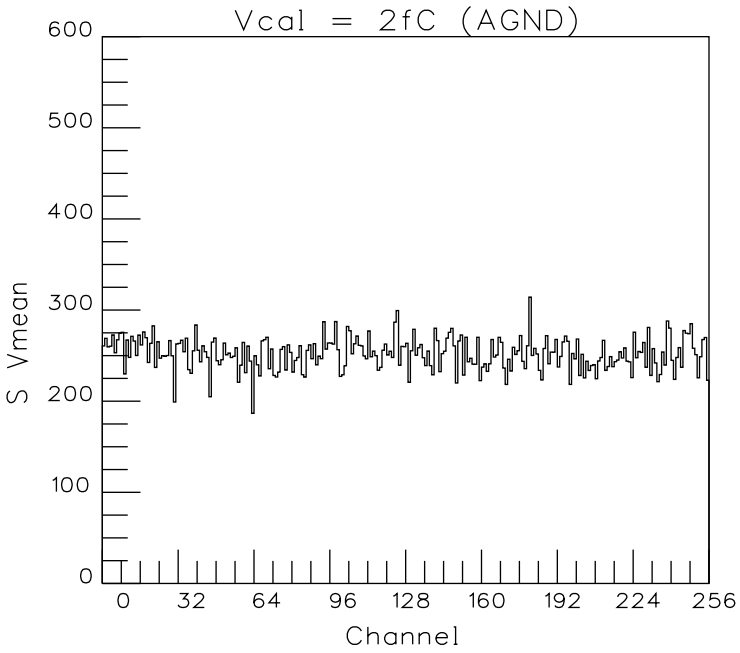
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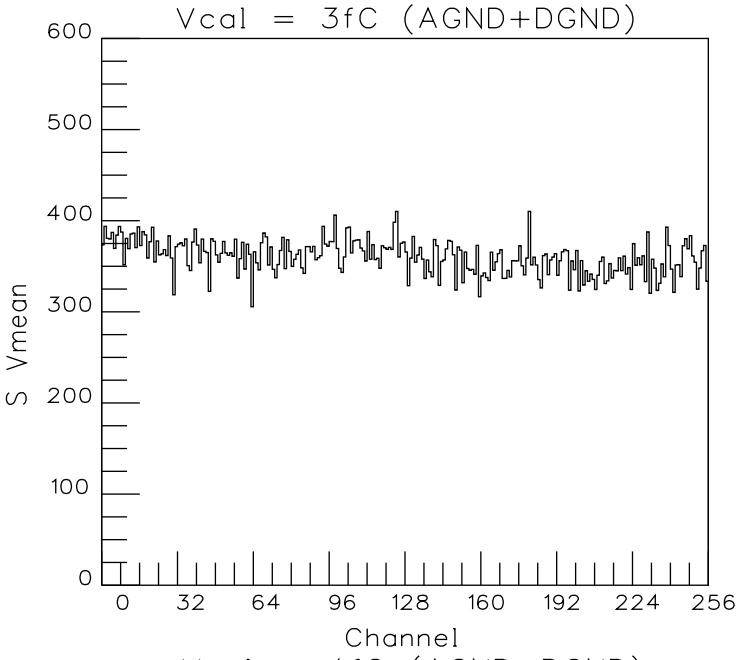
Vcal = 3fC (AGND+DGND)
S Vmean
Channel
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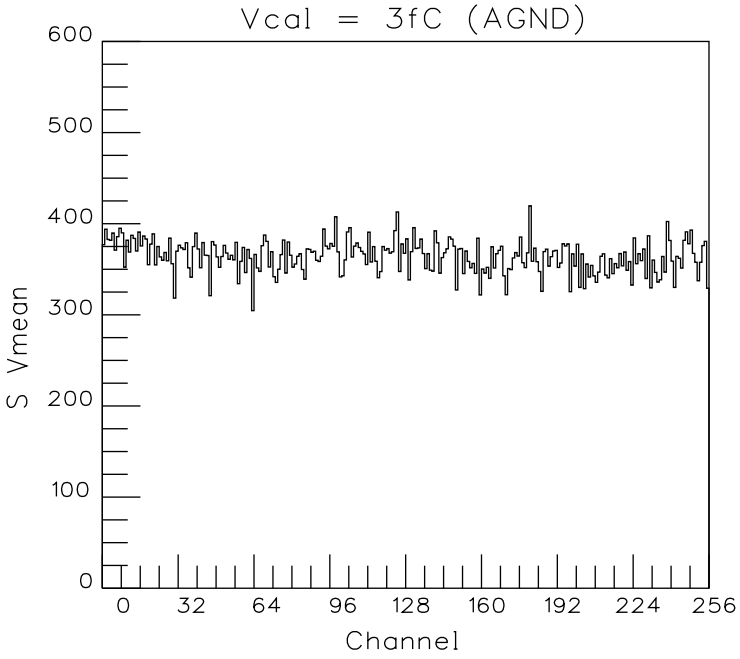
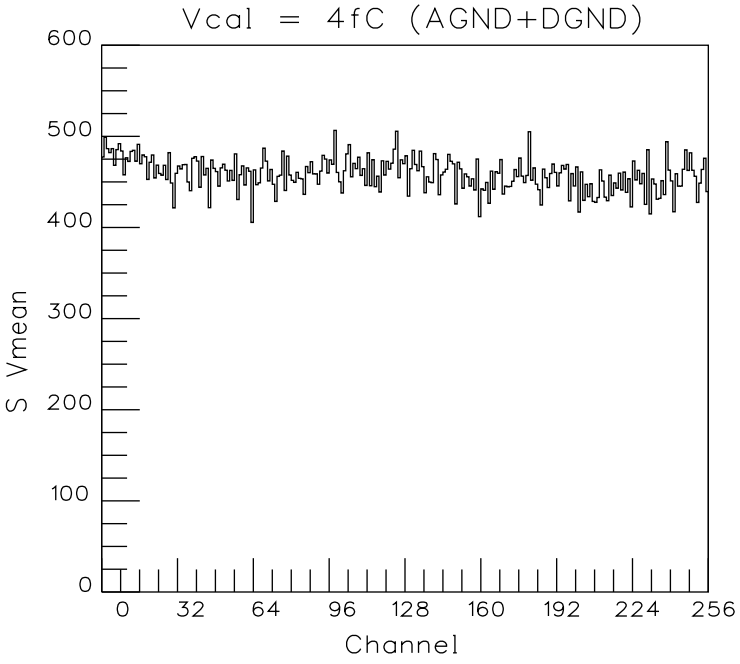
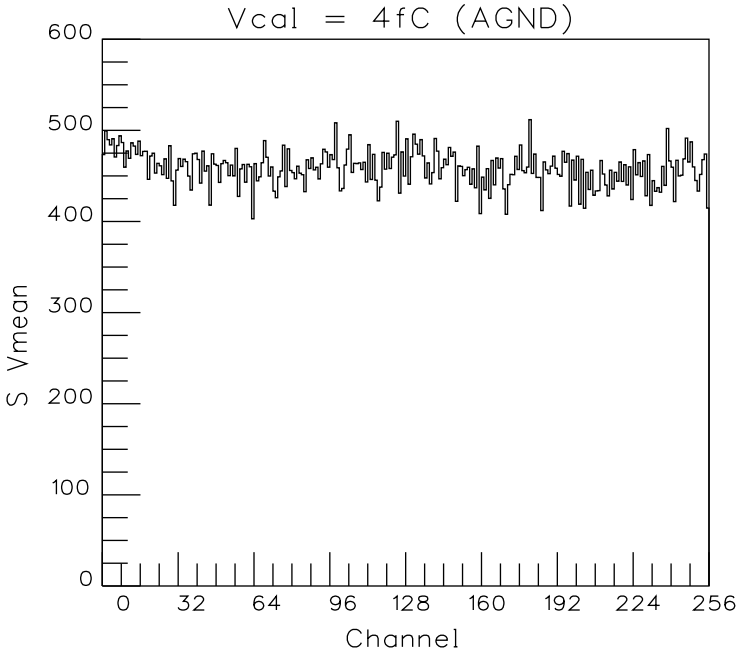
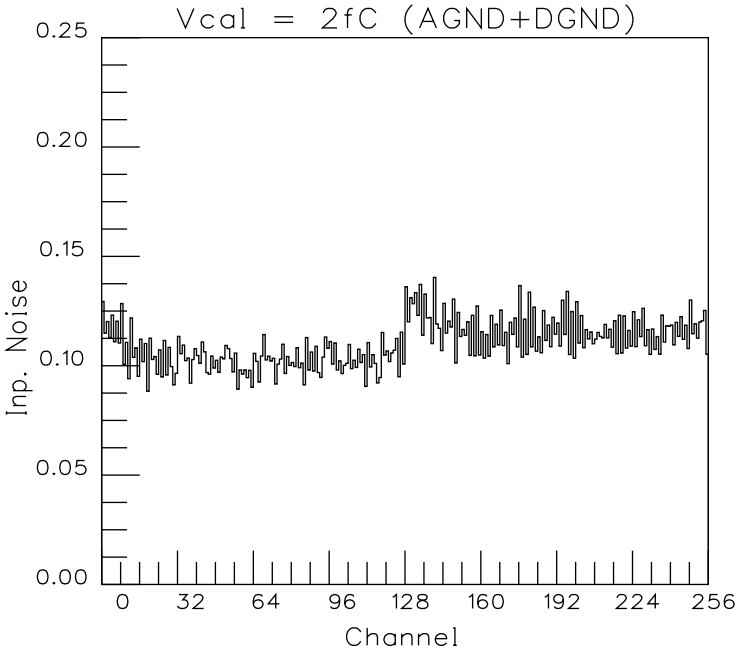
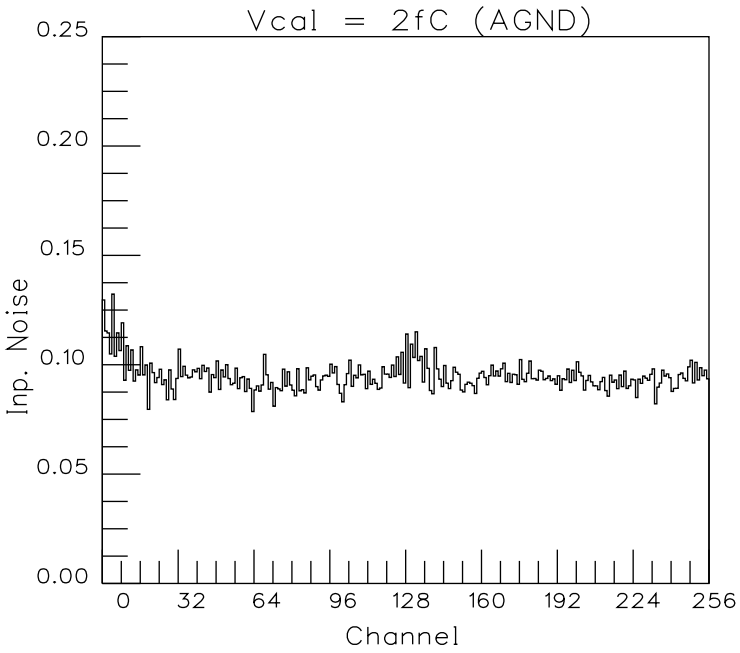
224
256

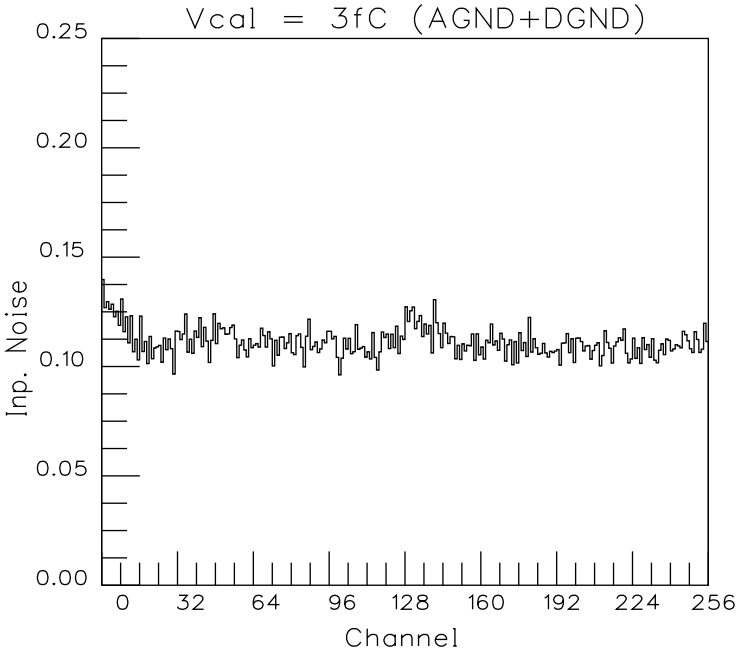

Vcal = 3fC (AGND)
S Vmean
Channel
0
100
200
300
400
500
600
0
32
64
96
128
160
192
224
256

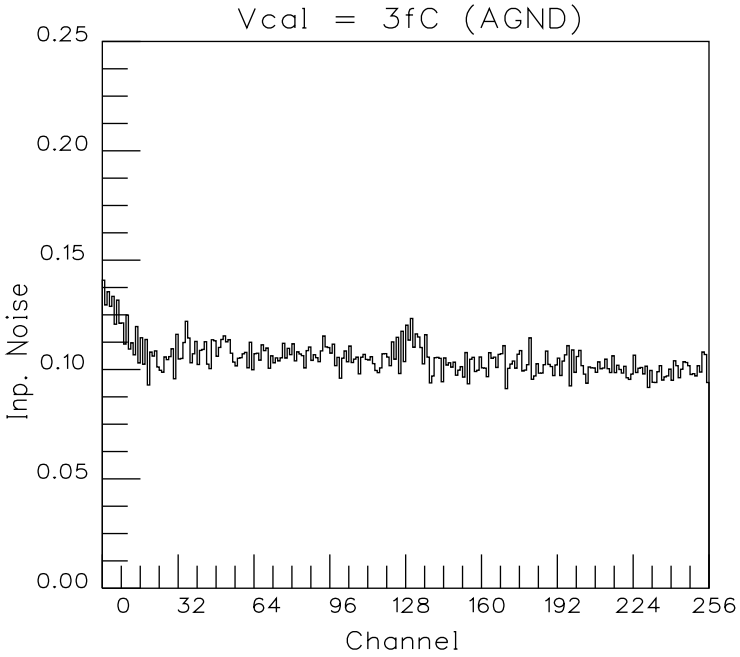

Vcal = 4fC (AGND+DGND)
S Vmean
Channel
0
100
200
300
400
500
600
0
32
64
96
128
160
192
224
256

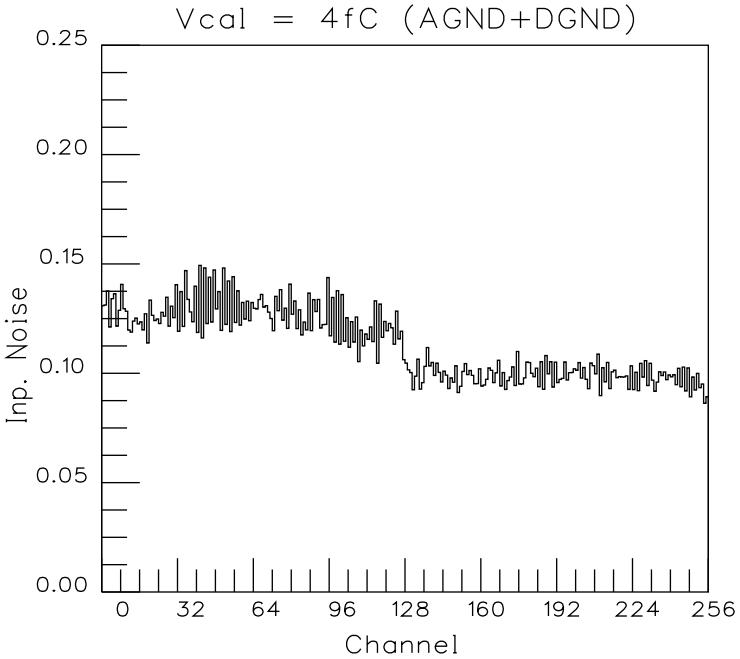

Vcal = 4fC (AGND)
S Vmean
Channel
0
100
200
300
400
500
600
0
32
64
96
128
160
192
224
256

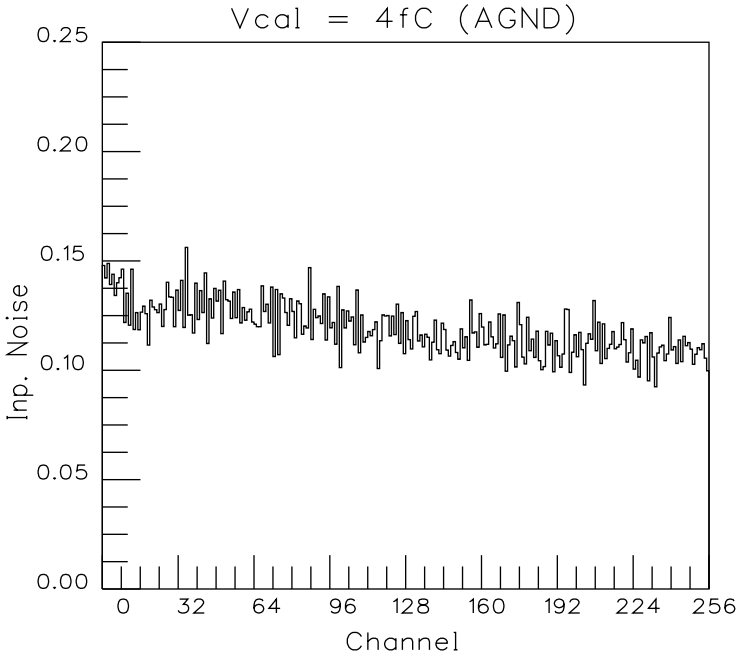

Vcal = 2fC (AGND+DGND)
Inp. Noise
0.25
0.20
0.15
0.10
0.05
0.00
0
32
64
96
128
160
192
224
256
Channel

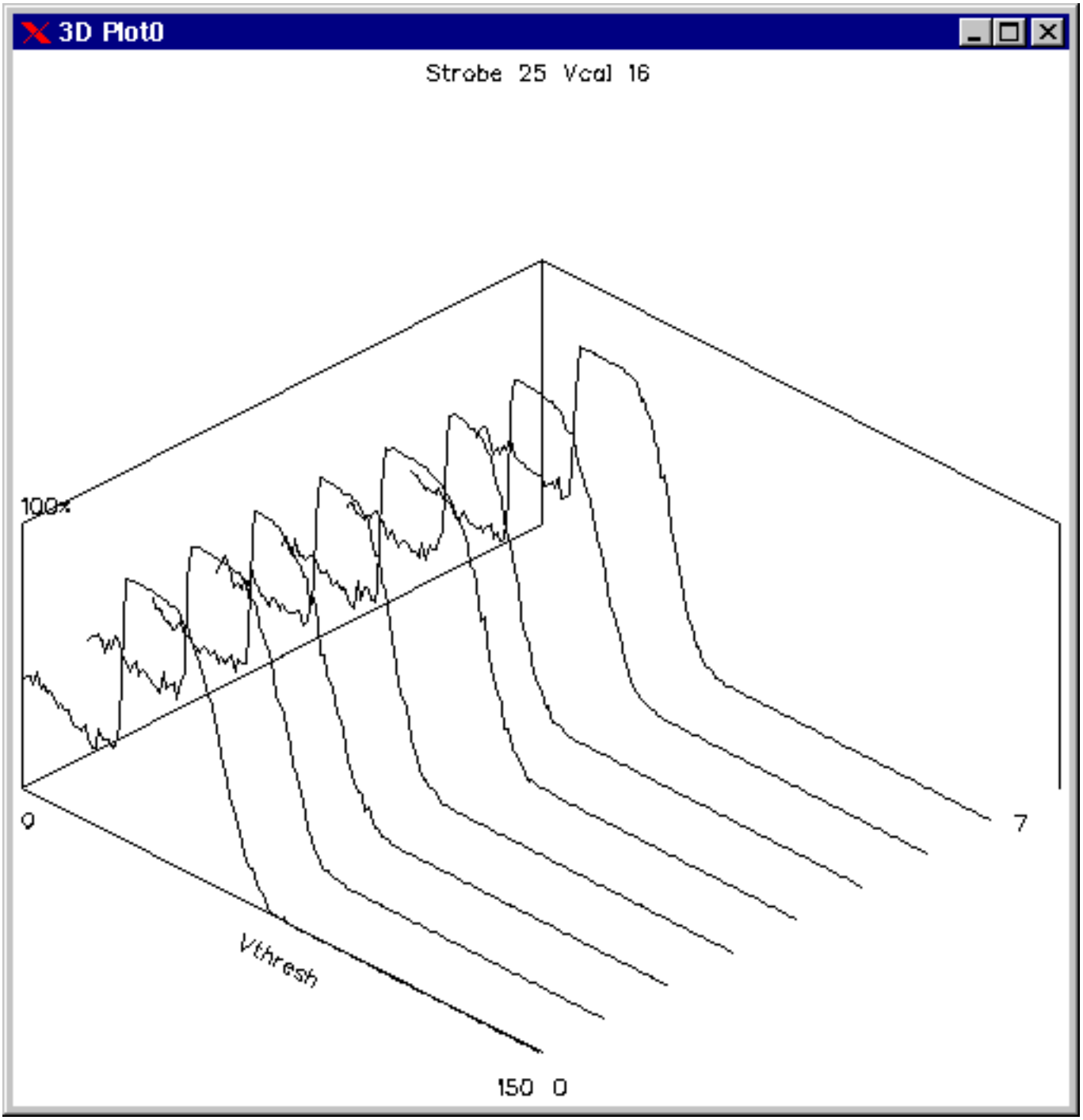

Vcal = 2fC (AGND)
Inp. Noise
0.25
0.20
0.15
0.10
0.05
0.00
0
32
64
96
128
160
192
224
256
Channel

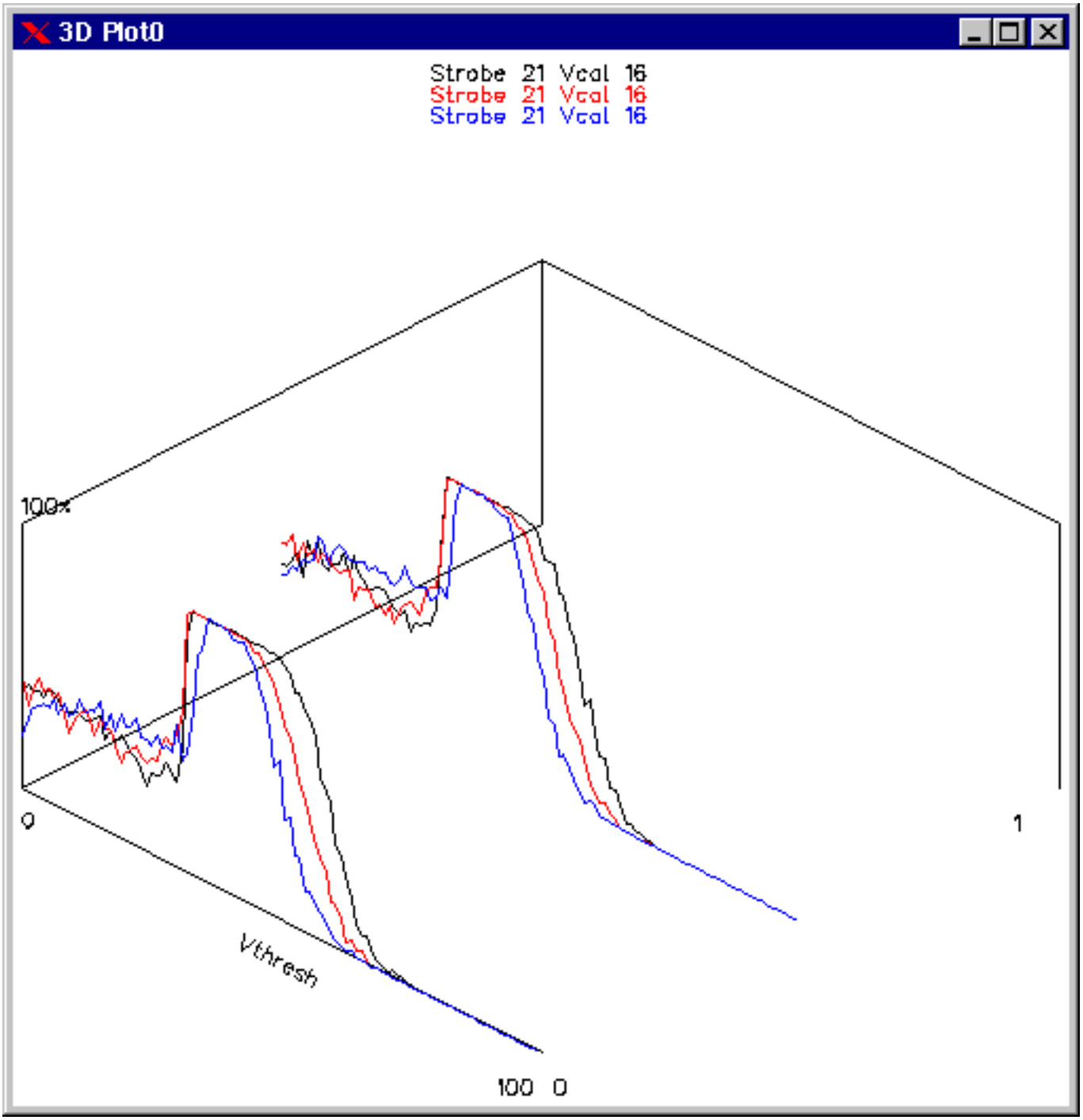

Vcal = 3fC (AGND+DGND)
Inp. Noise
0.25
0.20
0.15
0.10
0.05
0.00
0
32
64
96
128
160
192
224
256
Channel


Vcal = 3fC (AGND)
Inp. Noise
0.25
0.20
0.15
0.10
0.05
0.00
0
32
64
96
128
160
192
224
256
Channel


Vcal = 4fC (AGND+DGND)
Inp. Noise
0.25
0.20
0.15
0.10
0.05
0.00
0
32
64
96
128
160
192
224
256
Channel


Vcal = 4fC (AGND)
Inp. Noise
0.25
0.20
0.15
0.10
0.05
0.00
0
32
64
96
128
160
192
224
256
Channel


3D Plot0
Strobe 25 Vcal 16
100%
0
7
Vthresh
150 0


3D Plot0
Strobe 21 Vcal 16
Strobe 21 Vcal 16
Strobe 21 Vcal 16
100%
0
1
Vthresh
100 0