Proposed Reliability Tests

Tests on fully loaded hybrids

* Visual Inspection

* Bond Strength & Lifetime

* Solder pad adhesion

Tests on modules

* Intermittent life

* Thermal cycling

Visual Inspection (I)

* Purpose: The purpose of this test is to inspect the visible top metal layer(s) of the hybrid and passive components mounted on the hybrid. It shall be performed on a 100 percent inspection basis to detect and eliminate hybrids with visual defects that could lead to failure in normal operation.

* Apparatus: Stereo Microscope capable of the needed magnification, ESD protected work place, appropriate fixture/protection for hybrid or module, dust-free environment

* Procedure: A check list shall be used

* Note: For hybrids with thin film/printed resistors or capacitors refer to the full original standard

* Points to be inspected: See next page

Ref: MIL-STD-883E, Method 2032.1

Visual Inspection (II)

Points to be inspected:

o Bonding pads -- MIL-STD-883E Method 2032.1, page 40
o Metal traces: Scratches -- MIL-STD-883E Method 2032.1, page 39

Voids -- See MIL-STD-883E Method 2032.1, page 41

o Corrosion, Adherence, Protrusion -- MIL-STD-883E Method 2032.1, p. 43
o Overlap -- MIL-STD-883E Method 2032.1, page 43
o Substrate defects -- MIL-STD-883E Method 2032.1, page 45-46
o Nonplanar element inspection -- MIL-STD-883E Method 2032.1, pp. 54-62

Bond Strength (I)

* Purpose: The purpose of this test is to measure the strength of the wedge wire bonds at the die, the hybrid, the fanout and the detector.

* Apparatus: Suitable equipment for applying the specified stress to the bond. A calibrated measurement of the applied force in grams with an accuracy of 5 percent shall be provided by the equipment.

* Procedure: The wire shall be cut so as to provide two ends accessible for pull tests. The wire shall be gripped in a suitable device and simple pulling action applied to the wire (or the device) in such a manner that the force is applied approximately normal to the surface of the die or substrate. When a failure occurs, the force causing the failure and the failure category shall be recorded.

Ref: MIL-STD-883E Method 2011.7

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Bond Strength (II)

* Sample: At least 4 hybrids for each manufacturing lot available shall be randomly chosen. On each device, 10 bonds

o From the die to the hybrid
o From the die to the fanout
o From the fanout to the detector shall be taken at random.

* Required strength:

Wire composition and diameter	Minimum strength (g)
Al 0.0007 in	1.5
Au 0.0007 in	2.0
Al 0.0010 in	2.5
Au 0.0010 in	3.0
Al 0.00125/0.0013	3.0
Au 0.00125/0.0013	4.0
Al 0.0015 in	4.0
Au 0.0015 in	5.0

Bond Strength (III)

* Failure Categories:

1) Wire break at neckdown point
2) Wire break at point other than neckdown point
3) Failure in bond (interface between wire and metallization) at die
4) Failure in bond at hybrid
5) Failure in bond at fanout
6) Failure in bond at detector
7) Lifted metallization from die
8) Lifted metallization from hybrid
9) Lifted metallization from fanout
10) Lifted metallization from detector
11) Other fatal failures (broken die etc). Describe.

Bond Strength (IV)

* Accept:

o Zero failures
o Proper operation of the equipment is indicated when $s(X) < 0.25 X$, where X is the average bond pull strength.

Bond Lifetime: Temperature Aging (I)

* Purpose: The purpose of this test is to test the reliability of the wire bonds for the qualification of a specific hybrid and bonding technology.

* Sample: At least 4 hybrids from each production lot available.

* Procedure: The sample shall be exposed to elevated temperature of 150 deg.C during 1000 hours. Destructive bond pull test shall be performed before, several times during and after the 1000 hours. Humidity shall be small.

* Accept: All samples fulfill the requirements of the destructive bond pull test

Ref: Wire Bonding in Microelectronics, George Harman, McGraw Hill 1997

Bond Lifetime: Temperature Aging (II)

* Time-Temperature Regression: In case above temperature is higher than the maximum operating temperature specified for a given hybrid technology, or the available time is too short, the following time-temperature regression shall be applied (scaled from MIL-STD-883E, Method 1005.8)

Temp (deg.C)	Time (h)
125	5434
135	2695
150	1000
175	217
190	163

Bond Lifetime: Humidity Aging

* Purpose: The purpose of this test is to test the reliability of the wire bonds for the qualification of a specific hybrid and bonding technology.

* Sample: At least 4 hybrids from each production lot available.

* Procedure: The sample shall be exposed to 85 deg.C/85% R.H. during at least 24 hours. Destructive bond pull test shall be performed before, after 12 h and after 24 h.

* Accept: All samples fulfill the requirements of the destructive bond pull test.

Ref: Wire Bonding in Microelectronics, George Harman, McGraw Hill 1997

Solder Pad Adhesion

* Purpose: The purpose of this test is to check the capabilities of the hybrid solder pads to withstand a delamination (peel) stress of specified tension and time.

* Sample: 4 pads of 4 hybrids (16 pads in total) for each production lot.

* Note: This test is a modification of the original method 2004.5.

* Procedure: A copper wire with gauge as close to the pad width as possible, shall be soldered to the pad to be tested. A tension of x g (suggested value: 227 g) shall be applied to the wire, without shock, in a direction orthogonal to the hybrid. Test time is 30 seconds.

* Figure: See MIL-STD-883E, Method 2004.5, page 7

* Failure: Any evidence of loosening or breakage.

Ref: MIL-STD-883E, Method 2004.5

Modules: Intermittent Life

* Purpose: The purpose of this test is to determine a representative failure rate for modules and/or demonstrate the reliability of the devices.

* Sample: As large as affordable.

* Procedure: DUT's shall be exposed to 125 deg.C for 1000 hours minimum. Before, several times during and after the test, the devices shall be electrically tested. The hybrids shall be operated at nominal conditions during 50% of the time. The on and off periods shall be initiated by sudden, not gradual, application or removal of input signals and bias voltages. Current limiting resistors may be necessary. Testing at higher/lower temperature shall be performed if necessary according to the time-temperature regression table.

Ref: MIL-STD883E, Method 1006 and MIL-STD883E, Method 1005.8

Modules: Temperature and Power Cycling

* Purpose: The temperature & power cycling test is performed to determine the ability of the modules to withstand alternate exposures at high and low temperatures with operating bias periodically applied and removed.

* Temperature Cycles: -40 deg.C lower temperature, +125 deg.C higher temp.

Transition time 30 minutes max

Dwell time at each temp extreme: 10 minutes min

1000 Cycles

* Power Cycles: switch on/off every 5 minutes

* Failure Criteria: Any exceeding of parametric limits of the electrical or mechanical specifications. Measurements shall be done 5 times in total.

Ref: EIA/JEDEC Standard, Test Method A105-B

References

* Military standards and test methods

o MIL-STD-883E
o Their home page

* JEDEC Standards and test methods

o Their home page

* Proposed set of electrical measurements

Class H

3.2.1.1 b. Scratch in the bonding pad area that both exposes underlying material and reduces the metallization path width, where it enters the bonding pad, to less than 50 percent its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately (see figure 2032-39h).

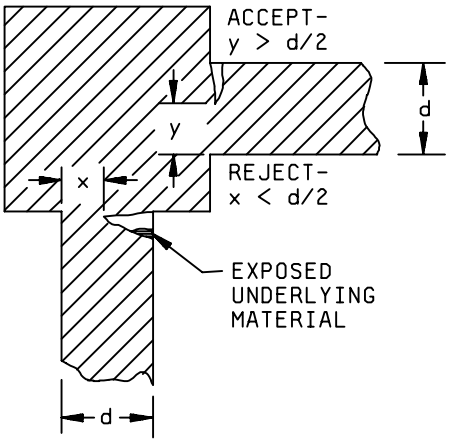


FIGURE 2032-39h. Class H metallization width reduction at bonding pad criteria.

c. Scratch or probe marks in the bonding pad area that expose underlying material over more than 25 percent of the original metallization area.

Class K

3.2.1.1 b. Less than 75 percent (see figure 2032-39k).

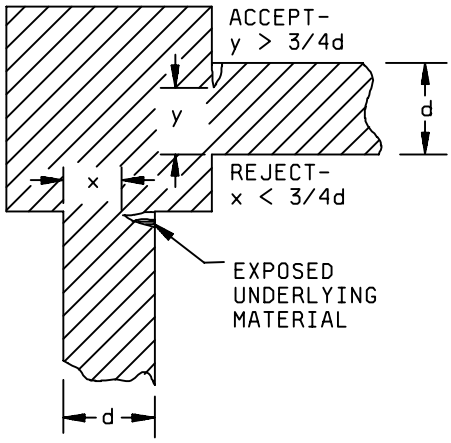


FIGURE 2032-39k. Class K metallization width reduction at bonding pad criteria.

c. Same as class H

3.2 Planar thick film element inspection. Inspection for visual defects described in this section shall be conducted on each planar thick film passive element. All inspection shall be performed at "low magnification" within the range of 10X to 60X magnification for both class H and class K.

Class H	Class K
3.2.1 Operating metallization defects "low magnification". No element shall be acceptable that exhibits: NOTE: The metallization defect criteria contained in this section apply to operating metallization only.	
3.2.1.1 Metallization scratches	
* a. A scratch or probe mark in the metallization, excluding bonding pads, that both exposes underlying material anywhere along its length and leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-38h). NOTE: Underlying material does not have to be exposed along the full length of the scratch. NOTE: This criteria does not apply to capacitors.	a. Same as Class H.

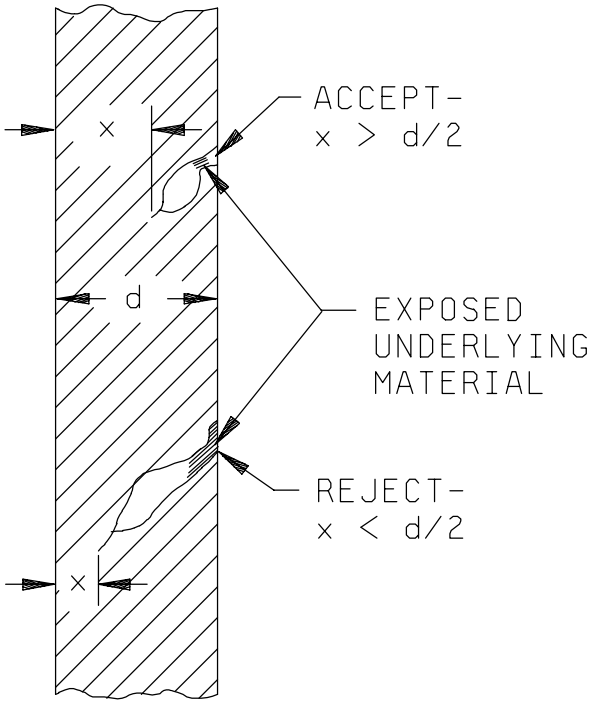


FIGURE 2032-38h. Class H metallization scratch criteria.

	Class H	Class K
3.2.1.2 Metallization voids.		
* a.	Void(s) in the metallization, excluding bonding pads, that leaves less than 50 percent of the original metallization width undisturbed (see figure 2032-40h).	a. Same as Class H.

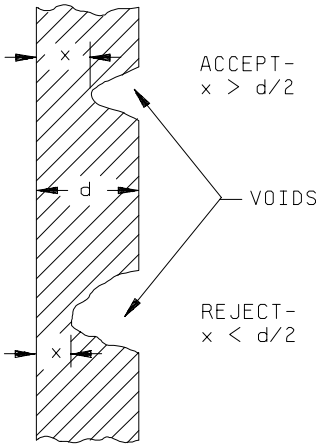


FIGURE 2032-40h. Class H metallization void criteria.

b.	Void(s) in the bonding pad area that reduces the metallization path width, where it enters the bonding pad, to less than 50 percent of its original metallization width. If two or more metallization paths enter a bonding pad, each shall be considered separately. NOTE: Figures 2032-39h and 2032-39k illustrate metallization width reduction at bonding pad criteria for scratches. Void criteria are similar.	b. Less than 75 percent.
c.	Void(s) in the bonding pad area that expose underlying material over more than 25 percent of the original metallization area. NOTE: For RF microwave elements on nonconductive substrates, a void created in the bonding pad area as a result of wire bond removal for performance optimization or tuning, is not rejectable provided that the void remains entirely visible.	c. Same as class H.

	Class H	Class K
3.2.1.6 Metallization overlap.		
	a. Contact overlap between the upper and lower metallizations that is less than 50 percent of the designed contact overlap area (see figure 2032-42h). NOTE: The overlap area is that area in which the upper metallization actually contacts the lower metallization.	a. Same as class H.

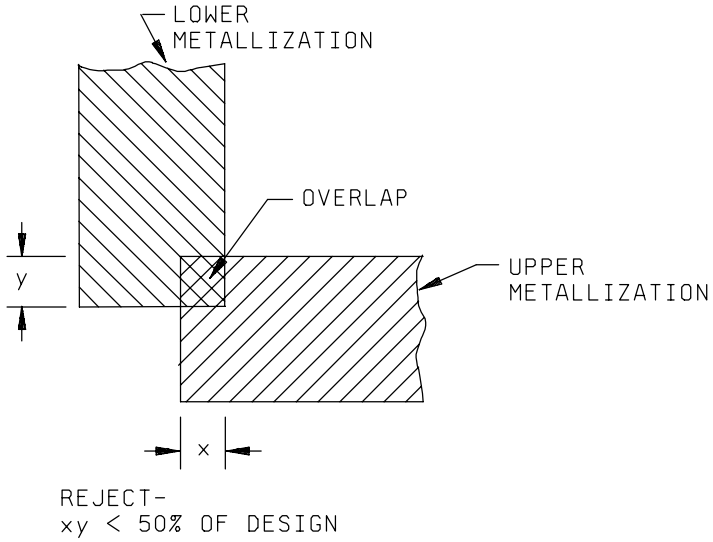


FIGURE 2032-42h. Class H metallization overlap criterion.

	Class H	Class K
3.2.2	Substrate defects, "low magnification". No element shall be acceptable that exhibits:	
	a. Less than 1.0 mil separation between the operating metallization and the edge of the element unless by design (see figure 2032-43h). NOTE: This criterion does not apply to substrates designed for wraparound conductors.	a. Same as class H.
	b. A chipout that extends into the active circuit area (see figure 2032-43h).	b. Same as class H.

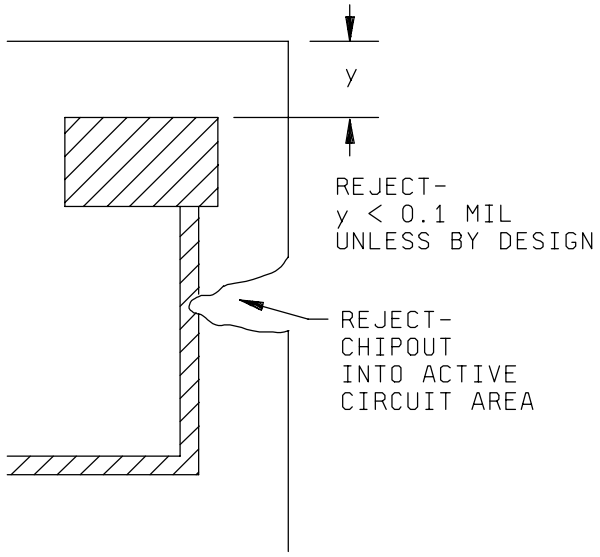


FIGURE 2032-43h. Class H separation and chipout criteria.

*		c. Any crack that exceeds 5.0 mils in length (see figure 2032-44h). NOTE: For fused quart or crystalline substrates, no cracking is allowed.	c. Same as Class H.
		d. Any crack that does not exhibit 1.0 mil of separation from any active circuit area or operating metallization (see figure 2032-44h).	d. Same as class H.

Class H

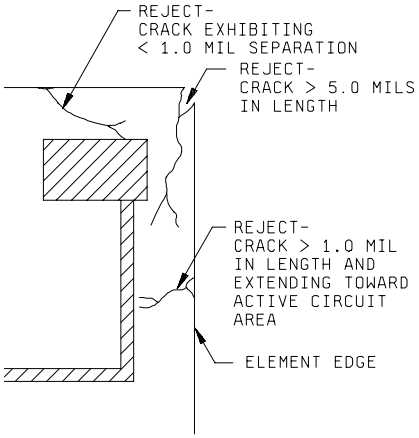


FIGURE 2032-44h. Class H additional crack criteria.

3.2.2 e. Any crack exceeding 1.0 mil in length extending from the element edge directly towards the active circuit area or operating metallization (see figure 2032-44h).

f. N/A

Class K

3.2.2 e. Same as class H.

f. Semicircular crack or combination of cracks along the element edge whose total length is equal to or greater than 75 percent of the narrowest separation between any two bonding pads (see figure 2032-45k).

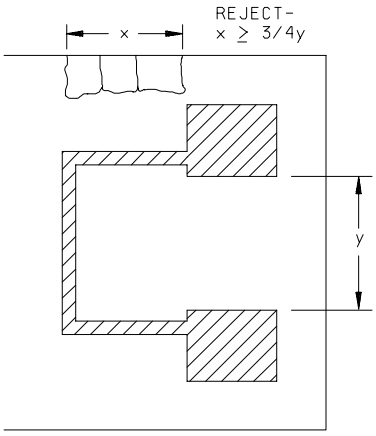


FIGURE 2032-45k. Class K semicircular crack criterion.

		Class H			Class K
3.2.5	b.	Voids in the insulating material that expose underlying metallization.	3.2.5	b.	Same as class H.
	c.	Vias that are less than 50 percent of the original design area.		c.	Same as class H.
	d.	Scratch that completely crosses the metallization and damages the insulating material surface on either side.		d.	Same as class H.

3.2.6 All thin film capacitors and those overlay capacitors used in GaAs microwave devices,"low magnification". No element shall be acceptable that exhibits:

a. Scratches that expose an underlying material.

b. Any peeling or lifting of the metallization.

c. Excess top metal which extend beyond the capacitor bottom metal.

d. Voids in the capacitor bottom metal which extend under the capacitor top metal.

e. Voids in the top metallization which leaves less than 75% of the metallization area undisturbed.

3.3 Nonplanar element inspection. Inspection for visual defects described in this section shall be conducted on each nonplanar passive element. The "low magnification" inspection shall be within the range of 10X to 60X.

		Class H			Class K
3.3.1		General nonplanar element defects, "low magnification". No element shall be acceptable that exhibits:			
	a.	Peeling or lifting of any metallization.		a.	Same as class H.
	b.	Protrusion between metallization terminals that leaves less than 5.0 mils separation (see figure 2032-54h).		b.	Same as class H.

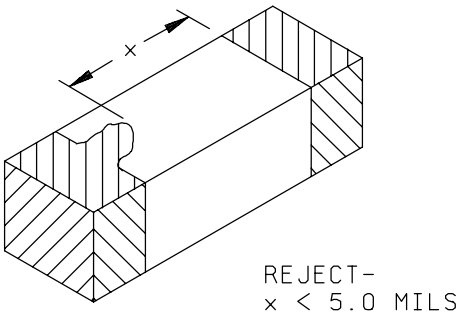


FIGURE 2032-54h. Class H metallization protrusion criterion.

		Class H			Class K
3.3.1	c.	Lifting, blistering, or peeling of insulation.	3.3.1	c.	Same as class H.
	d.	Voids in metallized terminals that expose underlying material over greater than 25 percent of any side of the metallized terminal area.		d.	Same as class H.
3.3.2	Foreign material defects "low magnification". No element shall be acceptable that exhibits:				
	a.	For mounted elements, unattached, conductive foreign material on the surface of the element. For unmounted elements, unattached, conductive foreign material on the surface of the element that is large enough to bridge operating metallization path, active circuitry, or any combination of these. NOTE: If an element has an insulating layer (such as glassivation) that covers operating metallization paths, active circuitry, or any combination of these, then the presence of unattached conductive foreign material that is large enough to bridge these features is acceptable since the features are protected by the insulating layer. NOTE: All foreign material shall be considered to be unattached unless otherwise verified to be attached. Verification of attachment shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.) by a suitable cleaning process approved by the acquiring activity, or by a blow-off with a nominal gas blow (approximately 20 psig). NOTE: Semiconductor particles are considered to be foreign material. NOTE: Removal of unattached foreign material may be attempted using the techniques for verification of attachment discussed above.		a.	Same as class H.
	b.	Attached, conductive foreign material that bridges metallization paths, active circuitry, or any combination of these.		b.	Same as class H.
	c.	Liquid droplets, inkdrops, or any chemical stain that appear to bridge any unglassivated active circuit areas.		c.	Same as class H.
	d.	Attached foreign material that covers more than 25 percent of a bonding pad area.		d.	Same as class H.

	Class H	Class K
3.3.3	Ceramic chip capacitor defects "low magnification". No element shall be acceptable that exhibits:	
	a. Crack, chip or void in the body that exposes metal plates, (see figure 2032-55h).	a. Same as class H.

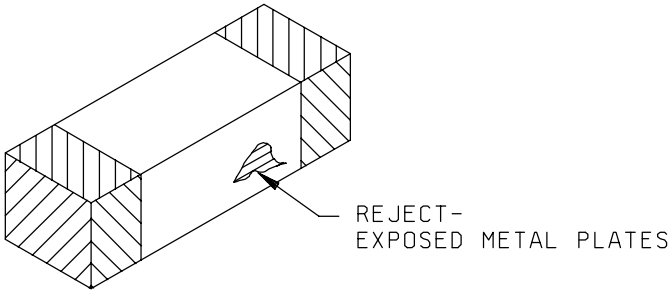


FIGURE 2032-55h. Class H metal plate exposure criteria.

	b. Crack that is greater than 50 percent of the width of the unmetallized sides, top, or bottom, or that extends around a corner (see figure 2032-56h).	b. Crack. NOTE: No cracks are allowed.

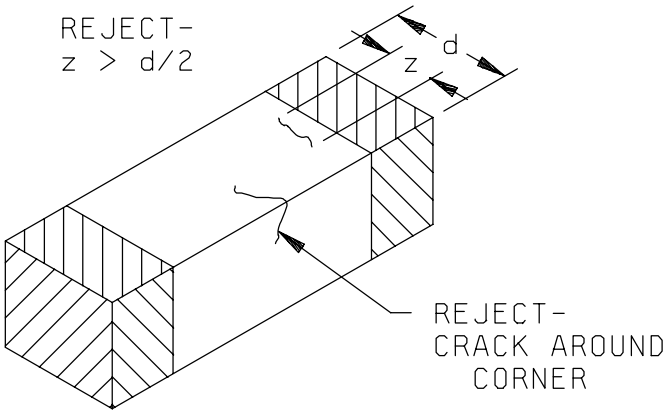


FIGURE 2032-56h. Class H crack criteria.

	Class H	Class K
3.3.3 c.	Evidence of separation (delamination) of metal plates or cracks along the plane of the metal plates (see figure 2032-57h). NOTE: Narrow grooves or channel less than 1.0 mil wide that exhibit a glass-like appearance and do not expose metal plates are acceptable.	3.2.3 c. Delamination. NOTE: No delamination is allowed.

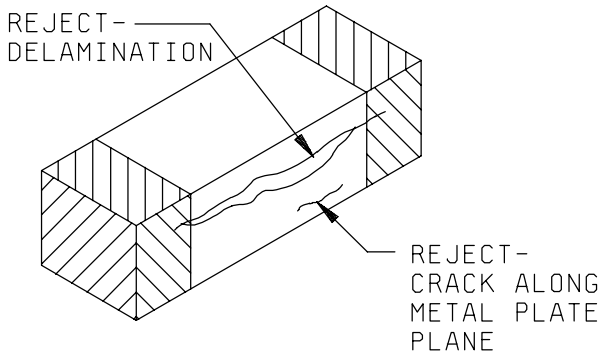


FIGURE 2032-57h. Class H delamination criteria.

d.	Crack or void in the metallization that exposes metal plates, or voids that are greater than 25 percent of the area of the metallized terminal (see figure 2032-58h).	d. Same as class H.

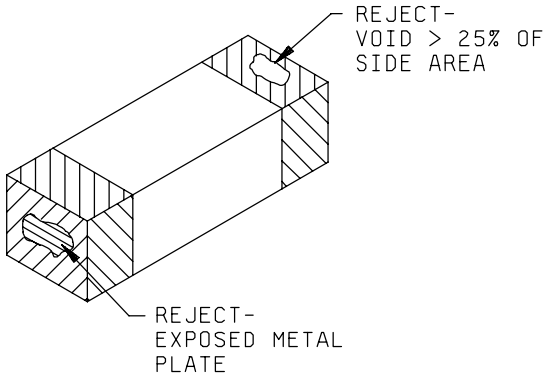


FIGURE 2032-58h. Class H termination defect criteria.

	Class H	Class K
3.3.3 e.	Void in the metallized edges of the element that are greater than 10 percent of the metallized edge dimension, or bare corners of metallized terminals (see figure 2032-59h). NOTE: This criteria ia applicable to solder attached elements only.	3.3.3 e. Same as class H.

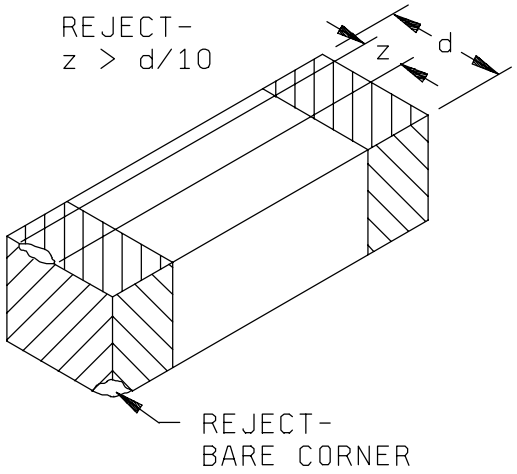


FIGURE 2032-59h. Class H metallized edge defect criteria.

f.	Attached foreign material on the body that covers an area greater than 5.0 mils square on any side.	f. Same as class H.

3.3.4 Tantalum chip capacitor defects, "low magnification." No element shall be acceptable that exhibits:

a.	Flaking or peeling of the encapsulant that exposes any underlying material.	a. Same as class H.
b.	A metallized terminal that is less than 90 percent free of encapsulant material.	b. Same as class H.
c.	Less than 50 percent continuous metallized terminal weld area without cracks.	c. Same as class H.
d.	Metallized terminal containing residue from the welding operation that is not firmly attached metallurgically to the anode cap.	d. Same as class H.

		Class H		Class K
3.3.4	e.	Metallized terminal not aligned as shown in the applicable drawing.	3.3.4	e. Same as class H.
	f.	Encapsulant preventing the metallized terminal from resting on the substrate bonding pads when the capacitor is in the bonding position except where the metallized terminal electrical contact is made by alternate means.		f. Same as class H.
	g.	Lifting, blistering or peeling of metallized terminal encapsulant.		g. Same as class H.
3.3.5	Parallel plate chip capacitor defects, "low magnification". No element shall be acceptable that exhibits:			
	a.	Metallization that extends greater than 50 percent around the edge of the capacitor (see figure 2032-60h).		a. Same as class H.

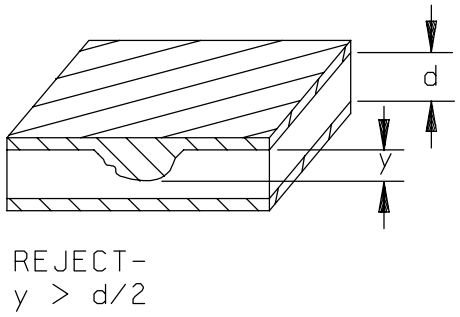


FIGURE 2032-60h. Class H metallization extension criterion.

3.3.5	b.	Evidence of cracks in the dielectric body (see figure 2032-61h).	3.3.5	b. Same as class H.

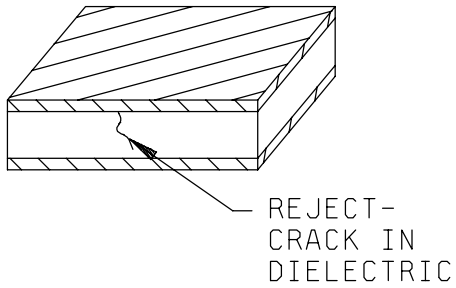


FIGURE 2032-61h. Class H crack in dielectric criterion.

3.3.6 Inductor and transformer defects, "low magnification". No element shall be acceptable that exhibits:		
	a. Peeling, lifting or blistering of winding metallization or insulation.	a. Same as class H.
	b. Evidence of shorts between adjacent turns or windings.	b. Same as class H.
	c. Cracks or exposure of bare magnetic core material.	c. Same as class H.
	d. Pits or voids in the core insulation greater than 5.0 mils area that expose the magnetic core material.	d. Same as class H.
	e. Separation less than 5.0 mils between wire termination points of the same or adjacent windings.	e. Same as class H.
	f. Missing polarity identification unless by design.	f. Same as class H.
	g. Operating metallization and multilevel thick film defects as described in 3.2.1 and 3.2.5 herein.	g. Same as class H.
3.3.7 Chip resistor defects, "low magnification". No element shall be acceptable that exhibits:		
	a. Reduction of the resistor width resulting from voids, bubbles, nicks, or scratches, or a combination of these, that leaves less than 50 percent of the narrowest resistor width (see figure 2032-62h).	a. Same as class H.

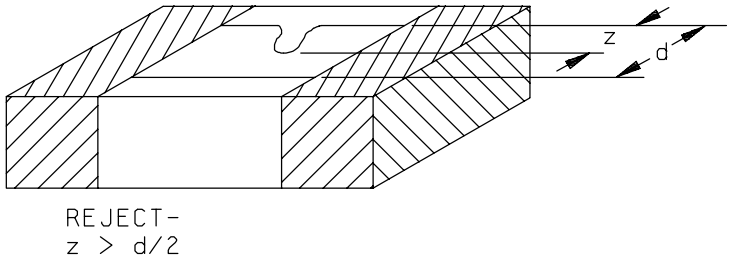


FIGURE 2032-62h. Class H resistor width reduction criterion.

			Class H		Class K
*	3.3.7	b.	A kerf that leaves less than 50 percent of the original width of the resistor unless by design.	3.3.7 b.	Same as class H.
		c.	Metallized termination width less than 10.0 mils unless by design (see figure 2032-63h).	c.	Same as class H.

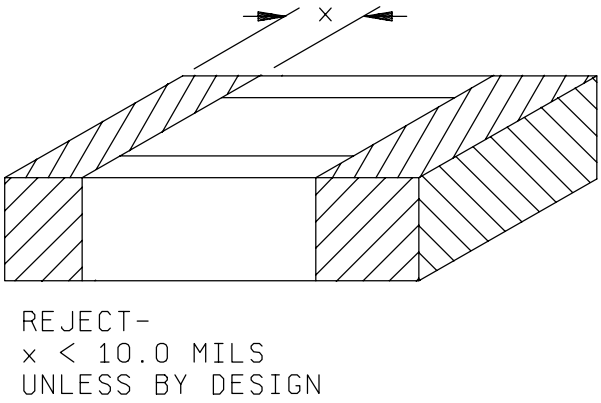


FIGURE 2032-63h. Class H termination width criterion.

		d.	A crack, chipout or void in the substrate greater than 3.0 mils in any direction (see figure 2032-64h).	d.	Same as class H.

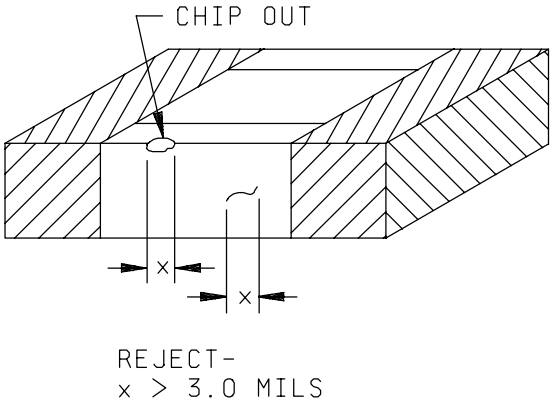


FIGURE 2032-64h. Class H substrate defect criteria.

	Class H	Class K
3.3.7 e.	Build-up of termination material on metallized termination areas greater than 3.0 mils high for weldable metallized terminations or 8.0 mils high for solderable metallized terminations (see figure 2032-65h).	Same as class H.

FIGURE 2032-65h. Class H termination material buildup criteria.

	Class H	Class K
f.	Termination material splattered throughout the resistor (see figure 2032-66h).	Same as class H.

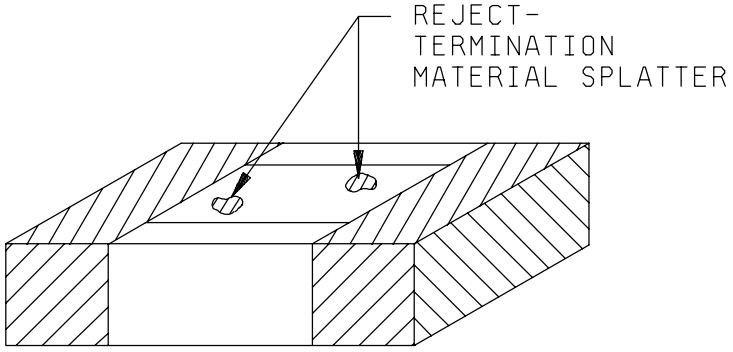


FIGURE 2032-66h. Class H termination material splatter criteria.

METHOD 2011.7

BOND STRENGTH (DESTRUCTIVE BOND PULL TEST)

1. PURPOSE. The purpose of this test is to measure bond strengths, evaluate bond strength distributions, or determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermocompression, ultrasonic, or related techniques. It may also be applied to bonds external to the device such as those from device terminals-to-substrate or wiring board or to internal bonds between die and substrate in non-wire-bonded device configurations such as beam lead or flip chip devices.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for applying the specified stress to the bond, lead wire or terminal as required in the specified test condition. A calibrated measurement and indication of the applied stress in grams force (gf) shall be provided by equipment capable of measuring stresses up to twice the specified minimum limit value, with an accuracy of ±5 percent or ±0.25 gf, whichever is the greater tolerance.

3. PROCEDURE. The test shall be conducted using the test condition specified in the applicable acquisition document consistent with the particular device construction. All bond pulls shall be counted and the specified sampling, acceptance, and added sample provisions shall be observed, as applicable. Unless otherwise specified, for conditions A, C, and D, the sample size number specified for the bond strength test shall determine the minimum sample size in terms of the minimum number of bond pulls to be accomplished rather than the number of complete devices in the sample, except that the required number of bond pulls shall be randomly selected from a minimum of 4 devices. Bond pulls in accordance with test conditions D, F, G, and H, while involving two or more bonds shall count as a single pull for bond strength and sample size number purposes. Unless otherwise specified, for conditions F, G, and H the sample size number specified shall determine the number of die to be tested (not bonds). For hybrid or multichip devices (all conditions), a minimum of 4 die or use all die if four are not available on a minimum of 2 completed devices shall be used. Where there is any adhesive, encapsulant or other material under, on or surrounding the die such as to increase the apparent bond strength, the bond strength test shall be performed prior to application.

When flip chip or beam-lead chips are bonded to substrates other than those in completed devices, the following conditions shall apply:

a. The sample of chips for this test shall be taken at random from the same chip population as that used in the completed devices that they are intended to represent.

b. The chips for this test shall be bonded on the same bonding apparatus as the completed devices, during the time period within which the completed devices are bonded.

c. The test chip substrates shall be processed, metallized, and handled identically with the completed device substrates, during the same time period within which the completed device substrates are processed.

3.1 Test conditions:

3.1.1 Test condition A - Bond peel. This test is normally employed for bonds external to the device package. The lead or terminal and the device package shall be gripped or clamped in such a manner that a peeling stress is exerted with the specified angle between the lead or terminal and the board or substrate. Unless otherwise specified, an angle of 90 degrees shall be used. When a failure occurs, the force causing the failure and the failure category shall be recorded.

3.1.2 Test condition C - Wire pull (single bond). This test is normally employed for internal bonds at the die or substrate and the lead frame of microelectronic devices. The wire connecting the die or substrate shall be cut so as to provide two ends accessible for pull test. In the case of short wire runs, it may be necessary to cut the wire close to one termination in order to allow pull test at the opposite termination. The wire shall be gripped in a suitable device and simple pulling action applied to the wire or to the device (with the wire clamped) in such a manner that the force is applied approximately normal to the surface of the die or substrate. When a failure occurs, the force causing the failure and the failure category shall be recorded.

3.1.3 Test condition D - Wire pull (double bond). This procedure is identical to that of test condition C, except that the pull is applied by inserting a hook under the lead wire (attached to die, substrate or header or both ends) with the device clamped and the pulling force applied approximately in the center of the wire in a direction approximately normal to the die or substrate surface or approximately normal to a straight line between the bonds. When a failure occurs, the force causing the failure and the failure category shall be recorded. The minimum bond strength shall be taken from table I. Figure 2011-1 may be used for wire diameters not specified in table I. For wire diameter or equivalent cross section >0.005 inch, where a hook will not fit under the wire, a suitable clamp can be used in lieu of a hook.

3.1.4 Test condition F - Bond shear (flip chip). This test is normally employed for internal bonds between a semiconductor die and a substrate to which it is attached in a face-bonded configuration. It may also be used to test the bonds between a substrate and an intermediate carrier or secondary substrate to which the die is mounted. A suitable tool or wedge shall be brought in contact with the die (or carrier) at a point just above the primary substrate and a force applied perpendicular to one edge of the die (or carrier) and parallel to the primary substrate, to cause bond failure by shear. When a failure occurs, the force at the time of failure, and the failure category shall be recorded.

3.1.5 Test condition G - Push-off test (beam lead). This test is normally employed for process control and is used on a sample of semiconductor die bonded to a specially prepared substrate. Therefore, it cannot be used for random sampling of production or inspection lots. A metallized substrate containing a hole shall be employed. The hole appropriately centered, shall be sufficiently large to provide clearance for a push tool, but not large enough to interfere with the bonding areas. The push tool shall be sufficiently large to minimize device cracking during testing, but not large enough to contact the beam leads in the anchor bond area. Proceed with push-off tests as follows: The substrate shall be rigidly held and the push tool inserted through the hole. The contact of the push tool to the silicon device shall be made without appreciable impact (less than 0.01 inch/minute (0.254 mm/minute) and forced against the underside of the bonded device at a constant rate. When failure occurs, the force at the time of failure, and the failure category shall be recorded.

3.1.6 Test condition H - Pull-off test (beam lead). This test is normally employed on a sample basis on beam lead devices which have been bonded down on a ceramic or other suitable substrate. The calibrated pull-off apparatus (see 2) shall include a pull-off rod (for instance, a current loop of nichrome or Kovar wire) to make connection with a hard setting adhesive material (for instance, heat sensitive polyvinyl acetate resin glue) on the back (top side) of the beam lead die. The substrate shall be rigidly installed in the pull-off fixture and the pull-off rod shall make firm mechanical connection to the adhesive material. The device shall be pulled within 5 degrees of the normal to at least the calculated force (see 3.2), or until the die is at 2.54 mm (0.10 inch) above the substrate. When a failure occurs, the force at the time of failure, the calculated force limit, and the failure category shall be recorded.

3.2 Failure criteria. Any bond pull which results in separation under an applied stress less than that indicated in table I as the required minimum bond strength for the indicated test condition, composition, and construction shall constitute a failure.

3.2.1 Failure category. Failure categories are as follows: When specified, the stress required to achieve separation and the category of separation or failure shall be recorded.

a. For internal wire bonds:

(a-1) Wire break at neckdown point (reduction of cross section due to bonding process).

(a-2) Wire break at point other than neckdown.

(a-3) Failure in bond (interface between wire and metallization) at die.

(a-4) Failure in bond (interface between wire and metallization) at substrate, package post, or other than die.

(a-5) Lifted metallization from die.

(a-6) Lifted metallization from substrate or package post.

(a-7) Fracture of die.

(a-8) Fracture of substrate.

b. For external bonds connecting device to wiring board or substrate:

(b-1) Lead or terminal break at deformation point (weld affected region).

(b-2) Lead or terminal break at point not affected by bonding process.

(b-3) Failure in bond interface (in solder or at point of weld interface between lead or terminal and the board or substrate conductor to which the bond was made).

(b-4) Conductor lifted from board or substrate.

(b-5) Fracture within board or substrate.

c. For flip-chip configurations:

(c-1) Failure in the bond material or pedestal, if applicable.

(c-2) Fracture of die (or carrier) or substrate (removal of portion of die or substrate immediately under the bond).

(c-3) Lifted metallization (separation of metallization or bonding pedestal from die (or carrier) or substrate.

d. For beam lead devices:

(d-1) Silicon broken.

(d-2) Beam lifting on silicon.

(d-3) Beam broken at bond.

(d-4) Beam broken at edge of silicon.

(d-5) Beam broken between bond and edge of silicon.

(d-6) Bond lifted.

(d-7) Lifted metallization (separation of metallization) from die, separation of bonding pad.

(d-8) Lifted metallization.

NOTE: RF/microwave hybrids that require extremely flat loops which may cause erroneous wire pull data may use the following formula to determine the proper wire pull value.

$$V_1 = V_2 \sin \Theta$$

Where: V_1 = New value to pull test.
V_2 = Table I value for size wire tested.
Θ = Greatest calculated wire loop angle (figure 2011-2).

Also, RF/microwave hybrids that contain wires that cannot be accessed with a pull hook must be duplicated on a test coupon in such a way to allow hook access for purposes of pull testing. These wires are to be bonded at the same time the production hybrids are bonded using the same setup, operator, and schedule. The test coupon wires are to be pull tested in lieu of the tuning or inaccessible wires on the production hybrid. Failures on the test coupon shall be considered as failures to production units and appropriate action is to be taken in accordance with the applicable specification (figure 2011-3).

TABLE I. Minimum bond strength.

Test condition	Wire composition and diameter 1/	Construction 2/	Minimum bond strength (grams force)	
			Pre seal	Post seal and any other processing and screening when applicable
A	---	---	Given in applicable document	Given in applicable document
C or D	AL 0.0007 in AU 0.0007 in	Wire	1.5 2.0	1.0 1.5
C or D	AL 0.0010 in AU 0.0010 in	Wire	2.5 3.0	1.5 2.5
C or D	AL 0.00125 in AU 0.00125 in	Wire	Same bond strength limits as the 0.0013 in wire	
C or D	AL 0.0013 in AU 0.0013 in	Wire	3.0 4.0	2.0 3.0
C or D	AL 0.0015 in AU 0.0015 in	Wire	4.0 5.0	2.5 4.0
C or D	AL 0.0030 in AU 0.0030 in	Wire	12.0 15.0	8.0 12.0
F	Any	Flip-clip	5 grams-force x number of bonds (bumps)	
G or H	Any	Beam lead	30 grams force in accordance with linear millimeter of nominal undeformed (before bonding) beam width. 3/	

1/ For wire diameters not specified, use the curve of figure 2011-1 to determine the bond pull limit.
2/ For ribbon wire, use the equivalent round wire diameter which gives the same cross-sectional area as the ribbon wire being tested.
3/ For condition G or H, the bond strength shall be determined by dividing the breaking force by the total of the nominal beam widths before bonding.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

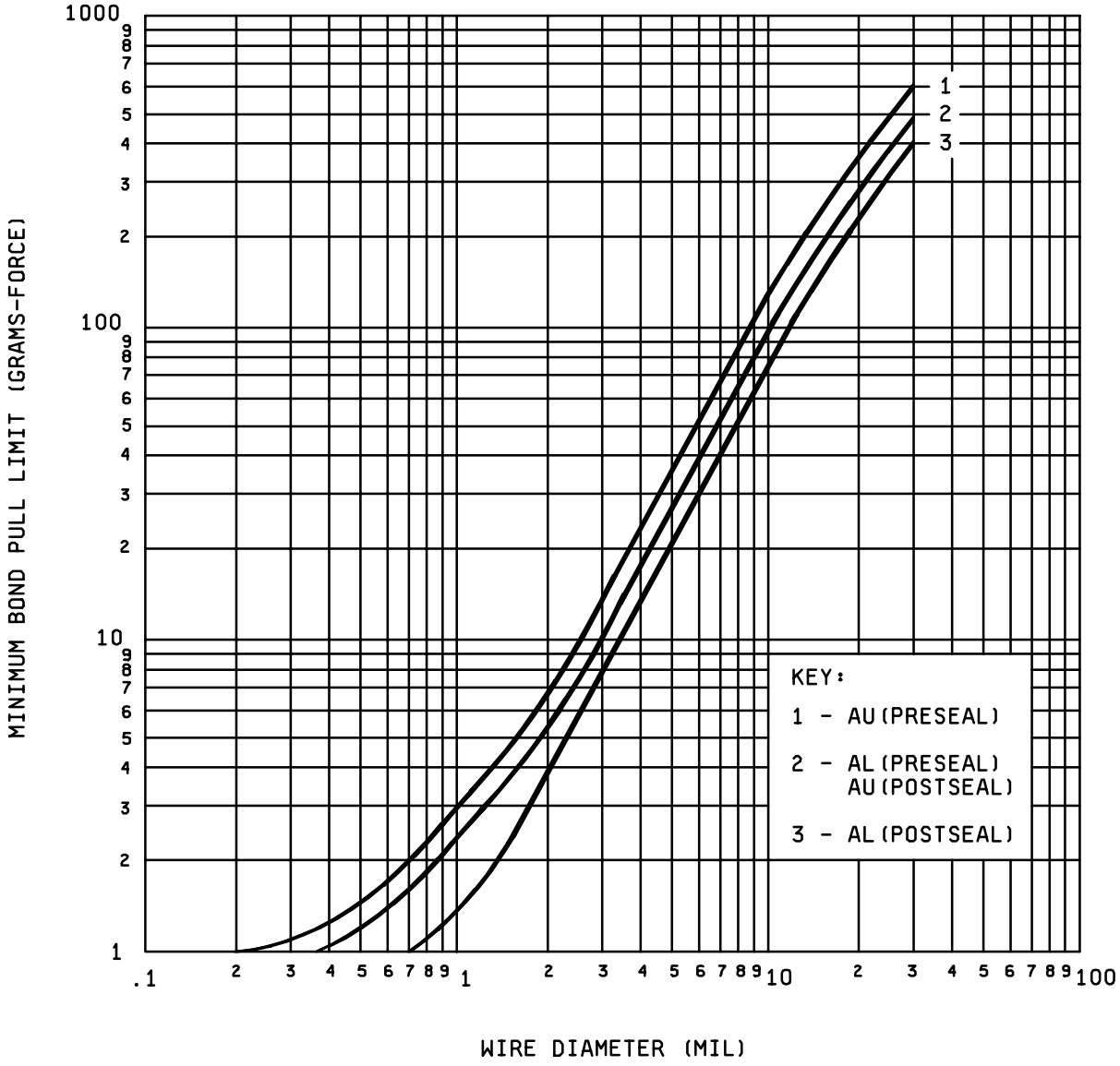
a. Test condition letter (see 3).

b. Minimum bond strength if other than specified in 3.2 or details of required strength distributions if applicable.

* c. Sample size number and accept number or number and selection of bond pulls to be tested on each device, and number of devices, if other than 4.

d. For test condition A, angle of bond peel if other than 90°, and bond strength limit (see 3.2).

e. Requirement for reporting of separation forces and failure categories, when applicable (see 3.2.1).



NOTE: The minimum bond strength should be taken from table I. Figure 2011-1 may be used for wire diameters not specified in table I.

FIGURE 2011-1. Minimum bond pull limits.

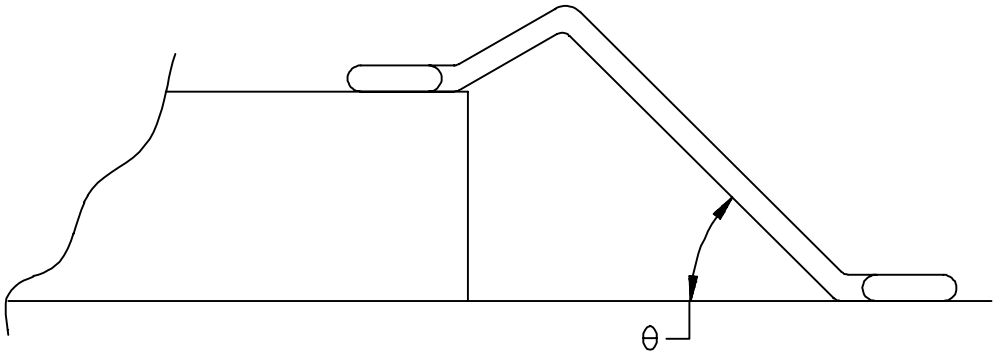


FIGURE 2011-2. Wire loop angle.

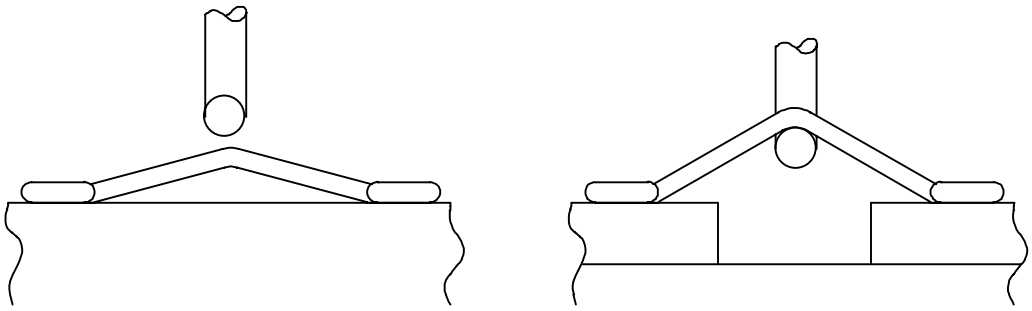


FIGURE 2011-3. Flat loop wire pull testing.

METHOD 1005.8

STEADY-STATE LIFE

1. PURPOSE. The steady-state life test is performed for the purpose of demonstrating the quality or reliability of devices subjected to the specified conditions over an extended time period. Life tests conducted within rated operating conditions should be conducted for a sufficiently long test period to assure that results are not characteristic of early failures or "infant mortality," and periodic observations of results should be made prior to the end of the life test to provide an indication of any significant variation of failure rate with time. Valid results at shorter intervals or at lower stresses require accelerated test conditions or a sufficiently large sample size to provide a reasonable probability of detection of failures in the sample corresponding to the distribution of potential failures in the lot(s) from which the sample was drawn. The test conditions provided in 3 below are intended to reflect these considerations.

When this test is employed for the purpose of assessing the general capability of a device or for device qualification tests in support of future device applications requiring high reliability, the test conditions should be selected so as to represent the maximum operating or testing (see test condition F) ratings of the device in terms of electrical input(s), load and bias and the corresponding maximum operating or testing temperature or other specified environment.

2. APPARATUS. Suitable sockets or other mounting means shall be provided to make firm electrical contact to the terminals of devices under test in the specified circuit configuration. Except as authorized by the acquiring or qualifying activity, the mounting means shall be so designated that they will not remove internally-dissipated heat from the device by conduction, other than that removed through the device terminals, the necessary electrical contacts and the gas or liquid chamber medium. The apparatus shall provide for maintaining the specified biases at the terminals of the device under test and, when specified, monitoring of the input excitation or output response. Power supplies and current-setting resistors shall be capable of maintaining the specified operating conditions as minimal throughout the testing period, despite normal variations in source voltages, ambient temperatures, etc. When test conditions result in significant power dissipation, the test apparatus shall be arranged so as to result in the approximate average power dissipation for each device whether devices are tested individually or in a group. The test circuits need not compensate for normal variations in individual device characteristics, but shall be so arranged that the existence of failed or abnormal (i.e., open, short, etc.) devices in a group does not negate the effect of the test for other devices in the group.

* 3. PROCEDURE. The microelectronic devices shall be subjected to the specified test condition (see 3.5) for the specified duration at the specified test temperature, and the required measurements shall be made at the specified intermediate points and end points. QML manufactures who are certified and qualified to MIL-PRF-38535 may modify the time or the condition independently from the regression conditions contained in table I or the test condition/circuit specified in the device specification or standard microcircuit drawing provided the modification is contained in the manufacturer's QM plan and the "Q" certification identifier is marked on the devices. Lead-, stud-, or case-mounted devices shall be mounted by the leads, stud, or case in their normal mounting configuration, and the point of connection shall be maintained at a temperature not less than the specified ambient temperature. The test condition, duration, sample size, and temperature selected prior to test shall be recorded and shall govern for the entire test. Test boards shall not employ load resistors which are common to more than one device, or to more than one output pin on the same device.

3.1 Test duration.

3.1.1 Test duration - standard life. The life test duration shall be 1,000 hours minimum at 125°C , unless otherwise specified or allowed (see 3.2.1). After the specified duration of the test, the device shall be removed from the test conditions and allowed to reach standard test conditions. Where the purpose of this test is to demonstrate compliance with a specified lambda (8), the test may be terminated at the specified duration or at the point of rejection if this occurs prior to the specified test duration.

* 3.1.2 Accelerated life test duration. For class level B, the life test duration, when accelerated, shall be the time equivalent to 1,000 hours at 125°C for the ambient temperature selected or specified (see table I). Within 72 hours after the specified duration of the test, the device shall be removed from the specified test conditions and allowed to reach standard test conditions without removal of bias. The interruption of bias for up to one minute for the purpose of moving the devices to cool-down positions separate from the chamber within which life testing was performed shall not be considered removal of bias.

3.2 Test temperature. The specified test temperature is the minimum ambient temperature to which all devices in the working area of the chamber shall be exposed. This shall be assured by making whatever adjustments are necessary in the chamber profile, loading, location of control or monitoring instruments, and the flow of air or other suitable gas or liquid chamber medium. Therefore, calibration shall be accomplished in the chamber in a fully loaded, (boards need not be loaded with devices) unpowered configuration, and the indicator sensor located at, or adjusted to reflect, the coldest point in the working area.

* 3.2.1 Test temperature - standard life. Unless otherwise specified, the ambient life test temperature shall be 125°C minimum for test conditions A through E (see 3.5), except that for hybrid microcircuits, the conditions may be modified in accordance with table I. At the supplier's option, the ambient temperature for conditions A through E may be increased and the test duration reduced in accordance with table I using the specified test circuit and bias conditions. Since case and junction temperature will, under normal circumstances, be significantly higher than ambient temperature, the circuit should be so structured that maximum rated case or junction temperatures for test or operation shall not exceed 200°C for class level B or 175°C for class level S (see 3.2.1.1).

* 3.2.1.1 Test temperature for high power devices. Regardless of power level, devices shall be able to be burned in or life-tested at their maximum rated operating temperature. For devices whose maximum operating temperature is stated in terms of ambient temperature, T_A, table I applies. For devices whose maximum operating temperature is stated in terms of case temperature, T_C, and where the ambient temperature would cause T_J to exceed +200°C (+175°C for class level S), the ambient operating temperature may be reduced during burn-in and life test from +125°C to a value that will demonstrate a T_J between +175°C and +200°C and T_C equal to or greater than +125°C without changing the test duration. Data supporting this reduction shall be available to the acquiring and qualifying activities upon request.

* 3.2.1.2 Test temperature for hybrid devices. The ambient or case life test temperature shall be as specified in table I, except case temperature life test shall be performed, as a minimum, at the maximum operating case temperature (T_C) specified for the device. Life test shall be for 1,000 hours minimum for class level S hybrid (class K). The device should be life tested at the maximum specified operating temperature, voltage, and loading conditions as specified in the detail specification. Since case and junction temperature will, under normal circumstances, be significantly higher than ambient temperature, the circuit should be so structured that the maximum rated junction temperature as specified in the device specification or drawing and the cure temperature of polymeric materials as specified in the baseline documentation shall not be exceeded. If no maximum junction temperature is specified, a maximum of 175°C is assumed. Accelerated life test (condition F) shall not be permitted. The specified test temperature shall be the minimum actual ambient or case temperature that must be maintained for all devices in the chamber. This shall be assured by making whatever adjustments are necessary in the chamber profile, loading, location of control or monitoring instruments and the flow of air or other suitable gas or liquid chamber medium.

3.2.2 Test temperature - accelerated life. When condition F is specified or is utilized as an option (when allowed by the applicable acquisition documents), the minimum ambient test temperature shall be +175°C , unless otherwise specified. Since accelerated testing will normally be performed at temperatures higher than the maximum rated operating junction temperature of the device(s) tested, care shall be taken to ensure that the device(s) does not go into thermal runaway.

3.2.3 Special considerations for devices with internal thermal limitation using test conditions A through E. For devices with internal thermal shutdown, extended exposure at a temperature in excess of the shut-down temperature will not provide a realistic indicator of long-term operating reliability. For devices equipped with thermal shutdown, operating life test shall be performed at an ambient temperature where the worst case junction temperature is at least 5°C below the worst case thermal shutdown threshold. Data supporting the defined thermal shutdown threshold shall be available to the preparing or acquiring activity upon request.

3.3 Measurements.

3.3.1 Measurements for test temperatures less than or equal to 150°C . Unless otherwise specified, all specified intermediate and end-point measurements shall be completed within 96 hours after removal of the device from the specified test conditions (i.e., either removal of temperature or bias). If these measurements cannot be completed within 96 hours, the devices shall be subjected to the same test condition (see 3.5) and temperature previously used for a minimum of 24 additional hours before intermediate or end-point measurements are made. When specified (or at the manufacturer's discretion, if not specified), intermediate measurements shall be made at 168 (+72, -0) hours and at 504 (+168, -0) hours. For tests in excess of 1,000 hours duration, additional intermediate measurement points, when specified, shall be 1000 (+168, -24) hours, 2,000 (+168, -24) hours, and each succeeding 1,000 (+168, -24) hour interval. These intermediate measurements shall consist of the parameters and conditions specified, including major functional characteristics of the device under test, sufficient to reveal both catastrophic and degradation failures to specified limits. Devices shall be cooled to less than 10°C of their power stable condition at room temperature prior to the removal of bias.

The interruption of bias for up to one minute for the purpose of moving the devices to cool-down positions separate from the chamber within which life testing was performed shall not be considered removal of bias. Alternatively, except for linear or MOS (CMOS, NMOS, PMOS, etc.) devices or unless otherwise specified, the bias may be removed during cooling, provided the case temperature of the devices under test is reduced to a maximum of 35°C within 30 minutes after removal of the test conditions and provided the devices under test are removed from the heated chamber within five minutes following removal of bias. All specified 25°C electrical measurements shall be completed prior to any reheating of the device(s).

3.3.2 Measurements for test temperatures greater than or equal to 175°C . Unless otherwise specified, all specified intermediate and end-point measurements shall be completed within 24 hours after removal of the device from the specified test conditions (i.e., either removal of temperature or bias). If these measurements cannot be completed within 24 hours, the steady-state life test shall be repeated using the same test condition, temperature and time. Devices shall be cooled to less than 10°C of their power stable condition at room temperature prior to the removal of bias, except that the interruption of bias for up to one minute for the purpose of moving the devices to cool-down positions shall not be considered removal of bias. All specified 25°C electrical measurements shall be completed prior to any reheating of the device(s).

3.3.3 Test setup monitoring. The test setup shall be monitored at the test temperature initially and at the conclusion of the test to establish that all devices are being stressed to the specified requirements. The following is the minimum acceptable monitoring procedure:

a. Device sockets. Initially and at least each 6 months thereafter, (once every 6 months or just prior to use if not used during the 6 month period) each test board or tray shall be checked to verify continuity to connector points to assure that bias supplies and signal information will be applied to each socket. Board capacitance or resistance required to ensure stability of devices under test shall be checked during these initial and periodic verification tests to ensure they will perform their proper function (i.e., that they are not open or shorted). Except for this initial and periodic verification, each device or device socket does not have to be checked; however, random sampling techniques shall be applied prior to each time a board is used and shall be adequate to assure that there are correct and continuous electrical connections to the devices under test.

b. Connectors to test boards or trays. After the test boards are loaded with devices, inserted into the oven, and brought up to at least 125°C or the specified test temperature, whichever is less, each required test voltage and signal condition shall be verified in at least one location on each test board or tray so as to assure electrical continuity and the correct application of specified electrical stresses for each connection or contact pair used in the applicable test configuration. This may be performed by opening the oven for a maximum of 10 minutes. When the test conditions are checked at a test socket, contact points on the instrument used to make this continuity check shall be equal to or smaller dimensions than the leads (contacts) of the devices to be tested and shall be constructed such that the socket contacts are not disfigured or damaged.

c. At the conclusion of the test period, prior to removal of devices from temperature and test conditions, the voltage and signal condition verification of b. above shall be repeated.

* d. For class level S devices, each test board or tray and each test socket shall be verified prior to test to assure that the specified test conditions are applied to each device. This may be accomplished by verifying the device functional response at each device output(s). An approved alternate procedure may be used.

Where failures or open contacts occur which result in removal of the required test stresses for any period of the required test duration (see 3.1), the test time shall be extended to assure actual exposure for the total minimum specified test duration. Any loss(es) or interruption(s) of bias in excess of 10 minutes total duration whether or not the chamber is at temperature during the final 24 hours of life test shall require extension of the test duration for an uninterrupted 24 hours minimum, after the last bias interruption.

3.4 Test sample. The test sample shall be as specified (see 4). When this test method is employed as an add-on life test for a series or family of device types, lesser quantities of any single device type may be introduced in any single addition to the total sample quantity, but the results shall not be considered valid until the minimum sample size for each device has been accumulated. Where all or part of the samples previously under test are extracted upon addition of new samples, the minimum sample size for each type shall be maintained once that level is initially reached and no sample shall be extracted until it has accumulated the specified minimum test hours (see 3.1).

3.5 Test conditions.

3.5.1 Test condition A, steady-state, reverse bias. This condition is illustrated on figure 1005-1 and is suitable for use on all types of circuits, both linear and digital. In this test, as many junctions as possible will be reverse biased to the specified voltage.

3.5.2 Test condition B, steady-state, forward bias. This test condition is illustrated on figure 1005-1 and can be used on all digital type circuits and some linear types. In this test, as many junctions as possible will be forward biased as specified.

3.5.3 Test condition C, steady-state, power and reverse bias. This condition is illustrated on figure 1005-1 and can be used on all digital type circuits and some linear types where the inputs can be reverse biased and the output can be biased for maximum power dissipation or vice versa.

3.5.4 Test condition D, parallel excitation. This test condition is typically illustrated on figure 1005-2 and is suitable for use on all circuit types. All circuits must be driven with an appropriate signal to simulate, as closely as possible, circuit application and all circuits shall have maximum load applied. The excitation frequency shall not be less than 60 Hz.

3.5.5 Test condition E, ring oscillator. This test condition is illustrated on figure 1005-3, with the output of the last circuit normally connected to the input of the first circuit. The series will be free running at a frequency established by the propagation delay of each circuit and associated wiring and the frequency shall not be less than 60 Hz. In the case of circuits which cause phase inversion, an odd number of circuits shall be used. Each circuit in the ring shall be loaded to its rated maximum. While this condition affords the opportunity to continuously monitor the test for catastrophic failures (i.e., ring stoppage), this shall not be considered acceptable as a substitute for the intermediate measurements (see 3.3).

* 3.5.6 Test condition F, (class level B only) temperature-accelerated test. In this test condition, microcircuits are subjected to bias(es) at an ambient test temperature (175°C to 300°C) which considerably exceeds their maximum rated temperature. At higher temperatures, it is generally found that microcircuits will not operate normally, and it is therefore necessary that special attention be given to the choice of bias circuits and conditions to assure that important circuit areas are adequately biased without damaging overstresses to other areas of the circuit. To properly select the actual biasing conditions to be used, it is recommended that an adequate sample of devices be exposed to the intended high temperature while measuring voltage(s) and current(s) at each device terminal to assure that the specified circuit and the applied electrical stresses do not induce damaging overstresses.

At the manufacturer's option, alternate time and temperature values may be established from table I. Any time-temperature combination which is contained in table I within the time limit of 30 to 1,000 hours may be used. The life test ground rules of 3.5 of method 1016 shall apply to life tests conducted using test condition F. The applied voltage at any or all terminals shall be equal to the voltage specified for the 125°C operating life in the applicable acquisition document, unless otherwise specified.

If necessary, with the specific approval of the qualifying activity, the applied voltage at any or all terminal(s) may be reduced to not less than 50 percent of the specified value(s) when it is demonstrated that excessive current flow or power dissipation would result from operation at the specified voltage(s). If the voltage(s) is so reduced, the life test duration shall be determined by the following formula:

$$T_a = \frac{t_o\,(100\%)}{100\% - V\%}$$

Where T_a is the adjusted total test duration in hours, t_o is the original test duration in hours, and V percent is the largest percentage of voltage reduction made in any specified voltage.

* 3.5.6.1 Special considerations for devices with internal thermal limitation. For devices with internal thermal shutdown, extended exposure at a temperature in excess of the shut-down temperature will not provide a realistic indicator of long-term operating reliability. For such devices, measurement of the case temperature should be made at the specified bias voltages at several different ambient temperatures. From these measurements, junction temperatures should be computed, and the operating life shall be performed at that ambient temperature which, with the voltage biases specified, will result in a worst case junction temperature at least 5°C but no more than 10°C below the minimum junction temperature at which the device would go into thermal shutdown, and the test time shall be determined from table I for the applicable device class level.

4. SUMMARY. The following details shall be specified in the applicable acquisition document:

a. Special preconditioning, when applicable.

b. Test temperature, and whether ambient, junction, or case, if other than as specified in 3.2.

c. Test duration, if other than as specified in 3.1.

d. Test mounting, if other than normal (see 3).

e. Test condition letter.

f. End-point measurements and intermediate measurements (see 3.3).

g. Criteria for device failure for intermediate and end-point measurements (see 3.3), if other than device specification limits, and criteria for lot acceptance.

h. Test sample (see 3.4).

i. Time to complete end-point measurements, if other than as specified (see 3.3).

j. Authorization for use of condition F and special maximum test rating for condition F, when applicable (see 4.b).

k. Time temperature conditions for condition F, if other than as specified in 3.5.6.

* TABLE I. Steady-state time temperature regression. 1/ 2/ 3/ 4/

Minimum temperature T_A (°C)	Minimum time (hours)			Test condition (see 3.5)
	Class level S	Class level B	Class level S hybrids (Class K)	
100		7500	7500	Hybrid only
105		4500	4500	"
110		3000	3000	"
115		2000	2000	"
120		1500	1500	"
125	1000	1000	1000	A -E
130	900	704	---	"
135	800	496	---	"
140	700	352	---	"
145	600	256	---	"
150	500	184	---	"
175		40	---	F
180		32	---	"
185		31	---	"
190		30	---	"

1/ Test condition F shall be authorized prior to use and consists of temperatures 175°C and higher.
2/ For condition F the maximum junction temperature is unlimited and care shall be taken to ensure the device(s) does not go into thermal runaway.
3/ The only allowed conditions are as stated above.
4/ Test temperatures below 125°C may be used for hybrid circuits only.

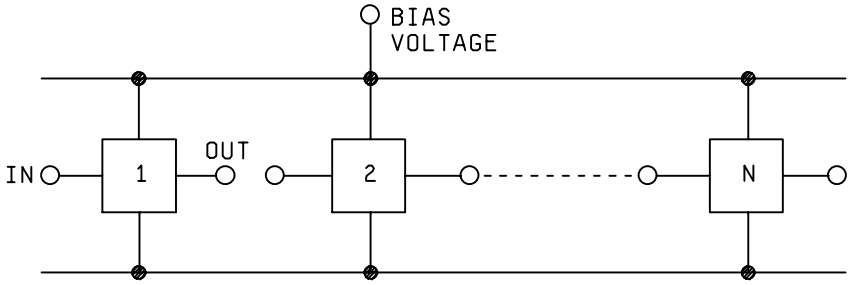


FIGURE 1005-1. Steady-state.

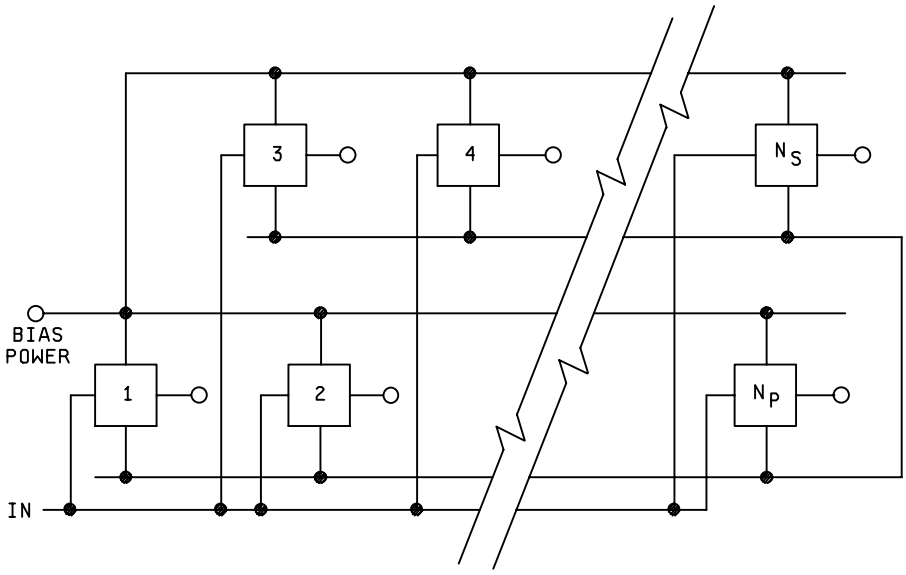
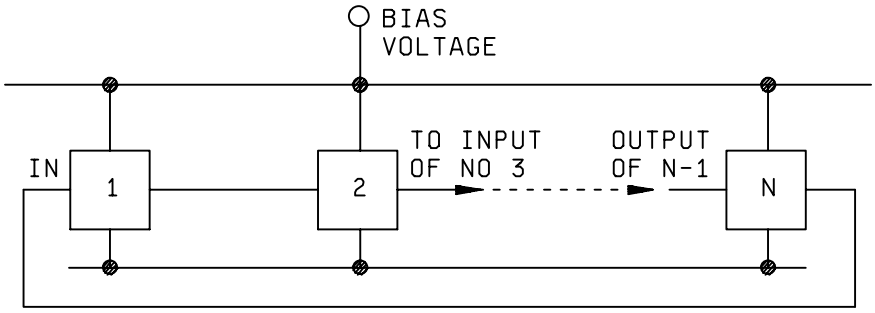
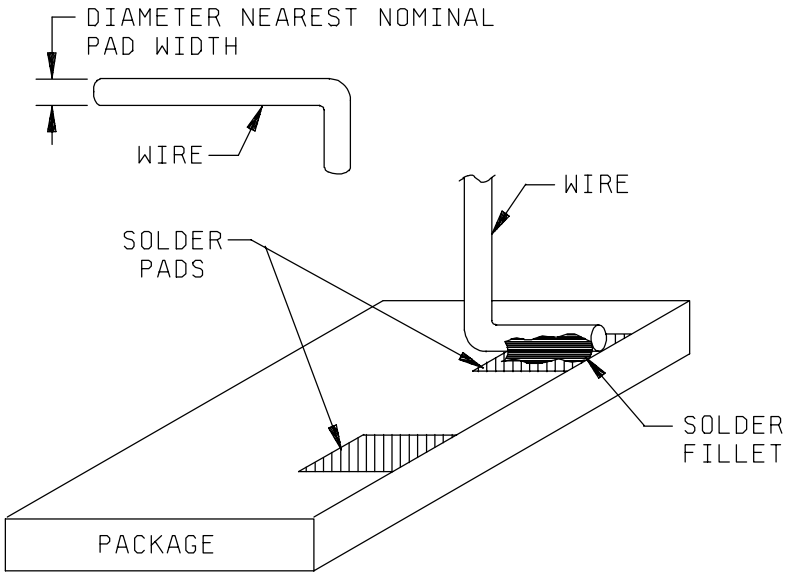


FIGURE 1005-2. Typical parallel, series excitation.



NOTE: For free running counter, N is an odd number and the output of N is connect to the input of 1.

FIGURE 1005-3. Ring oscillator.



MATERIALS

Flux: Flux type symbol “A” or “B” (flux type “L0” or “L1”) in accordance with ANSI/J-STD-004 (previously designated as Type R or RMA only, in accordance with MIL-F-14256).

Solder: Sn60A or Pb40A or Sn63A or Pb37A in accordance with ANSI/J-STD-006 (previously designated as Sn 60 or Sn 63 in accordance with QQ-S-571).

Wire: Soft annealed solid copper.

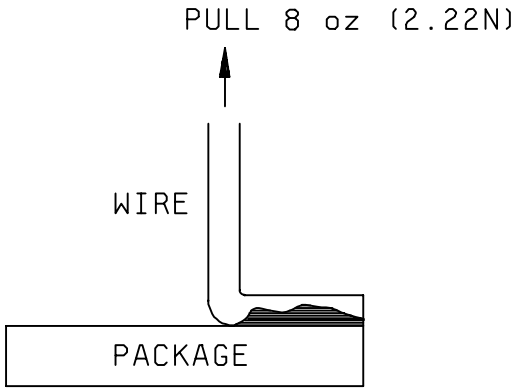


FIGURE 2004-2 Solder pad adhesion.

METHOD 1006

INTERMITTENT LIFE

1. PURPOSE. The intermittent life test is performed for the purpose of determining a representative failure rate for microelectronic devices or demonstrating quality or reliability of devices subjected to the specified conditions. It is intended for applications where the devices are exposed to cyclic variations in electrical stresses between the "on" and "off" condition and resultant cyclic variations in device and case temperatures.

2. APPARATUS. See method 1005 of this standard.

3. PROCEDURE. The device shall be tested in accordance with all the requirements of method 1005 except that all electrical stresses shall be alternately applied and removed. The "on" and "off" periods shall be initiated by sudden, not gradual, application or removal of the specified electrical inputs (including signal and bias).

4. SUMMARY. In addition to the requirements of method 1005 of this standard, the following detail shall be specified in the applicable acquisition document:

Frequency and duration of "on" and "off" cycles.