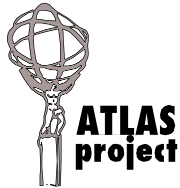

Design changes in the Cu/Polyimide barrel hybrid version 5

ATLAS Project Document No.	*Institute Document No.*	*Created:* **04/06/01**	*Page:* **1 of 8**
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Project breakdown name

Design changes in the Cu/Polyimide barrel hybrid version 5

abstract

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Distribution List

SCT

History of Changes

Rev. No.	Date	Pages	Description of changes
A	04/06/01	All	First version

1 Introduction

The Cu/Polyimide barrel hybrid has been developed for the readout of ASICs, ABCD, in the ATLAS SCT barrel modules. Because of distinct difference of geometrical configuration of the barrel and forward modules, the barrel hybrid was designed specifically for the barrel modules. After the barrel hybrid design review at CERN on 22nd June, 2000, the version 4 (k4) hybrid was introduced whose changes from the previous version were described in the document, “Design changes in the Cu/Polyimide barrel hybrid version 4” [1]. Number of barrel modules have been built for the final design review (FDR) of the barrel modules using the k4 hybrids and have been operated successfully in the laboratories, in the irradiated modules, in the beamtests, and in the system test at CERN.

The barrel module FDR was held on 24-25th June, 2001, at CERN. The barrel module was approved and recommended to proceed for mass production and the barrel hybrid, as a component of the barrel module, was also recommended to proceed for mass production, with a condition to document the necessary changes from the k4 to the mass production version.

There was no recommendation for a change in the hybrid design in the module FDR. However, in the k4 hybrid, there kept were a few options for connections which connections were made with wire-bondings for possible alternatives. In proceeding for mass production, these options are to be eliminated in order to save the work load and possible mistakes. This document describes the changes, together with two other changes, from the k4 hybrid to the mass production version, k5.

2 Design changes

2.1 Wire-bondings between AGND and DGND near ASICs

The connection of the analog ground (AGND) and the digital ground (DGND) and also the strength have been the issue. The wire-bonding pads between the two grounds were kept near the ASICs, 14 locations in total in a module. The default was to make connection with 5 wire-bonds.

These wire-bondings are to be made with a Cu trace between the two pads on the surface layer, Layer 1 whose thickness is about 25 μm, of a width of 0.1 mm wide.

2.2 Wire-bonding between the tempret line and DGND

The option was kept in order to minimize the extra noise if the noise is introduced through the temperature lines by disconnecting the temperature lines from DGND. Since the tempret line worked as the “DGNDsense” line, the default was to make the connection so that the “DGNDsense” line sensed the DGND potential near the middle of the 12 chips hybrid.

This connection is to be made with a Cu trace of a width of 0.1 mm wide.

2.3 Connecting ID4 to SELECT or VDD

Inside the ABCD chip, ID4 has a pull-down resistor and the chip is served by primary fibre, the LED output. In case the module is required to be served by an adjacent fibre, LEDX, the ID4 is set by SELECT-high. The option was to set ID4 high by connecting ID4 to the digital power supply potential, VDD, instead of the SELECT-high connection.

The default connection, ID4 to SELECT made with wire-bondings, is to be made with a Cu trace on a width of 0.1 mm wide.

2.4 Short circuiting SMD, R36

In the bias filtering circuitry, the surface mount device (SMD), R36, was laid out in order to optimize the resistance value in the filtering circuitry. The default was short-circuiting and a zero ohm resistor was soldered.

This short-circuiting is to be made with a Cu trace of a width of 0.5 mm wide.

2.5 Gap between decoupling capacitors and ground pattern

On the surface layer, four decoupling capacitors, C72 to C75, are laid in order to connect the backplane of the silicon microstrip sensors to the analog ground. The bonding pads where the wire-bondings between the sensor backplane and the capacitors are made are adjacent to the analog ground on the hybrid. The gap between the bonding pads and the ground pattern is to be enlarged from 0.85 mm to 1.0 mm in order to give an extra safety factor for high voltage breakdown.

2.6 ASIC die size

The latest information of the ABCD3T die size is 6.610 mm x 8.450 mm, from the calculation of the dicing step size of 6.640 mm x 8.480 mm and a saw blade thickness of 30 microns. The ASIC chip pad is 6.550 mm x 8.400 mm in the k4 version. The chip pad is only narrower by 60 microns. The nearest bonding pads are 0.8 mm away from the chip pad and the shrinkage of the gap by 30 microns, per side, is tolerable.

There will be no change to the size of the chip pads nor the nearest bonding pads.

3 Electrical drawings

The updated circuit diagrams are shown in Figure 1 and Figure 2 (2 pages), “Circuit Diagram of Barrel Cu/Polyimide Hybrid for ABCD3T chips (ATLAS/k5ABCD3/200105)”. The changes implemented are drawn in red.

The physical changes in the layout are shown in Figure 3 and Figure 4 (2 pages), “Changes from k4 to k5 barrel hybrid”. The changes are limited only in the surface layer, Layer 1, and narrow traces between the bonding pads. In case of emergency, a surgery is possible to remove the trace for disconnecting or to add wire-bondings or soldering for reinforcing the connection.

References

[1] Y. Unno, T. Kohriki, T. Kondo, et al., “Design changes in the Cu/Polyimide barrel hybrid version 4”, http://atlas.kek.jp/~unno/si_hybrid/k4/k4change000717.pdf

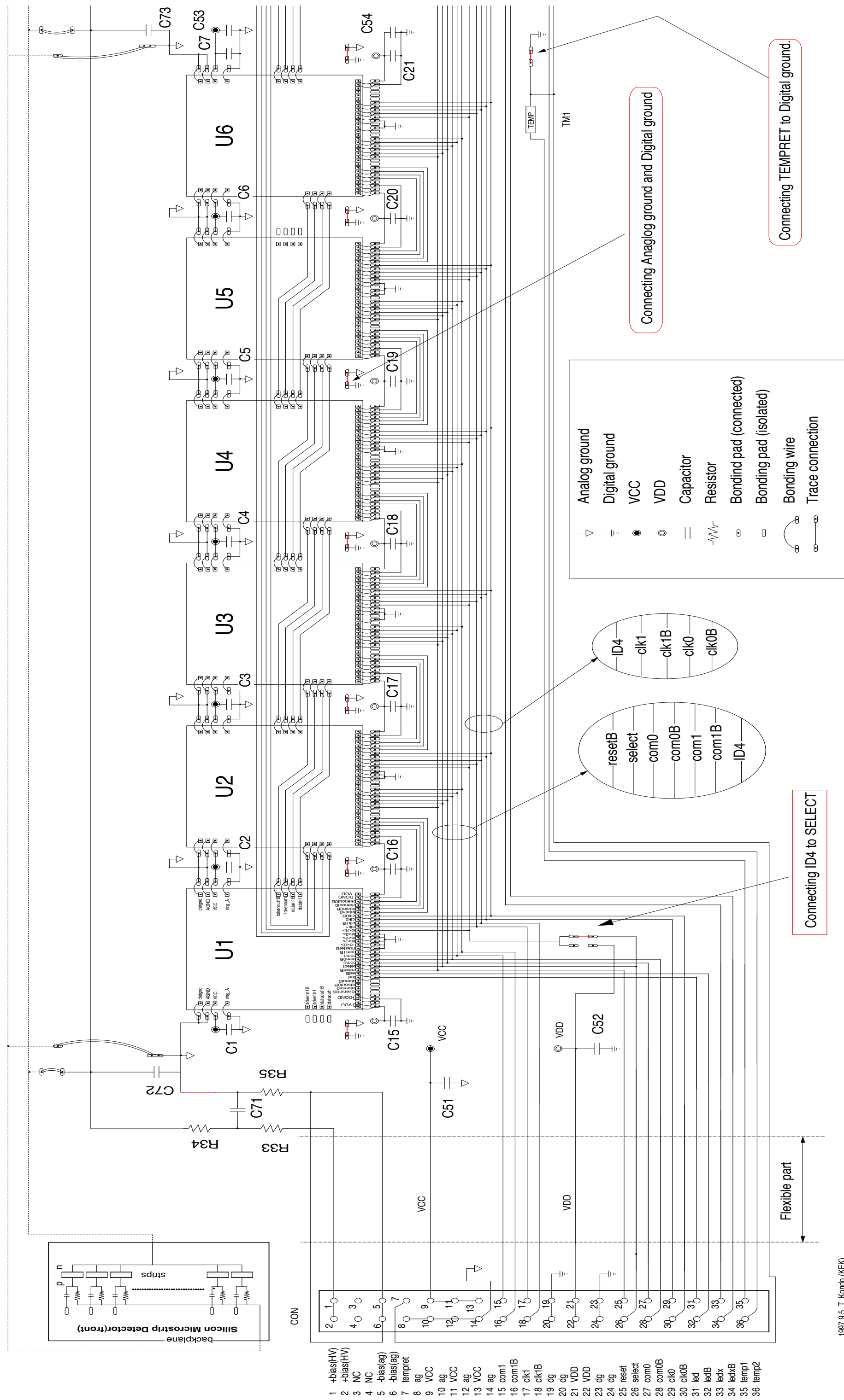

Figure 1 Circuit diagram of the barrel Cu/Polyimide hybrid version 5, connector side. The changes from k4 are shown in red

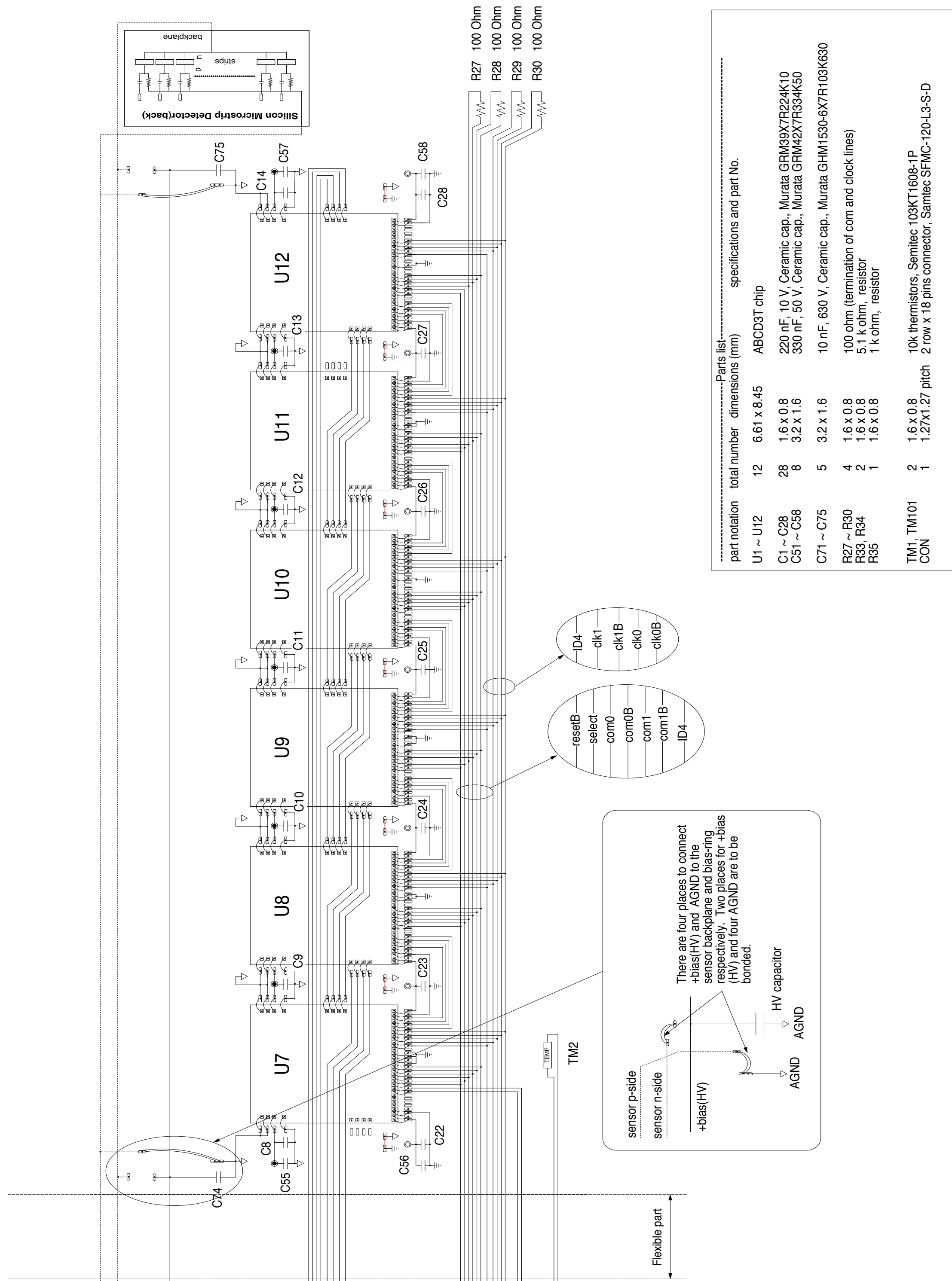

Figure 2 Circuit diagram of the barrel Cu/Polyimide hybrid version 5, far-end side. The changes from k4 are shown in red

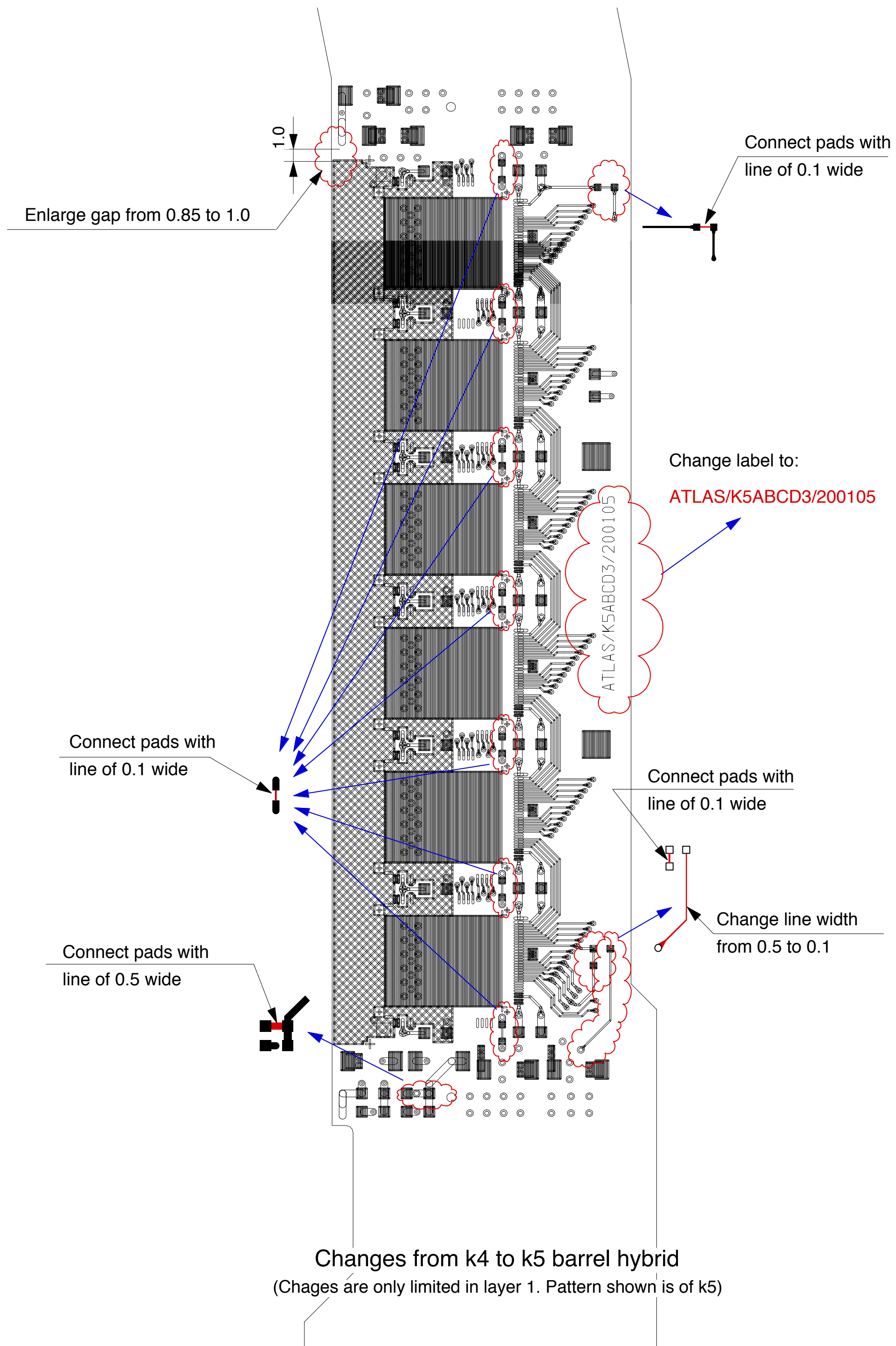

Figure 3 Layer 1 layout of the barrel Cu/Polyimide hybrid version 5, connector side. The changes from k4 are shown in red

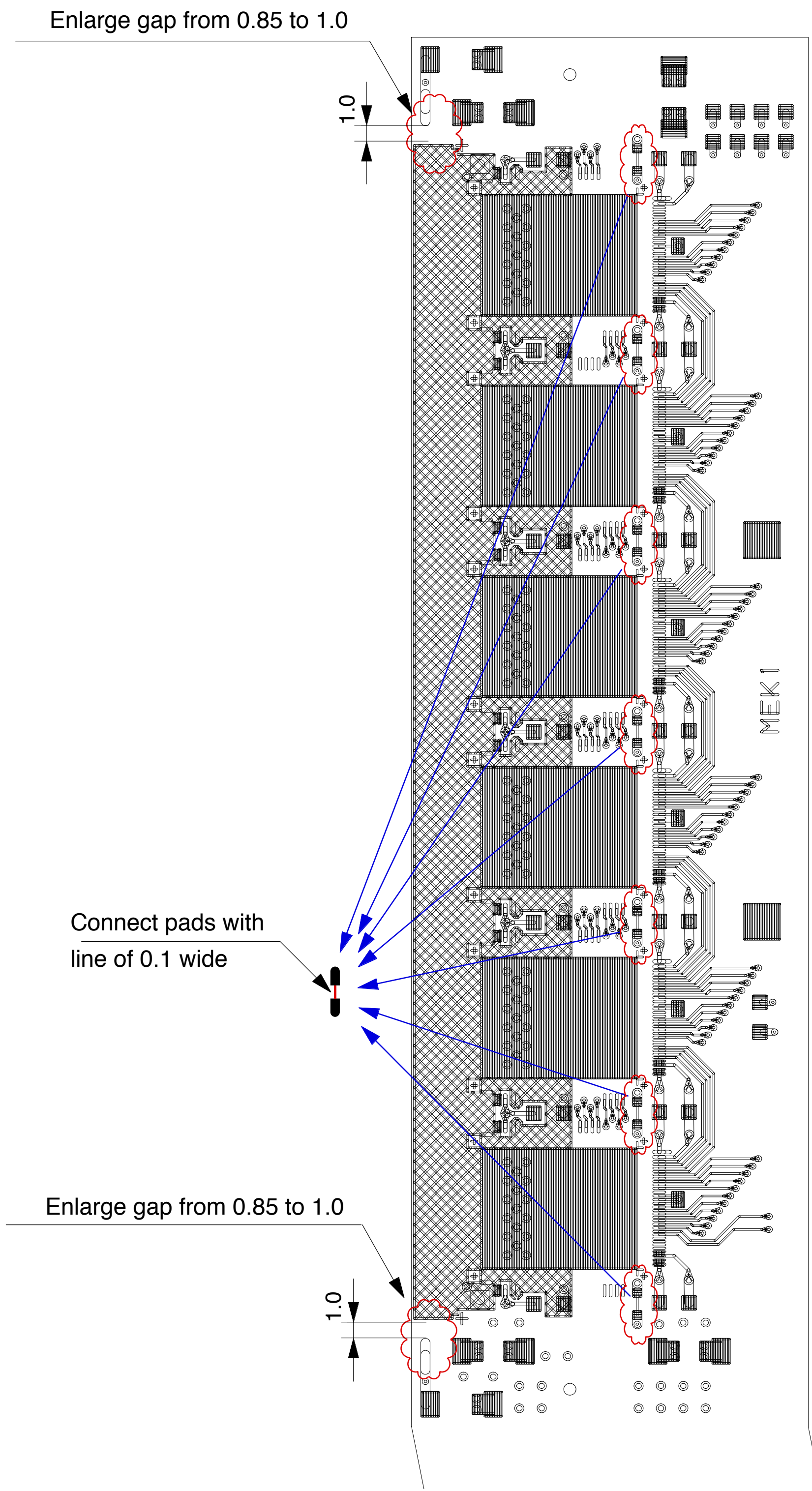

Figure 4 Layer 1 layout of the barrel Cu/Polyimide hybrid version 5, far-end side. The changes from k4 are shown in red