# Module Specification

(Updated: 1995/9/21)

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|---|---|
| Module overlap (active area?): | 3mm in z, 8 strips in $\phi$ |
| (look at the placement tolerance...then, | ->500μm(z), 2 strips($\phi$)/per side? |
| Module tilt angle: | 6~7° (TBD) |
| Mechanical tolerance: | |
| Placement of wafers within a module: | r/$\phi$=±5μm, z=±25μm |
| Placement of modules on support structure: | r=±250μm, $\phi$=±50μm, z=±100μm |
| Survey of modules on the support structure: (Warm/Cold?) | r=±50μm, $\phi$=±25μm, z=±50μm |
| Module and support structure stability: | r/$\phi$=±10μm, z=±100μm (chip power change by 20%?) |
| Thermal cycles (10[1] cycles in -20~70[2] °C): (50 cycles for sampling; 5 cycles every?) | <±5μm deformation<br>no electrical change |
| Electrical connectors: (100 cycles for sampling; ? cycles for every?) | survive 100 cycles |
| Wirebonds: | breakability of individual bond |
| Operating temperature: | |
| <Silicon>[3] operating temperature: | -10 °C (at coldest?) |
| <Silicon> temperature uniformity: | <5 °C |
| Design Constraints: | |
| Radiation level (TP p179, 3yrs $10^{33}$+7yrs $10^{34}$) | ?? $2\times10^{14}$ 1MeV-n/cm$^2$ ??<br>110 kGy |
| Power disipation: | |
| Detector (at 30cm) : | 300μm×6cm×6cm |
| Max leakage current of a wafer; | 0.66mA@0°C |
| Max operating voltage: | 300V(?) |
| Electronics (double-sides): | |
| Analog readout | 1024ch×3mW/ch=3.07W |
| Binary readout | 1536ch×2mW/ch=3.07W |

[1] 50 → 10 cycles (1995/9/21)
[2] -10~40°C → -20~70°C (1995/9/21)
[3] <Silicon>: Averaged over silicon detector