0.1 Silicon Microstrip Detector

0.0.1 System description

The SCT silicon microstrip detector system is providing capability of pattern recognition, momentum, and vertex resolution, working together with other parts of the inner detector system. In the barrel region, the high-precision detector layers (silicon pixel and silicon microstrip detectors) are arranged on concentric cylinders around the beam axis in the region with $|\eta| < 1$, while the end-cap detectors are mounted on disks perpendicular to the beam axis. The silicon microstrip detector part is made of four concentric cylinders in the barrel and nine disks per side in the forward region. The total number of precision layers is limited because of the material they introduce and their high cost

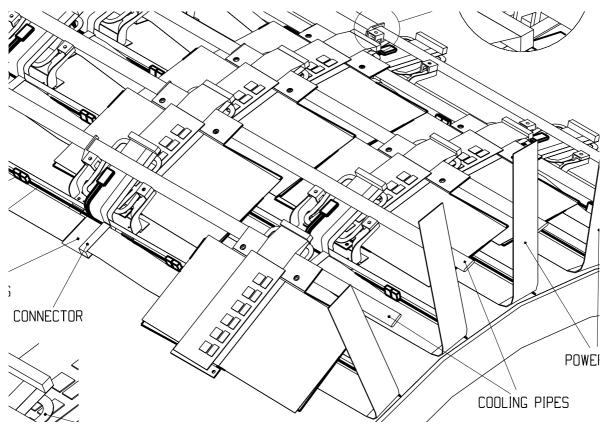


Figure 0.1 A view of the silicon microstrip modules, cooling, electrical and optical service arrangement in the barrel cylinder.

The microstrip detector system is made of microstrip detectors, each of $6.36 \times 6.40 \text{ cm}^2$ in area with 768 readout strips with 80 µm pitch, covering 61 m² area of silicon in total. One module is made of four such detectors which provides precision measurement of points in the R ϕ and z coordinates using small angle stereo arrangement. On each side of the module, two detectors are wire-bonded to form 12.8 cm long strips. Two such pairs are then glued together back-to-back at a 40 mrad angle, separated by a heat transport plate. With on-off readout of the strips, the spatial resolution is 16 µm in R ϕ and 580 µm in z. Tracks can be distinguished if separated by more than ~ 200 µm. The forward modules are very similar in construction but use ta-

pered detectors, with one set of strips aligned radially. The number of readout channels is 6.2 million, in total, in the barrel and forward regions.

The barrel modules are mounted individually on carbon-fibre cylinders which carry the cooling and electrical service systems; the four complete barrels at radii of 300, 373, 447 and 520 mm are then linked together. Figure 0.1 shows the design of a barrel cylinder with modules, cooling pipes, and electrical services. The system requires cold operation of the detectors, evacuation of the heat generated by the electronics and the detector leakage current effectively, and a very high dimensional stability. The structure is designed with materials with as low a radiation length and a coefficient of thermal expansion as possible.

The silicon microstrip detector system will experience a severe radiation level of 2 x 10^{14} particles/cm² accumulated in 10 years of operation in the inner-most barrel region. This radiation level alters the character of the detectors: increasing the leakage current more than 3 orders of magnitude than the initial current, mutating the bulk type from the initial n-type to the p-type, and decreasing the bulk resistivity which in turn increasing the depletion voltage. The microstrip detector system is designed to be operated at a temperature around -7 °C in order to reduce the leakage current to suppress the heat generation and to suppress the activation of pseudo-acceptor states generated by the radiation damage.

Prototype microstrip detectors have been built, irradiated, and tested to conform the performance after the radiation damage. Prototype modules have been designed and tested for the thermal stability against the thermal runaway. Electrical modules have been built and tested in labs and in beams to confirm the required performance in resolution, signal-to-noise and speed.

0.0.1 R&D and design where the Japanese group is being involved

0.0.1.1 Silicon microstrip detector development

The radiation level in the inner detector is very high (See Appendix H.4). The primary source of the radiation is the particles originating from the primary vertices. In the outer region of the silicon system, the neutrons coming from the calorimeter has influence over the particles from the primary vertices.

The effect of radiation damage to the silicon strip detectors is three folds: increase of the leakage current, increase of depletion voltage, and decrease of charge collection. The former two effects are strongly temperature dependent, with both "beneficial annealing" effects in the depletion voltage and the leakage current, in which the damage is recovered with time, and also "reverse annealing" which leads to an increase in the depletion voltage with time. An operation temperature of -7 °C of the detector is planned to suppress the leakage current and the reverse annealing.

Assuming conservatively that the detector is removed each year for maintenance, a 'standard access procedure' (SAP), a warm-up time of 2 days at 20 $^{\circ}$ C, and a 14 day maintenance period at 17 $^{\circ}$ C, the depletion voltage of the detector will increase and, in the inner-most barrel region, reach near 400 V after 10 years of operation.

The detector technologies against this high radiation level has been investigated, including both the double-sided and single-sided readout technologies. Although the double-sided readout technology has attractiveness in reducing the material, the high depletion voltage requires ei-

ther very robust AC coupling capacitors in the detector, which is difficult for more than 100 V, or to float at least one side of readout electronics, which offsets the attractiveness of less material. The candidates are, then, the single-sided readout technology where the voltage of the readout side is to be grounded. The technology with the n-strip readout (n-in-n) or the p-strip readout (p-in-n) on the n-bulk silicon have been put for full comparison. The advantages and the disadvantages of the technologies are,

a) n-in-n

Advantages: After the type inversion of the silicon bulk, n-readout strips become the p-n junction. This allows the detector to be operated partially depleted while maintaining high detection efficiency. Thus, the detector can cope with the increase of depletion voltage and tolerate unexpected increase of depletion voltage, e.g., unexpected warm-up, higher luminosity, etc., softly.

Disadvantages: Before the type-inversion, the p-n junction is in the backside. The backside lithograph-process is required for the p-n junction to be kept inside the geometrical dimension. This backside process adds an extra cost.

Technical issue: The n-strip readout in the n-side of the n-type silicon detectors requires a so-called p-stop structure between the n-strips. The design of the p-stop structure is critical to minimize the inter-strip capacitance and reduce the noise generated in the edge of the structure. This is because there are trapped positive charges in the silicon and oxide interface which causes the surface of the bulk to be conductive n-type which is difficult to deplete even with high bias voltage. The p-stop structure is a p-implantation and cuts the conductive surface. Along the accumulation of radiation damage, the positive charges trapped in the interface will increase (and eventually saturated). Although the bulk will be mutated to p-type after heavy radiation damage, the surface is still remaining to be n-type. Thus, the p-n junction after the radiation damage is at the edge of the p-stop structure rather than at the n-strips. Although the p-n junction in the readout side allows the lower operation voltage, if the electric field strength enhanced by the positive trapped charge is high enough, specially at defects in the edge of the p-stop structure, there would be development of tiny avalanche breakdown named "micro-discharge" occasionally [0-1]. This has been shown in the study of the "micro-discharge" in the silicon strip structure with a super-sensitive infra-red camera as shown in Figure 0.2. The design of the p-stop structure was the major issue in the design of the n-in-n detector.

b) p-in-n

Advantages: The p-in-n detector requires the lithograph-process only in one side. Thus it has implication of lower production cost.

Disadvantages: The p-n junction moves from the initial p-strips to the backside n-contact after heavy radiation damage because of the mutation of the bulk. In the partially depleted operation the collected charges to the p-strips would be less because of undepleted region near the readout side. Thus, the p-in-n detector requires high voltage to be efficient, as high as the full depletion voltage or more.

Technical issue: The p-n junction after heavy radiation damage is in the backside n-contact. Since the backside is not lithographically processed, the p-n junction will extend to the physical cutting edges. If the p-n junction is exposed in the initial phase, it is known to break in very low bias voltage. However, recently, there has been accumulation of knowledge that the p-in-n detectors do not break down in low bias voltages when they are radiation damaged. The major

technical issues were then the confirmation of no-breakdown as high as 400 volts and high efficiency near or below the depletion voltage afer heavy radiation damage.

After long collaborative work in the SCT community in the comparison of two technologies, the following results were established:

1) The p-in-n detectors post-irradiation have been shown to be operated up to 500 volts with the leakage current similar to the n-in-n detectors [Figure 0.3].

2) The p-in-n detectors have to be run close to the full depletion voltage for full efficiency.

3) The depletion voltage is not a well controlled parameter. However, the measurements indicate operation voltages, at the end of ATLAS, with 300 μ m thick detectors of ~250 volts for n-in-n and ~450 volts for p-in-n to have high efficiency at low radii.

3) The Hamamatsu n-in-n detector with polysilicon field plates above the p-stops has reached the stage of development that it could be ordered now with full confidence that it would perform well throughout the life of ATLAS at all SCT radii.

Considering the resource available and the cost of detectors, the SCT community has chosen the p-in-n technology for the whole SCT with the design: (i) The voltage limited to < 350volts (ii)The innermost barrel and inner rings of detectors to be thinned to ~ 270 microns if necessary to achieve full depletion.

Projections for the SCT after 10 years of operation indicate, in the most pessimistic case, the depletion voltage, V_D , does not exceed 450V for 300 µm thick silicon; this means that even in the SAP scenario the operation at 350 V of *p*-in-*n* detector designs with the thickness of 270 µm will meet the LHC requirements.

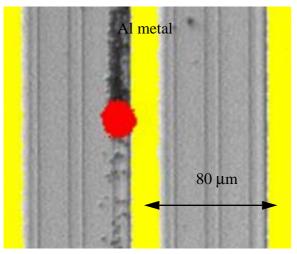


Figure 0.2 Hot spot in the edge of p-stop structure in the n-side of a n-in-n detector, identified with the IR camera.

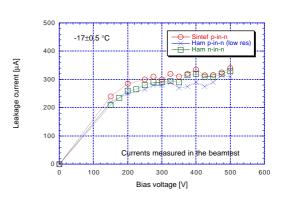


Figure 0.3 Leakage currents measured in a beamtests of the Hamamatsu n-in-n and p-in-n detectors after 3 x 10^{14} protons/cm² irradiation, together with a SINTEF p-in-n detector.

0.0.0.1 Silicon microstrip module development

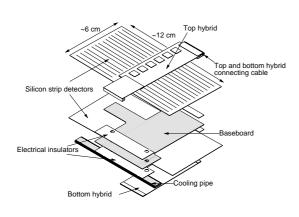
Topology of the module

Two types of module topology were investigated: one is with hybrids mounted on the middle of module ("centre-tap design"), the other with hybrids attached in the end of the module ("end-tap design").

Two types of thermo-mechanical modules were built at KEK and separately at RAL and compared the thermal performance. The modules were placed inside an environmental chamber. Both the ambient temperature and the pressure inside the chamber were controlled in these measurements. The ambient temperatures was set to 0°C. The heaters were powered with 1 W for the silicon detectors and 3 W for the hybrid pair. The data taken in vacuum were particularly useful in separating out the contribution of air convection cooling and to find parameters for use in finite element analyses. The centre-tap design showed temperature gradients across the module which are acceptable for use in the ATLAS SCT (See Appendix H.6).

Effective overlap along z and a minimization of dead regions preferred to a barrel module configuration with the hybrid electronics package mounted over the active region of the silicon, rather than off the end as was common in small vertex detectors. Electronic noise analyses for the shaping times used in SCT show that a centre tapped configuration will have the minimum noise contribution from the series resistance of the readout strip. The improvement over an end tapped configuration is about 150 electrons. Experience on constructing the two types of modules in the community showed that the centre-tap design is more robust than the end-tap design in the construction.

In balance, the centre-tap design was adopted as the module topology in the barrel region. An expanded view of the module is shown in Figure 0.4.



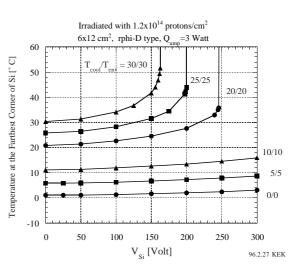


Figure 0.4 Expanded view of the barrel silicon trip module. The baseboard is the heat spreader with the PG1700.

Figure 0.5 Thermal runaway measurement in the module with irradiated detectors.

Thermal stability against thermal runaway

The critical issue in the design of the module is the thermal stability against the thermal runaway of the silicon strip detectors after heavy radiation damage. This is a new feature in the design of the silicon strip modules different from the previous detectors. The leakage current of the damaged detectors is so high that it heats up the silicon detectors themselves. The leakage current is an exponential function of the temperature, and feedback of self-heating leads to a higher temperature and to the thermal runaway unless the heat is extracted effectively from the module to the cooling element. The initial heat flux normalized at 0 °C after 10 years of operation is 100 μ W/mm². The design requirement against the thermal runaway was that the runway should not occur less than twice the initial heat flux, i.e., 200 μ W/mm².

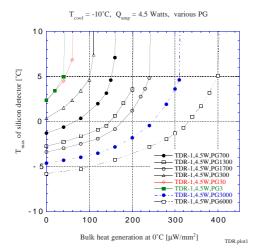
The thermal runaway has been demonstrated to take place in radiation damaged silicon detectors [0-2]. A realistic ATLAS silicon strip module was fabricated using two irradiated detectors. A mock-up hybrid, instrumented with a 3 W heater was placed near the middle of the module. A cooling pipe ran over the edge of the hybrid and the temperature of the furthest corner of the silicon was measured as a function of the bias voltage applied to the irradiated detectors. Heat was therefore generated in both the silicon and the hybrid. In this particular study stable thermal containment was obtained for all relevant bias voltages for cooling/air temperatures below 10° C, and runaway actually occurred at 250 V bias when they were increased to 20° C [Figure 0.5].

The thermal runaway was extensively studied using a finite element analysis program . In the analysis, the heat spreader sandwiched in the middle of the module was realized to play a critical role in the prevention of the thermal runaway. Figure 0.6 shows the character of the thermal runaway, the highest temperature of the silicon detector, as a function of initial heat flux. The material called "Pyrolytic graphite (PG)" is available in the market and the one with the thermal conductivity of 1700 W/m/K has been taken as the primary candidate of the heat spreader. The optimization of the shape of the heat spreader is done with the finite element analysis in order to minimize the material. The thermal profile in the module has been simulated as shown in Figure 0.6, where the thermal runaway is about to occur.

Another expression of the thermal runaway is made as a function of time, which visualizes the lifetime of the damaged detector. The runaway occurs much faster than as expressed with the function of heat flux. This is because the heat flux is a multiplication of voltage and the leakage current, where both the voltage and the leakage current increase as time. Thus, the heat flux is at least the quadratic of the time. As the heat flux becomes near the runaway point, the temperature rises quadratically. Thus, the total effect of the runaway as a function of time is more than 4th power of the time. One consequence of the study is that to be away from the runaway is to limit the operation voltage. The life of the detector is then determined by the loss of efficiency (Appendix H.6).

Thermo-distortion measurement

Another important thermo-mechanical issue concerns distortions between the construction temperature of ~25°C and the operating temperature of ~ -10°C. The thermal test barrel module was measured using an ESPI system developed at Oxford Univ., UK, which is sensitive to distortions of 250 nm or larger. The measured distortion of the module was 9 μ m when cooled from 24°C to 0°C without turning on the heaters. When heaters were turned on with 1 W for the silicon and 3 W for the chips the incremental distortion was 4.8 μ m at 0°C and 1 μ m at room temperature (Appendix H.6).



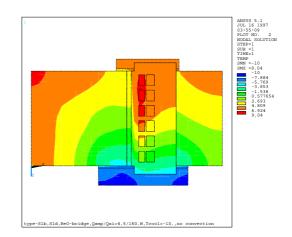


Figure 0.6 Thermal runaway analysis as a function of heat flux in the silicon bulk for three thermal conductivities of PG. 100 μ W/mm² is the heat flux at 300 V after 2 x 10¹⁴ pions/cm² fluence

Figure 0.7 Thermal profile finite element analysis with the input heat flux of 160 $\mu W/mm^2$ in the silicon and 4.5 W in FEE with the cooling contact at -10 °C

Beam tests

Number of beamtests have been executed at KEK using the testbeam line in the 12 GeV proton synchrotron in order to evaluate the performance of the detector with the clearly defined particles.

One of the results is the measurement of the efficiency as a function of bias voltage of the irradiated double-sided detector. The damage level was $1 \times 10^{14} \text{ proton/cm}^2$. This measurement enabled us to quantify the efficiency of the n-side readout and the p-side readout simultaneously The result was a precursor of the result presented in the detector development, that the n-side was efficient with the bias voltage as low as half the bias voltage required to for the p-side. [0-4]

Another beamtest was the evaluation of the various p-stop structures in the n-side of the n-in-n detector. The structures implemented were the ordinary common (full-common), the common but has openings in the p-stops (slit-common) for comparison, the individual common only surrounding the n-strips (individual), and the combined structure where the n-strip and the individual p-stop were bayed in the trace of common frame (combined). The point of the measurement is to quantify the effect of un-touched area which is a conductive n-type surface. The charge collection loss was measured between the n-strips. The charge collection was nearly equal in the full-common and the combined region, while the individual structure showed the least collection among the structures [0-5].

0.0.0.1 Barrel structure development

In the barrel the modules are mounted on the cylinder. One row of the module is made of 12 units. Two concepts were developed for the mounting: one is to mount the 12 module onto an interim unit (called stave) to make a super-unit, and the other is to mount the modules individually and directly on to the cylinder. After the evaluation of assembly steps, testing steps, mate-

rials involved, arrangement of cooling connections, etc., the latter concept of mounting the modules directly on to the cylinder was adopted for the barrel structure.

0.0.1 Construction plan of the Japanese group

The proposed responsibility

The proposed responsibility of the Japanese group is

1) Production of 57% of the barrel silicon strip detectors (about 5,800 detectors),

2) Production of 27% of the barrel silicon strip modules for the 3rd barrel cylinder, including the assembly of hybrids to be used in the module production (about 700 modules),

3) Production of 18% of all optical links which is mainly the production of flex part of the links for the barrel section,

4) Assembly of 3rd barrel cylinder.

The concept of the proposed responsibility is to deliver the completed 3rd barrel cylinder to CERN. The clusters involved in the barrel module assembly in the SCT community is four: Japan, Scandinavia, UK and US. With these involvement, 25% of module production is the nominal number and considering the resource of the clusters, the fabrication of four cylinders are split into the clusters.

In order to construct the barrel silicon detector system, not only the modules but also other components, such as front-end electronics, power supplies, off-detector electronics, are required. Since Japan will not produce components other than listed above, the resource responsible for completing the 3rd barrel in the detector system is provided by producing the detectors compensating the required resource. Japan has been playing an important role of developing the silicon strip detectors, together with the high quality of semiconductor industry, especially the good collaboration with Hamamatsu photonics Co. Ltd., it is natural to concentrate the Japanese resource to the production of silicon strip detectors.

Silicon strip module is an mechanical and electrical object. It is critical to understand the electrical properties of the modules to complete the full cylinder assembly and delivery. The fabrication of the hybrid and testing is the basic building block to complete the job.

Japan is also in good position having a Kapton flex circuit production capability in industry. The discussion leads to production of the flex part of the opt-link units which will be attached to the cylinder between the modules and the low-mass tapes and the opt-fibres. This is the production of component. The fabrication into the opt-flex unit is still under discussion.

Construction plan:

Once the Prototying has finished, the production of the detectors is the responsibility of the vendor, including the basic testing such as the leakage current, C-V measurement, strip open/short, AC capacitor open/short. The testing of the process against the radiation damage will be sampled with "baby" detectors (1 cm x 1 cm) and other test structures implemented in the same wafer, which are to be irradiated to the full fluence along the production of detectors. The irradiation is the coordinated task of the SCT community and the testing will be the task of module construction clusters, i.e., KEK and universities (defined as the Japanese group) for the Japanese share of the modules.

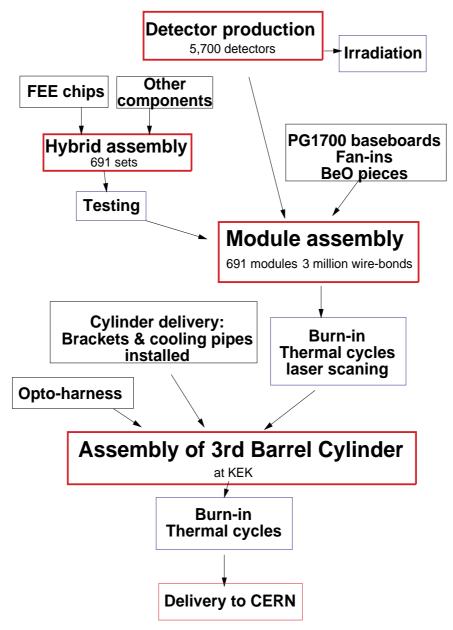


Figure 0.8 Construction flow of the 3rd barrel cylinder.

The components of the hybrids will be provided as a kit including the tested "good die" front-end LSI's. The hybrid assembly, basic testing of functionality, and burn-in will be done in industry with the supervision of the Japanese group.

Mechanical assembly of the modules will be done in the industry where an automatic wire-bonder is available. The automatic bonder is essential considering the large number of modules of 700, where 2.2 million wire-bonding is involved. Prototyping and establishing the assembly process, including the testing and quality control, will be the part of Japanese group responsibility. Supervision of the fabrication will be continued by the group once the module

production is started in industry. The burn-in of the modules, thermal cyclings, and the scanning of the strip-channel quality with a laser scan equipment will be done by the Japanese group.

Assembly of the 3rd barrel cylinder is to take place at KEK. Burn-in and thermal cycling will be performed along the mounting of the modules on to the cylinder.

Time scale:

Detector production: Starting in the Japanese fiscal year (JFY) of 1999, continuing for 3 years

Hybrid production: Starting in the JFY 1999, continuing for 2 years

Module fabrication: Starting in the middle of JFY 1999, continuing 3 years

3rd barrel assembly: Staring in the end of JFY 2000, continuing 2 years

All the domestic work will be done by the middle of 2002. The completed 3rd barrel cylinder will be shipped to CERN in the summer of 2002 and its installation into the inner detector will take place at CERN subsequently.

0.2 References

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