# Beam Test of a Large Area n-on-n Silicon Strip Detector with Fast Binary Readout Electronics

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*Abstract*

A large area (60 mm × 60 mm) n-bulk and n-strip readout silicon strip detector was prototyped for the ATLAS SCT detector. Detector modules of 12 cm strip length were made by butting two detectors. One of the 12 cm modules was irradiated with protons to a fluence of $1.2 \times 10^{14}$ p/cm$^2$. A beam test was carried out for the non-irradiated and the irradiated detector modules. Efficiency, noise occupancy and performance in the edge regions were analyzed using the beam test data. High efficiency was obtained for the non-irradiated detector and for the irradiated detector for bias voltages down to about half the full depletion voltage. The noise occupancy was $<2 \times 10^{-4}$ for the 12 cm strips. The measurement of the edge region exhibited a difference in the sensitivity under the bias resistance where no extension of the n$^+$-implant was fabricated.

## I. INTRODUCTION

A large area silicon strip detector (60 mm × 60 mm) with n-strip readout electrodes on an n-bulk substrate was fabricated to prototype a detector for the ATLAS Semiconductor Tracker (SCT) [1]. Typical silicon strip detectors are read out with p-strips on n-bulk silicon. After a fluence of several times $10^{13}$ particles/cm$^2$, the bulk becomes p-like and the p-strips now form an ohmic contact, which requires the detector be fully depleted to maintain electrical isolation between strips. SCT silicon strip detectors are expected to accumulate more than $10^{14}$ p/cm$^2$ in 10 years of operation. This would result in a depletion voltage of about 300 V at a fluence of $2 \times 10^{14}$ p/cm$^2$ even in the best case where the detectors were cooled to around -10 °C throughout their lifetime to suppress the increase of acceptor-like states (anti-annealing).

The choice of n-strip readout on n-bulk material is based on the idea that the p-n junction will be at the n-side strips after type inversion, so that interstrip isolation is maintained even in partial depletion. This means that the detectors are still usable at fluences that exceed the limit determined by the maximum safe operating voltage and yields a gradual deterioration of detector performance where usability is ultimately limited by inadequate signal-to-noise ratio.

The purpose of this test was to compare the tracking performance of the n-on-n detector before and after type-inversion and in partial depletion. We also studied the effects at dead regions at the periphery of the detector, specifically at the ends of the strips and the biasing structures.

## II. N-STRIP ON N-BULK DETECTOR

One large area (60 mm × 60 mm), n-strip on n-bulk silicon strip detector was fabricated out of one 4-inch wafer[2]. The n-on-n detectors require semiconductor manufacturing processing not only on the n-side but also on the p-side to have an initial p-n junction, which by itself presents a challenge for the manufacturer to maintain a high fabrication yield. The specification of the detector, designated "nn75AC", is summarized in Table 1.

The large-area p-n junction on the backside was lithographed to have a bias-potential holding structure to the dicing edge and was covered by aluminum metal to make one large area DC-contact pad. The n$^+$-implant strips were laid out with a strip pitch of 75 µm. The strips were AC-coupled to the aluminum readout metal strips with a double-layer structure of silicon dioxide ($SiO_2$) and silicon nitride (SiN) to suppress eventual pin-holes in the insulator. The n$^+$-implant strips were separated by a continuous common p$^+$-stop implantation. The width of the n$^+$-implant strip of 16 µm was chosen to give a reasonably low inter-strip capacitance, which is the major contributor of the intrinsic noise of the electronics. The width of the p-stop was determined by leaving a space between the n-implant and the p-stop of 8 µm which allowed a mask alignment error of 1 µm while maintaining good separation between the n-implant and the p-implant.

The n-implant strips are biased through polysilicon resistors connected to a bias rail surrounding the n-strip area. A value of 1 MΩ was chosen to give an acceptable voltage drop for the leakage current at the operating temperature of -10 °C when heavily damaged, and yet limit their noise contribution to a few percent.

The readout implant strip (n$^+$) ends about 1 mm from the dicing edge of the detector. At the end with the bias resistor, the prototype detector used in this beam test had no implant extension under the polysilicon resistance so that the n$^+$-

Table 1
Specification of the n-on-n single-sided silicon strip detector (nn75AC)

| | |
|---|---|
| Detector type: | N-bulk, n-strip, AC-coupled, Single-sided |
| Bulk type: | N-bulk |
| Resistivity: | 4~8 kΩcm |
| Size (Outer): | 6 cm × 6cm |
| P-side structure: | DC-coupled pad<br>Junction breakdown ≥300V |
| N-side structure: | Active-to-edge insensitive area ≤ 1.0 mm<br>Polysilicon bias resistor: 1.0±0.2 MΩ<br>AC-coupling: $SiO_2$ 0.25µm+SiN 0.05µm<br>Interstrip capacitance ≤10 pF/6cm |
| Strip isolation: | Continuos floating p-stop |
| Strip parameters: | |
| Strip pitch: | 75 µm |
| Readout pitch: | 75 µm |
| Implant width: | 16 µm |
| Width of Al readout: | 16 µm |
| P-stop width: | 43 µm |
| Gap between implants: | 8 µm |
| Al thickness: | 1.5 µm |
| Resistance of Al readout: | ≤20 Ω/cm |
| Resistance of implant | ≤100kΩ/cm |
| DC-contact to implant | Contact hole/pad |
| Number of strips: | (128×6=768 readouts) + 6 dummies |
| Sensitive width: | 768×75µm = 57.6 µm |
| Leakage current: | Total including guard <25µA at 200V<br>Per strip <50nA at 200V |

implant strip ends near the connection of the polysilicon resistor to the implant strip.

## III. Modules

A single-sided detector module with a strip length of 12 cm was fabricated by butting and wire-bonding two nn75AC detectors together (Fig. 1). The readout electronics were mounted on a hybrid traversing the detector near the middle of the 12 cm detector unit and connected to the strips in the middle. This geometry minimizes the inter-strip coupling due to extra lines connecting the strips to the electronics and the noise contribution due to the strip resistance [3]. The module was mounted in a printed-circuit support card used for mechanical mounting and interfacing the 20 m long signal cables and power lines to the VME readout electronics sitting in the counting hut. Two modules were tested: one module with non-irradiated detectors, and the other with detectors irradiated with protons to a fluence of $1.2 \times 10^{14}$ p/cm$^2$. The readout hybrid was mounted on the detector after the irradiation of the detectors.

The fast binary readout front-end electronics consisted of pairs of chips: the first chip, implemented in bipolar transistor technology, comprised a fast amplifier, shaper, and discriminator to detect the presence of hits. The second chip, implemented in radiation-hard CMOS, was a clocked digital pipeline to accommodate the trigger latency time. Two types of bipolar chip were used - LBIC [4] and CAFE [5] - both with

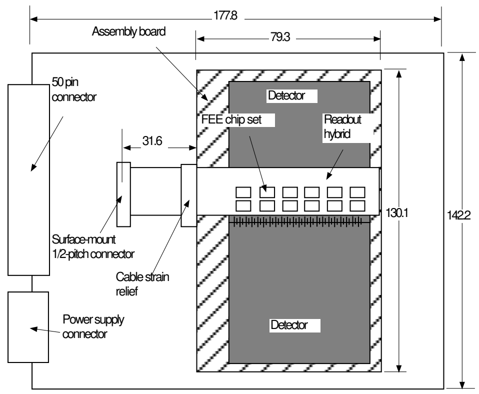


Fig. 1. 12cm-detector module assembled onto the support card. The support card interfaces the signals and power supplies to the detector and front-end electronics (FEE). The module is viewed from upstream. The strips runs vertically.

the same circuit blocks, but differing somewhat in the implementation of the circuitry and manufacturer. The LBIC had 64 channels per chip with a shaper peaking time of about 22 ns, and the CAFE had 128 channels with a peaking time of 25 ns. Both chips were operated at a power of about 1 mW per channel. The CDP128 digital buffer chip was used with both chips, and clocked at 40 MHz. The non-irradiated detector was read out with the LBIC chips and the irradiated detector with CAFE chips.

## IV. Proton irradiation

The detectors were irradiated with 12 GeV protons at the KEK Proton Synchrotron. The detector module was placed upstream of the EP1-A beam line. Typical beam intensity was about $2\times10^{12}$ protons per spill, with a spill every 4 sec. It took about 8 hours to achieve a fluence of $1.2 \times 10^{14}$ p/cm$^2$ uniformly over the detector area of 6 cm × 12 cm. The fluence and its uniformity were measured with the $^7$Be activation method using aluminum foils. The measured fluence was $1.2 \times 10^{14}$ p/cm$^2$ with an error of 5 % due to uncertainties in the activation measurement. Details of the KEK-PS irradiation setup can be found elsewhere [6]. A bias voltage of 50 V was applied to the detectors during the irradiation.

The detector was enclosed in a cold-box cooled with a Peltier thermo unit and kept in the beam area for about 12 days after the irradiation until the end of the beam cycle. For the first 5 days in the beam area the temperature was kept at about 11 °C. Due to a failure in the cooling unit in the last 7 days it went up to about 30 °C and sometimes even higher. After extraction from the beam line, the detector was kept in a freezer at a temperature of -20 °C. During mounting of the electronics hybrid and electronic testing the module was occasionally powered up at room temperature for a total of 40 hr.

The full depletion voltage of the irradiated detector was estimated from the C-V measurements of two other nn75AC detectors irradiated at the same time and kept in the freezer.

The measured full depletion voltage was 210 ± 10 V, which coincides with the predicted full depletion voltage of 200 V according to the parameterization used by H. Ziock et al. [7]. The beneficial short term annealing had finished and the anti-annealing had taken over while the module was still in the beam line. The full depletion voltage of the 12 cm module was estimated to be 250 ± 30 V depending on the temperature of the detector while it was powered up. Because of the warm-up in the beam line and the later powering-up, we call the condition of the irradiated detector "$1.2 \times 10^{14}$ p/cm$^2$ + Warm-up".

## V. BEAMTEST SETUP

The beam test was carried out in the π2 beam line in the 12 GeV proton synchrotron at KEK, using 4 GeV/c negative pions. A set of 5 detector modules was installed in the beam line (Fig. 2): 3 modules, ATT2, ATT4, and UCSC2, to be tested (DUT=device-under-test) and 2 modules, UCSC1 and LBIC2, to define a beam particle track (anchor planes). The module data are summarized in Table 2. The non-irradiated detector module was UCSC2 and the irradiated detector module was ATT4. ATT2 served as an additional comparison device and used DC coupled p-strip on n-bulk detectors fabricated at LBNL, as did LBIC2. The detectors were aligned as shown in Fig. 2 since the instrumented area was different for each detector. To minimize multiple scattering the detectors were mounted as close together as possible in a module-holding crate and rotated as a whole. The rotation was limited to less than 20 degrees to ensure overlap of the detectors.

At the high damage levels that ATT4 was subjected to the detector must be cooled to reduce the leakage current, both to reduce electronic noise and to limit self-heating of the detector, which can lead to thermal runaway. All the detectors were mounted in a cold box and operated at temperatures between -5 and 0 °C in the beam test, cooled by a flow of cold nitrogen gas from the evaporation of liquid nitrogen. The irradiated detector and the non-irradiated detectors could be biased up to 300 V without breakdown failure. The irradiated detector, however, went into thermal runaway at a bias voltage of 280 V, due to cooling limitations.

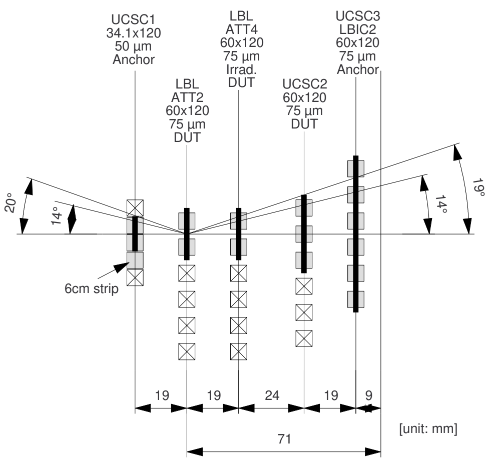


Fig. 2 Detector layout in the cold box, viewed from the top. Beam hits the detectors from the left. Each small box represents a 128 ch FEE chip, and the hatched boxes with thick solid line represent the instrumented region. The character of the detectors are listed at the top of the detectors. The strip length was 12 cm unless otherwise mentioned.

Table 2.
Detector modules used in the beam test

| Name | Readout side | Bulk | Coupling | Pitch [µm] | FE chip | Instrumented chip area |
|---|---|---|---|---|---|---|
| Anchor | | | | | | |
| UCSC1 | n | n | AC | 50 | LBIC | 3 |
| LBIC2 | p | n | DC | 75 | LBIC | 6 |
| DUT | | | | | | |
| ATT2 | p | n | DC | 75 | CAFE | 2 |
| ATT4 | n | n | AC | 75 | CAFE | 2 |
| UCSC2 | n | n | AC | 75 | LBIC | 3 |

Note: ATT4 = detector irradiated, Others = non-irradiated

## VI. RESULTS

The primary goal of the beam test was to evaluate the efficiency, i.e., the ability to detect a charged particle traversing the detector. Three variables are available for this investigation: 1. The bias voltage of the detector, which controls the depletion thickness; 2. The threshold of the binary readout electronics, which sets the efficiency and noise occupancy; and 3. The rotation angle of the detectors, which defines the incident angle of the beam particles and changes the number of strips over which the track's charge is distributed. Varying these settings, efficiency was evaluated for the non-irradiated and the irradiated detectors. Based on previous beam tests[8], a nominal threshold of 1 fC was selected to provide good efficiency at a low noise occupancy.

In the following analysis, the efficiency was defined by the following criteria: 1. Defining hit-clusters. Contiguous hit strips were defined as a hit-cluster. The position of the hit-cluster was the geometrical center of the strips; the center of the strip if it was a single strip hit, the midpoint between two strips when it was a two strip hit, etc. 2. Requiring only one cluster in the upstream and the downstream anchor planes, not adjacent to a dead strip/region, and aligned within 500 µm relative to the incident angle. 3. Finding a hit-cluster in an efficiency window of 500 µm full width centered about the interpolated position from the anchor clusters. In evaluating the noise occupancy, the number of hit strips was counted outside of twice the efficiency window.

### A. *Bias voltage dependence of efficiency*

The full depletion voltages of the non-irradiated and the irradiated detectors were quite different, about 45 V for the non-irradiated and between 200 to 300 V for the irradiated detector. The measured efficiency as a function of the bias voltages is plotted in Fig. 3 at a threshold of 1 fC (we have interpolated the efficiency from the neighboring threshold

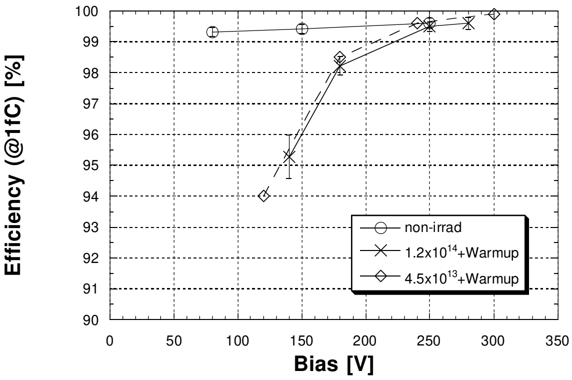


Fig. 3 Efficiency of the non-irradiated (circle) and of the irradiated (cross) detectors as a function of bias voltage at a threshold of 1 fC and at the rotation angle of 0 degrees. Shown together is the n-side of the irradiated double-sided detector (diamond) which bias voltages were scaled assuming the double-sided had a full depletion voltage of 100 V and the irradiated detector 300 V.

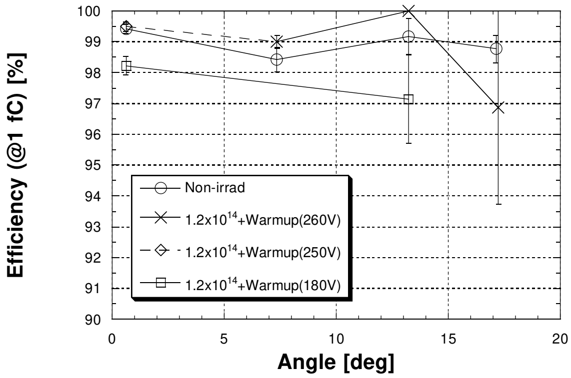


Fig. 4 Angular dependence of the efficiency at a threshold of 1 fC for the non-irradiated and the irradiated detectors with varied bias voltages.

points when the 1 fC threshold was not available) and a rotation angle of 0 degrees. The non-irradiated detector (circle) was very efficient (>99 %) at the bias voltages above 80 V. The irradiated detector (cross) was losing efficiency below 250 V, but was still efficient (>95 %) above 140 V.

Also shown in the figure is the measurement of the n-side efficiency (diamond) of an irradiated double-sided detector taken in a previous beam test [8]. To allow a direct comparison, the bias voltages of this detector were scaled so that the full depletion voltage, taken at 100 V, was to be at 300 V. The good coincidence of two measurements confirms the general trend of the efficiency in the partially depleted regions.

### *B. Angle dependence of efficiency*

The detectors were rotated up to 17 degrees in the cold box. The efficiency variations are plotted in Fig. 4. At large angles the errors were large due to low statistics of tracks. The non-irradiated detector kept high efficiency (>99 %) up to the largest angle. The irradiated detector also kept high efficiency when biased high. Partially depleted operation (>180 V) still gave good efficiency (>97 %) up to the measured angle of 13 degrees.

### *C. Noise occupancy*

Electronic noise is another important aspect of the silicon strip detector and readout electronics chain. The noise can be evaluated from the noise occupancy, i.e., the noise hit rate per strip in a given time slice. The occupancy for a 12 cm strip length and 75 μm pitch was $<2 \times 10^{-4}$ at thresholds >1 fC with the current chip set. No deterioration of the noise occupancy was observed at partial depletion of the irradiated detector. Noise occupancy vs. efficiency at normal incidence for the non-irradiated and the irradiated detectors are shown in Fig. 5. Each data point corresponds to a threshold setting indicated in

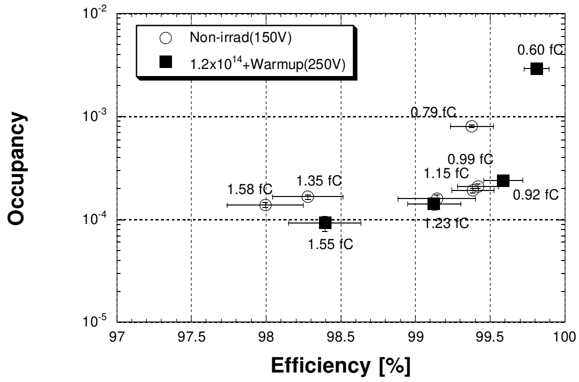


Fig. 5 Efficiency vs. occupancy with the threshold as a parameter. High efficiency was achieved with low noise for the 12 cm strip length.

the figure. High efficiency of >98 % was achieved with a noise occupancy of around $10^{-4}$ up to a threshold of 1.5 fC.

### *D. Insensitive edge region*

The insensitive edge region of the butted detector pair was mapped by rotating the upstream anchor detector, UCSC1, by 90 degrees. This detector had a strip pitch of 50 μm and provided sufficient position resolution to scan the interesting region of the bias resistance of about 230 μm length. The insensitive lengths obtained both for the non-irradiated and the irradiated detectors are shown in Fig. 6. Also shown in the figure is the distance from the one edge of the $n^+$-implant to the implant edge of the adjoining detector measured under the microscope, which was 2210 ± 10 μm. The insensitive regions were 1960~1980 μm and 2140~2170 μm for the non-irradiated and the irradiated detectors respectively. The insensitive region was much narrower in the non-irradiated detector than visually observed. Also, there was a systematic difference between the non-irradiated and the irradiated detectors. The irradiated detector showed the insensitive distance nearly equal to the visually measured.

A schematic drawing of the structures around the polysilicon bias resistance is shown in Fig. 7. Since the strip

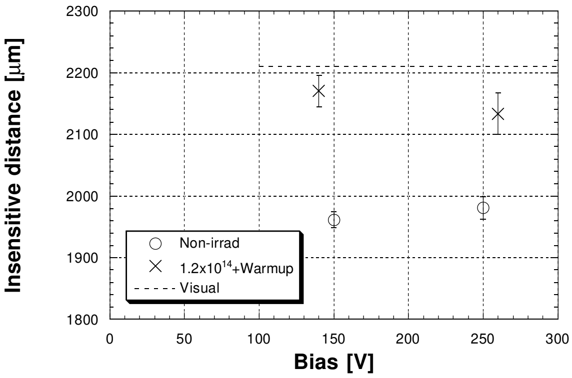


Fig. 6 Insensitive distances measured with the beam: non-irradiated detector (circle) and the irradiated detector (cross). The distance from one edge of the implant to the other edge of the implant strip has been measured visually (2210±10 μm).

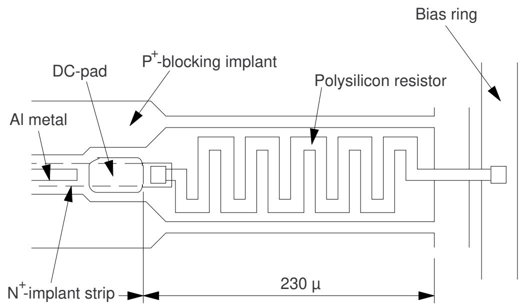


Fig. 7 Structure around the polysilicon bias resistor of the n-side. The $n^+$-implant strip ends at the DC-pad; no $n^+$-implant strip was designed under the bias resistor in this detector.

structure is on the n-side, a $p^+$-blocking implant surrounds the $n^+$-strip. The sensitive distance in the non-irradiated detector was slightly narrower but consistent with the area surrounded by the $p^+$-blocking implant. It seems like that the $n^+$-implant region was extended due to the conductive accumulation layer. When irradiated and type-inverted, the sensitive region was reduced nearly to that of the $n^+$-implant. The effect of the accumulation layer seemed to be limited in this case.

## VII. SUMMARY

A large area (60 mm × 60 mm) n-bulk and n-strip readout silicon strip detector was prototyped for the ATLAS SCT detector. The detector had strips with a 75 μm pitch and AC-coupled readout on the n-side and one lithographed DC pad with guard structure on the backside to form the pre-radiation p-n junction. Detector modules of 12 cm strip length were made by butting two detectors and electrically connecting them by wire-bonding. The strips were read out at the middle of the 12 cm strip with fast bipolar amplifier-shaper-discriminator chips and CMOS digital buffer chips clocked at 40 MHz. One of the modules was irradiated to protons to a fluence of $1.2 \times 10^{14}$ p/cm$^2$ and subsequently experienced some warm-up, which increased the depletion voltage.

A beam test was carried out with the non-irradiated and irradiated detector modules. Efficiency, noise occupancy and the insensitive edge region were analyzed in the beam test data. The detectors were operated at temperatures around -5 °C to 0 °C with the flow of cold nitrogen gas. They sustained bias voltages up to 300 V both for the non-irradiated and the irradiated devices without major breakdown, although the irradiated detector showed thermal runaway at 280 V due to cooling limitations.

The bias voltage dependence of the efficiency showed high efficiency (>99 %) for bias voltages >80 V in the non-irradiated detector (full depletion voltage ~45 V). The irradiated detector showed high efficiency (>95 %) for bias voltages >140 V, which was about half the full depletion voltage. Even for angled tracks up to 13 degrees incident angle the efficiency was high (>98 %) at partial depletion (>180 V). The noise occupancy was low ($<2 \times 10^{-4}$) for thresholds >1 fC.

The measurement at the edge region exhibited a difference in the sensitivity beneath the bias resistance where no extension of the $n^+$-implant was fabricated: the non-irradiated detector showed good sensitivity while the irradiated detector did not. The effect of the electron accumulation layer would be limited in the irradiated detector compared to that of the non-irradiated case.

## VIII. ACKNOWLEDGMENTS

The authors thank the ATLAS SCT collaboration for the use of the DAQ hardware and to the operation staff of the KEK EP1A beam line for the proton irradiation. One of the authors, G. Moorhead, thanks especially to the Foundation for High-Energy Accelerator Science for his travel fund. The work is supported in part by DOE and the US-Japan Scientific cooperation program.

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