Beam Test of a Large Area n-on-n Silicon Strip Detector with Fast Binary Readout Electronics

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Abstract

A large area (60 mm × 60 mm) n-bulk and n-strip readout silicon strip detector was prototyped for the ATLAS SCT detector. Detector modules of 12 cm strip length were made by butting two detectors. One of the 12 cm module was irradiated to protons to a fluence of 1.2×10^{14} p/cm^2. A beam test was carried out for the non-irradiated and the irradiated detector modules. Efficiency, noise occupancy and edge insensitive region were analyzed in the beam test data. The bias voltage dependence of the efficiency showed high efficiency in the non-irradiated detector, and the irradiated detector for the bias voltages which was about half the full depletion voltage. Even for the angled tracks the efficiency was high for the partial depletion operation. The noise occupancy was low (<2×10^{-4}) for the 12 cm strips. The measurement of the edge region exhibited clear difference of the sensitivity under the bias resistance where no extension of the n$^+$-implant was fabricated: the non-irradiated detector showed sensitivity while the irradiated detector did not. The result was also confirmed with the laser light.

I. INTRODUCTION

A large area (60 mm × 60 mm), n-bulk and n-strip readout silicon strip detector was fabricated to prototype a detector for the ATLAS Semiconductor Tracker (SCT)[1]. The ordinary silicon strip detector is to read out p-strips on n-bulk silicon wafer. The choice of the n-strip readout on n-bulk wafer is based on a thought that the p-n junction will be n-side after the so-called type inversion when the silicon bulk has accumulated a fluence more than a several times 10^{13} particles/cm^2. The SCT silicon strip detector is expected to accumulate more than 10^{14} p/cm^2 in 10 years of operation, and the full depletion voltage would be near 300 V at a fluence of 2×10^{14} p/cm^2 in the best case when the detector were cooled around -10 °C all over the lifetime to suppress the so-called anti-annealing effect of the radiation damage to the bulk. The readout from the p-n junction side will allow an operation without depleting the silicon bulk fully, thus allowing to apply a bias voltage of 200 V for example, after the type inversion and heavily damaged, for easing the overall design of the silicon strip detector and the detector module including the electronics and peripherals.

The n-on-n detector is readout from the strips on one-side, thus it is a single-sided detector from the readout point of view. Semiconductor process wise, it is a double-sided process because the backside, which has to be the p-n junction side initially, also has to be processed. Since the p-n junction moves from the p-side, which is the initial non-irradiated case, to the n-side after the type inversion, it is of interest to test the detector in both cases and evaluate its tracking performance to the charged particles.

The edge of the readout implant strip (n$^+$) ends about 1 mm from the dicing edge of the detector. More in detail, the one side of the strip has a bias resistor made of polysilicon trace. Usually the implant strip extends under the polysilicon resistor to maximize the sensitive region. The prototype detector used in this beam test had no extension and the n$^+$-implant strip ends near the connection of the polysilicon resistor to the implant strip. In the n-side, the positive oxide charge in the silicon bulk and the silicon dioxide (SiO_2) interface is said to create the electron accumulation layer in the surface of the silicon bulk and electrically shorts the neighboring strips, thus requiring a p-implant to cut the accumulation layer. The n-side of this detector has the lithographed p-stop implantation. Although the n$^+$-implant has a limited area, it may extends to the edge of the p-stop implantation because of the accumulation layer. The sensitivity of the area under the polysilicon resistor would give an insight to the understanding.

II. N-STRIP ON N-BULK DETECTOR

One large area (60 mm × 60 mm), n-bulk and n-strip readout silicon strip detector was fabricated out of one 4-inch wafer[2]. The n-on-n detector has semiconductor manufacturing process not only in the n-side but also in the p-side to make the p-n junction in the planar geometry. One detector out of one wafer and the double-sided process is a challenge for the manufacturer by itself with respect to the yield of the fabrication. The specification of the detector is summarized in Table 1.

The resistivity of the bulk was specified to have the minimum and the maximum; the minimum was set not to have too high full depletion voltage and the maximum was set to keep the junction breakdown not to be low. The p-side had a large area of p-n junction which was lithographed to have a bias-potential holding structure to the dicing edge and was covered by aluminum metal to make one large area DC-contact pad.

The n^+-implant strips were laid out to have a strip pitch of 75 micron. The strips were AC-coupled to the aluminum readout metal strips with a double-layer structure of insulating materials (silicon dioxide(SiO_2) and silicon nitride(SiN)) to suppress the eventual pin-holes in the insulator. Each n^+-implant strips were separated with continuous-piece of common p^+-stop implantation. The width of the n^+-implant strip of 16 µm was chosen to give a reasonably low inter-strip capacitance, which is the major factor of the intrinsic equivalent noise charge (ENC) of the detector. The width of the p-stop was determined by leaving a space between the n-implant and the p-stop of 8 µm which space allowed a mask alignment error of 1 µm and yet keeping a good separation of the n-implant and the p-implant.

The n-implant strips were connected to the n-bias rail surrounding the n-strip area through a bias resistor made of polysilicon material. The value of 1 MΩ was chosen to give an acceptable voltage drop for the leakage current at the operating temperature of -10 °C when heavily damaged, and yet to give a low ENC due to the resistance. Total number of readout strips was 768 which was for the 6 readout chips with 128 channels each. We called the detector "nn75AC" representing the character of the detector.

Table 1 Specification of the n-on-n single-sided silicon strip detector (nn75AC)

Detector type:	n-bulk, n-strip, AC-coupled, Single-sided
Bulk type:	n-bulk
Resistivity:	4~8 kΩcm
Size (Outer):	6 cm × 6cm
p-side structure:	DC-coupled pad junction breakdown ≥300V
n-side structure:	active-to-edge insensitive area ≤ 1.0 mm polysilicon bias resistor: 1.0±0.2 MΩ AC-coupling: SiO_2 0.25µm+SiN 0.05µm Interstrip capacitance ≤10 pF/6cm
strip isolation:	continuos floating p-stop
Strip parameters:	
Strip pitch:	75 µm
Readout pitch:	75 µm
Implant width:	16 µm
Width of Al readout:	16 µm
p-stop width:	43 µm
gap between implants:	8 µm
Al thickness:	1.5 µm
Resistance of Al readout:	≤20 Ω/cm
Resistance of implant	≤100kΩ/cm
DC-contact to implant	contact hole/pad
Number of strips:	(128×6=768 readouts) + 6 dummies
Sensitive width:	768×75µm = 57.6 µm
Leakage current:	Total including guard <25µA at 200V Per strip <50nA at 200V

III. 12 CM MODULES

Using two of the nn75AC detectors, a detector module with a strip length of 12 cm was made for the beam test (Fig. 1). Two detectors were butted and 6 cm strips were wire-bonded to be a 12 cm strip. The readout front-end electronics was carried on a hybrid traversing the detector near the middle of the 12 cm detector unit to contact the strips in the shortest distance and to read out in the middle. This geometry minimizes the inter-strip coupling due to the extra lines connecting the strips to the electronics and the ENC due to the strip resistance. The hybrid was connected to the PC board called "Support card" which carried the detector and interfaced the signal cables and the power lines to the back-end electronics sitting in the counting hut separated about 20 m. The module was equipped with two detectors reading out in one coordinate thus a single-sided module. Two modules were tested: one module with non-irradiated detectors, and the other with detectors irradiated to protons at a fluence of 1.2×10^{14} p/cm^2.

The readout front-end electronics was made out of pair of two chips: the front chip was a bipolar LSI which functioned as a fast amplifier, shaper, and discriminator to make the signal pulses to on-off signals, and the back LSI was a CMOS digital buffer to allow pipelining of the signals. Two kind of bipolar chips were used: one was named LBIC[3] and the other ATT[4], different implementation of the circuitry and the manufacturer. The LBIC had a shaper peaking time of about 22 ns, and the ATT about 35 ns with time-walk compensation circuitry. The digital buffer chip called CDP128 was used for both chips and clocked at 40 MHz. The non-irradiated detector was readout with the LBIC chips and the irradiated detector with the ATT chips. The readout system is called "Fast binary readout electronics".

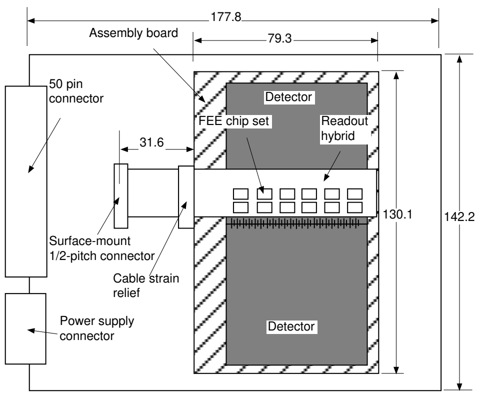

Fig. 1 12cm-detector module assembled onto the support card which interfaces the signals and power supplies to the detector and front-end electronics (FEE). The view corresponds when the module is looked from upstream. The strips runs vertically.

IV. PROTON IRRADIATION

The detector module(ATT) was irradiated with 12 GeV protons at the KEK Proton Synchrotron in order to investigate an effect of a radiation damage due to high fluence of high energy protons. The detector module was placed at an upstream of the EP1-A beam line in the north experimental hall of the KEK-PS. Typical beam intensity was about 2×10^{12} protons per spill in every 4 sec. The FWHM of the beam size was about 5 cm (horizontal) × 3 cm (vertical). It took about 8 hours to achieve a fluence of 1.2×10^{14} p/cm^2 uniformly over the detector area of 6 cm × 12 cm. The fluence and its uniformity were measured with the ^{7}Be activation method using aluminum foils. The measured fluence was 1.2×10^{14} p/cm^2 with an error of 5 % dominated by the calibration of SSD used for the measurement of activation. The uniformity over the 12 cm length was less than 8 % except one of the far-ends. Details of a KEK-PS irradiation can be found elsewhere[5]. A bias voltage of 50 V was applied to the detector during the irradiation.

The detector was enclosed in a thermo-box cooled with a Peltier thermo unit and kept in the beam area for about 12 days after the irradiation until the end of the beam cycle. The first 5 days in the beam area the temperature was kept at about 11 ˚C but in the last 7 days it went up to about 32 ˚C or sometimes even higher because of a malfunctioning of the thermo unit. After extracting the beam line, the detector was kept in a freezer at a temperature of around -20 °C, occasionally powered up in a room temperature to test the module for a total of one day long before the beam test.

The full depletion voltage of the irradiated detector was estimated from the C-V measurements of two other nn75AC detectors irradiated at the same time and kept in the freezer. The measured full depletion voltage was 210 ± 10 V, which coincides with the predicted full depletion voltage of 200 V according to the H. Ziock parameterization[6], with the fluence, the temperature history, and a multiplication factor of 1.1 for the planar to strip geometry. The beneficial short term annealing had finished and the anti-annealing had took over while it was in the beam line. The full depletion voltage of the 12 cm module was estimated to be 250 ± 30 V depending on the temperature of the detector while it was powered up. Because of the warm-up in the beam line and the powered-up, we call the condition of the irradiated detector as "1.2×10^{14} p/cm^2 + Warmup".

V. BEAMTEST SETUP

The beam test was carried out in the π2 beam line in the 12 GeV proton synchroton at KEK, using 4 GeV/c negative pions. A set of 5 detector modules were aligned in the beam line (Fig. 2): 3 modules, ATT2, ATT4, and UCSC2, to be tested (DUT=device-under-test) and 2 modules, UCSC1 and LBIC2, to define a beam particle passage (Anchor). The non-irradiated detector module was UCSC2 and the irradiated detector module was ATT4. Detector type, pitch, and readout chip are summarized in Table 2. Since the instrumented area were different detector by detector, the detectors were aligned as in the figure. To minimize the multiple scattering the detectors were set as close as possible in a module holding crate and rotated as a whole. The rotation was limited less than 20 degrees to have overlap of the detectors.

Since the irradiated detector drew a large leakage current, the detector was required to be cooled to prevent thermal runaway and to reduce the amount of the leakage current. All the detectors were set in a cold box and operated at temperatures between -5 and 0 °C in the beam test, cooled with a flow of cold nitrogen gas from the evaporation of the liquid nitrogen. No humidity control was provided in the cold box. The irradiated detector and the non-irradiated detectors were biased up to 300 V without breakdown failure. The irradiated detector, however, showed a thermal runaway at a bias voltage of 280 V. Typical leakage currents of the detectors were about 1 µA in the UCSC2 and about 3 mA in the ATT4 at a bias voltage of 200 V in the operating condition.

Table 2. Detector modules used in the beam test

Name	Readout side	Bulk	Coupling	Pitch [µm]	FE chip	Instrumented chip area
Anchor						
UCSC1	n	n	AC	50	LBIC	3
LBIC2	p	n	DC	75	LBIC	6
DUT						
ATT2	p	n	DC	75	ATT	2
ATT4	n	n	AC	75	ATT	2
UCSC2	n	n	AC	75	LBIC	3

Note: ATT4 = irradiated, Others = non-irradiated

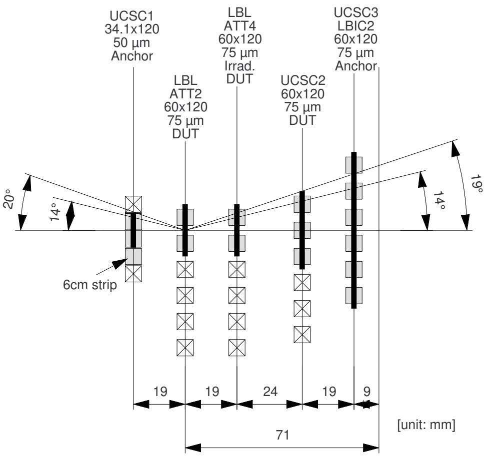

Fig. 2 Detector layout in the cold box, viewed from the top. Beam hit the detectors from the left. Each small box represents a 128 ch FEE chip, and the hatched boxes with thick solid line represent the instrumented region. The character of the detectors are listed at the top of the detectors. The strip length was 12 cm otherwise mentioned.

VI. RESULTS

The primary goal of the beam test was to evaluate the efficiency, i.e., the ability to detect a charged particle traversing the detector. Variables of the beam test were the bias voltage of the detector controlling the depletion of the bulk, the threshold of the binary readout electronics, and the rotation angle of the detectors defining the incident angle of the beam particles to the detector which in turn controlled the sharing of a track path, i.e., the electron/hole charges, to the strips. Varying these settings, efficiency was evaluated for the non-irradiated and the irradiated detectors. From the previous beam tests[7] a threshold of 1 fC was thought to be a reasonable choice in maximizing the efficiency and minimizing the noise occupancy.

In the following analysis, the efficiency was defined as in the following criteria: (1) Defining hit-clusters. A consecutive hit strips were clustered and defined as a hit-cluster. The position of the hit-cluster was the geometrical center of the strips; center of the strip if it was a single strip hit, middle of the two strips when it was a two strip hit, etc.; (2) Requiring only one cluster in the upstream and the downstream anchor planes, not being adjacent to a dead strip/region, and they were aligned within 500 μm relative to the incident angle; (3) Whether a hit-cluster was found in an efficiency window of 500 μm full width which center was the interpolated position from the anchor clusters. In evaluating the noise occupancy, number of hit strips was counted for those which were outside of twice the efficiency window.

Particularly interesting in this beam test was the evaluation of the edge insensitive region where two detectors were butted. There was the insensitive region of about 1 mm surrounding edge of the each detector: about 2 mm in total. In addition to this insensitive region, no n^+ implantation was designed under the bias resistance of a length of about 200 μm in this detector.

A. *Bias voltage dependence of efficiency*

The full depletion voltages of the non-irradiated and the irradiated detectors were quite different, in addition to the side of the p-n junction. It was about 70 V for the non-irradiated and between 200 to 300 V for the irradiated detector. The measured efficiency variation as a function of the bias voltages is plotted in Fig. 3 at a threshold of 1 fC (we have interpolated the efficiency from the neighboring thresholds when the 1fC threshold was not available) and the rotation angle at 0 degree. The non-irradiated detector (circle) was very efficient (>99 %) at the bias voltages above 80 V. The irradiated detector (cross) was losing efficiency below 250 V, but was still efficient (>95 %) above 140 V.

Shown together in the figure is the measurement of the n-side efficiency (diamond) of the irradiated double-sided detector in the previous beam test [ref. 7], which bias voltages were scaled by taking the full depletion voltage of the irradiated double-sided detector at 100 V and the irradiated detector of this beam test at 300 V. The good coincidence of two measurements confirms the general trend of the efficiency in the partially depleted regions. Ambiguity in the full depletion voltage would be enhanced by the ambiguity of threshold calibration.

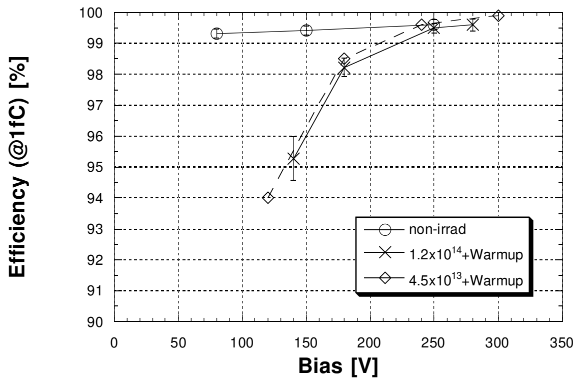

Fig. 3 Variation of the efficiency of the non-irradiated (circle) and of the irradiated (cross)as a function of bias voltage at a threshold of 1 fC and at the rotation angle of 0 degree. Shown together is the n-side of the irradiated double-sided detector (diamond) which bias voltages were scaled assuming the double-sided had a full depletion voltage of 100 V and the irradiated detector had 300 V.

B. *Angle dependence of efficiency*

The detectors were rotated up to 17 degrees in the cold box. The efficiency variations were plotted in Fig. 4. In large angles the errors were large due to low statistics of tracks. The non-irradiated detector kept high efficiency (>99 %) up to the largest angle. The irradiated detector also kept high efficiency when biased high. Partially depleted operation (>180 V) still gave good efficiency (>97 %) up to the measured angle of 13 degrees.

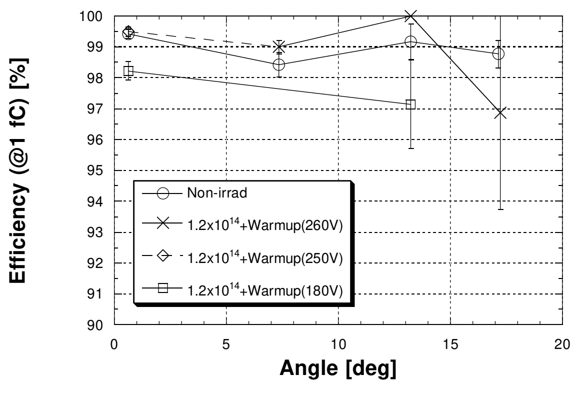

Fig. 4 Angular dependence of the efficiency at a threshold of 1 fC for the non-irradiated and the irradiated detectors with varied bias voltages.

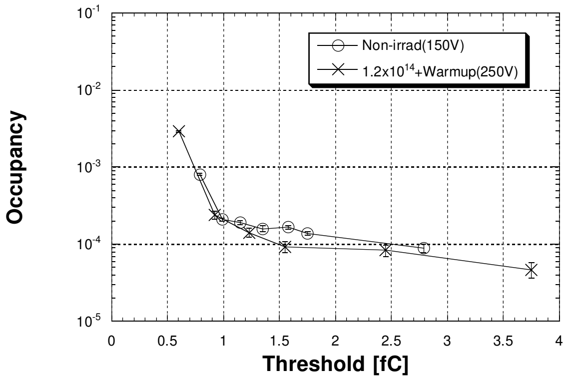

Fig. 5 Noise occupancy as a function of threshold. The noises above 1 fC are a component other than the intrinsic Gaussian noise. The occupancy will be reduced with a new "edge-sensitive" digital buffer by the "lifetime" reduction factor for the chips (LBIC=0.6, CAFE=2.5).

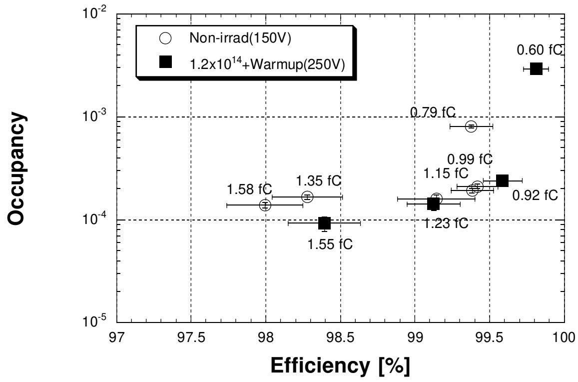

Fig. 6 Efficiency vs. occupancy with the threshold as a parameter. High efficiency was achieved with low noise for the 12 cm strip length. The occupancy will be reduced with a new "edge-sensitive" digital buffer by the "lifetime" reduction factor for the chips (LBIC=0.6, CAFE=2.5).

C. Noise occupancy

Electrical noise is another important aspect of the silicon strip detector and readout electronics chain. The noise can be evaluated as a form of noise occupancy which is a hit rate in a strip with noise. The occupancy is the direct measure in the real experiment. The noise occupancy is plotted in Fig. 5 as a function of thresholds. There were two components in the noise occupancy: below 1 fC the occupancy was dominated by the intrinsic noise of sigma of 0.2 ~ 0.25 fC (1250 ~ 1550 e), above 1 fC there was another component which was associated with the track hits. The occupancy of the 12 cm strip in the 75 μm pitch was $<2 \times 10^{-4}$ in >1 fC with the current chip set.

The CDP128 was designed to be "level-sensitive" in which signals above a threshold ("life time") is counted in every clock cycles. A new digital buffer design which will be "edge-sensitive" will reduce the occupancy of the ATT chips, by a factor of 2.5 together with a new CAFE chip[8] with a faster and symmetrical pulse shaping envisaged. The LBIC chip will, on the contrary, increase the noise by a reduction factor of 0.6.

Performance of the binary readout electronics is shown in Fig. 6 in a scatter plot of the efficiency and the noise occupancy at a bias voltage shown in the figure and at a rotation angle of 0 degree. Each data point corresponds to a threshold setting associated in the figure. High efficiency of >98 % was achieved with a noise occupancy level of around 10^{-4} up to the threshold of 1.5 fC.

D. Edge insensitive region

The edge insensitive region of the butted two detectors was mapped by rotating the upstream anchor detector, UCSC1, by 90 degrees. The detector had a strip pitch of 50 μm and was good enough to scan the interested region of the bias resistance of about 200 μm. Coincidence of the anchor and the non-irradiated DUT detector, UCSC2, is shown in Fig. 7. The insensitive edge region of about 2 mm was clearly observed. By fitting the error function, an insensitive distance of 1961 ± 13 μm was obtained.

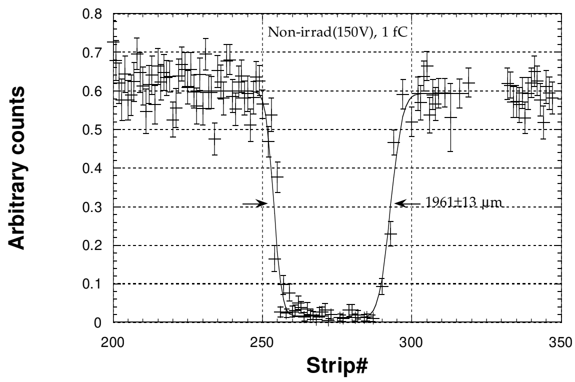

Fig. 7 Edge insensitive region where two detectors were butted. The region was mapped with a 50 μm pitch strip detector orthogonally aligned to the non-irradiated DUT detector. One detector had about 1 mm edge space.

The insensitive distances were obtained both for the non-irradiated and the irradiated detectors and are shown in Fig. 8. Together shown in the figure is the distance of the one edge of the n^+-implant to the other edge of the implant measured under the microscope which was 2210 ± 10 μm for both detectors.

The insensitive regions were 1960~1980 μm and 2140~2170 μm for the non-irradiated and the irradiated detectors respectively. The insensitive region was much narrower in the non-irradiated detector than the visual inspection. Also, there was systematic difference between the non-irradiated and the irradiated detectors. The irradiated detector showed the insensitive distance nearly equal to the visually measured.

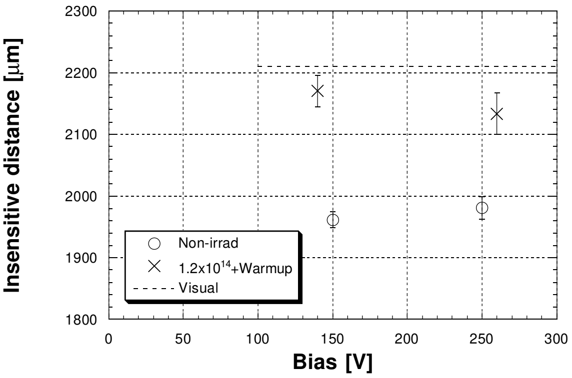

Fig. 8 Insensitive distances measured with the beam: non-irradiated detector (circle) and the irradiated detector (cross). The distance from one edge of the implant to the other edge of the implant strip has been measured visually (2210±10 μm).

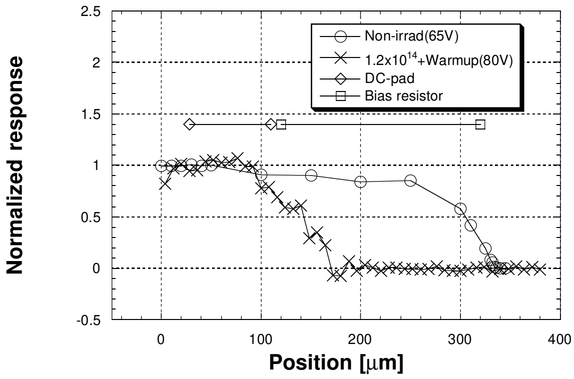

Fig. 10 The charge collection under the bias resistor where no n^+-implant strip was fabricated has been measured by using a laser light (1064 nm). The laser response was obtained for non-irradiated (circle) and the irradiated (cross) detectors. The areas of the bias resistance (square) and the DC-pad (diamond) are shown together.

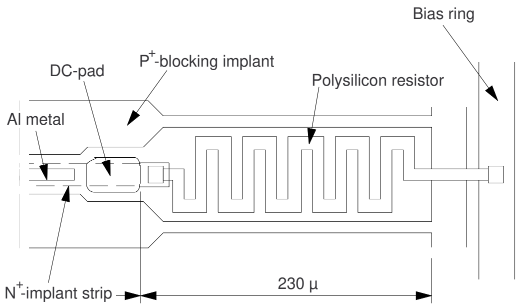

Fig. 9 Structure around the polysilicon bias resistor of the n-side. The n^+-implant strip ends at the DC-pad; no n^+-implant strip was designed under the bias resistor in this detector.

A schematic drawing of the structures around the polysilicon bias resistance is shown in Fig. 9. Since the strip structure was on the n-side, a p^+-blocking implant was surrounding the n^+-strip and the polysilicon resistor. The sensitive distance was slightly narrower but consistent with the surrounded area with the p^+-blocking implant when it was non-irradiated. When irradiated and type-inverted, the sensitive region was reduced nearly to that of the n^+-implant. Because of the high resistivity of the accumulation layer and the large leakage current in the irradiated detector, the electric field might extends much less than that of the non-irradiated detector from the n^+-implant to the p^+-blocking implant.

Since the observation was very interesting with respect to the surface of the non-irradiated and the irradiated detector, the sensitivity under the bias resistance was measured with a laser light (1064 nm) scanning equipment[9] for the non-irradiated and the irradiated detectors from the same batch and the same irradiation. The responses are shown in Fig. 10 for the two detectors. There was clear difference: the non-irradiated detector showed sensitivity under the bias resistance although there was no n^+-implant strip, while the irradiated detector showed almost no sensitivity; thus confirmed the observation of the beam test.

VII. SUMMARY

A large area (60 mm × 60 mm) n-bulk and n-strip readout silicon strip detector was prototyped for the ATLAS SCT detector. The detector had strips with a 75 micron pitch and AC-coupled readout on the n-side and one lithographed p-DC pad in the backside to make the p-n junction. Detector modules of 12 cm strip length were made by butting two detectors and electrically connected with wire-bonding. The strips were read out at the middle of the strip with pairs of fast bipolar amplifier-shaper-discriminator chips and CMOS digital buffer chips clocked at 40 MHz. One of the 12 cm module was irradiated to protons to a fluence of 1.2×10^{14} p/cm^2, which then experienced warm-up after the irradiation.

A beam test was carried out for the non-irradiated and the irradiated detector modules. Efficiency, noise occupancy and edge insensitive region were analyzed in the beam test data. The bias voltage dependence of the efficiency showed high efficiency (>99 %) for the bias voltages (>80 V) in the non-irradiated detector (full depletion voltage ~70 V). The irradiated detector showed high efficiency (>95 %) for the bias voltages (>140 V) which was about half the full depletion voltage. Even for the angled tracks (<13 degrees) the efficiency was high (>98 %) for the partial depletion (>180 V) operation. The noise occupancy was low ($<2 \times 10^{-4}$) above the threshold of >1 fC for the 12 cm strips.

The measurement of the edge region exhibited clear difference of the sensitivity under the bias resistance where no extension of the n^+-implant was fabricated: the non-irradiated detector showed sensitivity while the irradiated detector did not. The result was also confirmed with the laser light. The effect of the electron accumulation layer was limited in area in the irradiated detector than that of the non-irradiated case.

The detectors were operated at temperatures around -5 °C to 0 °C with the flow of cold nitrogen gas and sustained the bias voltage up to 300 V both for the non-irradiated and the irradiated cases without major breakdown, though the irradiated detector showed a thermal runaway at 280 V.

VIII. ACKNOWLEDGMENT

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IX. REFERENCES

[1] ATLAS collaboration, Technical proposal, CERN/LHCC/94-43, 1994

[2] Hamamatsu photonics, Ichino-cho, Hamamatsu 435, Japan

[3] E. Spencer et al., IEEE Trans. Nucl. Sci. 42(1995)796

[4] I. Kipnis et al., IEEE Trans. Nucl. Sci. 41(1995)1095

[5] S. Terada et al., KEK Preprint 96-77, 1996, to be published in Nucl. Instr. Meth.

[6] H. Ziock et al., Nucl. Instr. Meth. A342(1994)96

[7] Y. Unno et al., IEEE Trans. Nucl. Sci. 43(1996)1175; and KEK preprint 96-7, to be published in Nucl. Instr. Meth.

[8] I. Kipnis et al., CAFE: A complementary bipolar analog front-end integrated circuit for the ATLAS SCT.

[9] Y. Unno et al., KEK preprint 95-197, to be published in Nucl. Instr. Meth.