Evaluation of p-stop structures in the n-side of n-on-n silicon strip detectors

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Abstract--Large area (63.6 mm x 64 mm) n-on-n silicon strip detectors have been fabricated, implementing various p-stop structures in the n-side. The detectors were characterized in laboratory and in beamtests. The beamtests showed that the individual p-stop structure collected less charge in the region between the strips than other p-stop structures.

I. Introduction

Large area n-on-n silicon strip detectors were fabricated out of 4-inch silicon wafers. They consisted of n-implant strips in n-bulk silicon for the segmented readout and a large p-pad in the backside for the initial p-n junction. The detector was designed to function, in the heavy radiation environment such as LHC, well after the type inversion of the silicon bulk and the large increase of the depletion voltage [1].

Initially and even after the type inversion, the surface of the n-side is known to have n-type characteristics due to the accumulation layer of electrons in the interface of the surface oxide and the bulk. This accumulation layer is conductive and shorts the n-strips unless the n-strips are isolated with a p-implant structure surrounding the n-strips. A conventional way is to implant all-over the surface leaving openings for the n-strips (Full-common p-stop structure).

The p-implant has a finite resistivity and the continuous p-implant may couple neighbouring n-strips capacitively. A new type of p-stop structure was proposed by isolating the p-implant individually (Individual p-stop structure) [2]. The individual p-stop structure separates the n-strips but there remains an accumulation layer outside the p-stops which is continuous over the whole surface. A modified version has been proposed, which splits each n-strip region into a cell with a narrow p-implant line and place the individual p-stop frame within the cell (Combined p-stop structure) [3]. This structure will cut the continuous accumulation layer.

The prototype detectors were fabricated with six regions of these p-stop structures. We evaluated the p-stop structures for interstrip capacitance, efficiency, charge-collection and noise performance.

II. N-on-N Silicon Strip Detector

A. Detector

The specification of the fabricated detector is summarized in Table I. The silicon strip detector was named “nn80AC” since the detector had n-strips on n-bulk, a strip pitch of 80 μm, and an AC coupling readout configuration. The detector had 768 readout strips divided into 6 zones with 128 strips per zone. The zones had combinations of p-stop structure and width of readout metal as listed in Table II. Zones 1 to 4 had the same strip and metal width but different p-stop structures. Zones 4 to 6 had the same p-stop structure but different metal widths. The different metal width is irrelevant in this analysis.

The detector, p-stop structures, and strip widths are indicated schematically in Fig. 1. The p-stop structures of interest were Zones 2 (Individual), 3 (Combined), and 4 (Full-common). Zone 1 (Slit-common) was implemented to differentiate the effect of continuous and interrupted accumulation layers.

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Table I

Specification of the n-on-n single-sided silicon strip detector (nn80AC)

Detector type:	N-bulk, n-strip, AC-coupled, Single-sided
Bulk type:	N-bulk
Resistivity:	4~8 kΩcm
Size (Outer):	6.36 cm × 6.4cm (width × length)
N-sensitive area:	Width: 770 × 80µm =61.6 mm
	Length: 62 mm
P-side structure:	DC-coupled pad
	Junction breakdown ≥300V
Surface protection	SiO_2 passivation
Number of N-strips:	(128 × 6 zones=768 readouts)+2 dummies
N-strip isolation:	Various p-stop structures (Table II)
N-strip parameters:	
Polysilicon bias resistor:	1.5±0.5 MΩ
Strip pitch:	80 µm
Readout pitch:	80 µm
Implant width:	16 µm
Width of Al. readout:	16 µm, and others (Table II)
P-stop width:	43 µm, and others (Table II)
Al. thickness:	1.5 µm
Resistance of Al. readout:	≤20 Ω/cm
Resistance of implant:	≤100kΩ/cm
AC-coupling:	SiO_2 0.25µm+SiN 0.05µm

Table II

N-implant and p-stop widths

Zone	P-stop structure	Metal [µm]	P-stop [µm]	No. strips
1	Slit-common	16 µ	2 x 18 µ	128
2	Individual	16 µ	2 x 18 µ	128
3	Combined	16 µ	2 x 11 µ + 6 µ	128
4	Full-common	16 µ	44 µ	128
5	Full-common	22 µ	44 µ	128
6	Full-common	10 µ	44 µ	128

B. Modules

In order to measure the efficiency, charge collection, and noise, two "modules" were constructed using the detectors and a set of readout LSI's: LBIC for the preamplification, shaping, and discrimination, and CDP for buffering the on-off binary hit pattern [4]. One type of module was made by placing the readout hybrids near the middle of the detectors as shown in Fig.2, called the "Centre-tap" module. The other design was made by placing the hybrids at one end of detectors, called the "End-tap" design. The data presented in this paper come from both modules.

In the modules two sets of two detectors were glued on top and bottom of a heat conducting baseboard. Two detectors on one side were daisy-chained to make a strip length of 12 cm. The heat conducting baseboard was prototyped with a pyrolytic graphite (PG700) which had a high thermal conductivity, about 300 W/m/K [5]. The top and the bottom detectors were rotated by 40 mrad relative to each other to make a stereo measurement of the positions of passing charged particles. The module was attached to an external PC board which also carried electronics to transmit and receive the signals over 20 m distance from the module to the backend electronics.

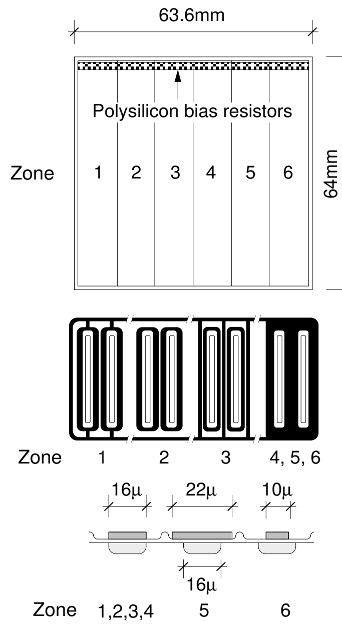

Fig.1 Schematic diagram of the detector (top), p-stop structures (middle), and strip widths (bottom). Zones are: 1=Slit-common, 2=Individual, 3=Combined, 4, 5, 6=Full-common (metal=16, 22, 10 µm, respectively)

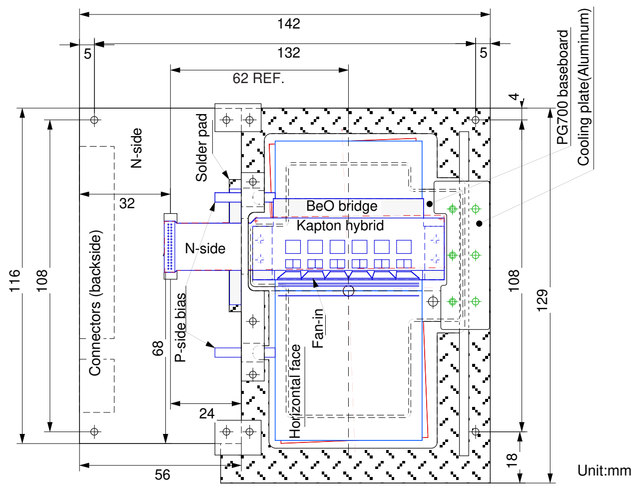

Fig.2 "Centre-tap" module, mounted on a PC board for data communication. Strip runs vertically. The bottom detectors were rotated 40 mrad to the top detectors. A pitch-adapting "Fan-in" was used to match the strip pitch of 80 µm and the pad pitch of 43 µm of LBIC's.

III. Measurements

A. Interstrip capacitance

In order to characterize and compare the zones, capacitance between the strips, so-called "interstrip capacitance", was measured for one strip relative to 24 strips total in adjacent neighbours, i.e., 12 strips per side. The results for Zones, 1 to 4, are shown in Fig.3. There were systematic errors of at most 0.5 pF in the measurement.

A strong variation of the interstrip capacitance was observed below 60 volts bias voltage. This is an indication that below depletion the n-side is shorted.

Above this bias voltage, the interstrip capacitances decreased slowly. They did not show saturation even at 200 volts. There are two sources which may cause the slow decrease. One is the p-stop implant. Although it is shallow, it requires the electric field to deplete. The other is an accumulation layer in the interface of the passivation oxide and the bulk. The oxide-bulk interface contains interface states which are charged up positively and attract electrons which form a conductive accumulation layer. Apart from the global behaviour, the individual and the combined p-stop structures had the least capacitance.

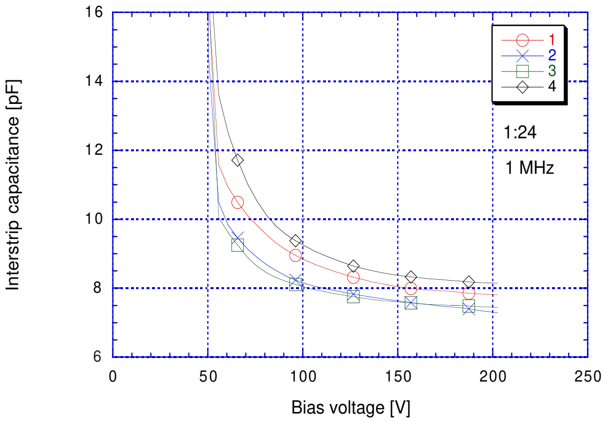

Fig.3 Inter-strip capacitances in Zones 1(slit-common), 2(individual), 3(combined), and 4(full-common), measured at 1 MHz and 1 strip against neighbour 24 strips. The slow decrease of the capacitance above 60 volts is a reflection of conductive layer between the n-strips.

B. Beamtests

Two beamtests were carried out for the fabricated modules using 4 GeV/c pions from the 12 GeV proton synchrotron at KEK. Two modules were sandwiched with high precision silicon-strip detector "telescopes". The distance between the telescopes was about 74 mm and the two modules were placed at near equal spacing. Incident particles were triggered by the coincidence of three scintillation counters with an area of 20 mm x 20 mm.

Each telescope module was made of two single-sided strip detectors with their strips in orthogonal directions: one was in the horizontal direction, X, and the other in the vertical direction, Y. The silicon-strip detector was made of an implant strip pitch of 25 µm and a readout pitch of 50 µm. The sensitive region was 19.2 mm x 19.2 mm with a number of readout channels being 384. Signal pulse heights were read out and the resulting spatial resolution was about 5 µm [6].

Data were collected at bias voltages of 80, 120, 160, and 200 volts. Threshold voltage of the discriminator was varied and expressed in charge in the unit of femto-Coulomb (fC) according to a common calibration curve.

C. Response in the strip and mid-strip regions

Instead of relying on the electronics calibration of the different zones, the gain of the different zones was obtained in a in-situ calibration with the beam by assuming that the charge collection near the readout strip was the same in different zones at a very high bias voltage.

In order to define the near -strip region, the efficiency for detecting particles was mapped out between two readout strips. The detection efficiency was defined by counting hits or clusters of hits within ±250 µm from the interpolated position of a track given by the precision telescope hits. An example of the plot is shown in Fig.4. Although less pronounced at low thresholds, the loss of efficiency in the region between the strips was evident in the high threshold. By fitting a Gaussian, the "mid-strip" region was defined with a full-width of 20 µm around the minimum. The "strip" region was defined with a full-width of 40 µm around the complementary point to the minimum, which left 10 µm gap between the strip and the mid-strip regions. The definition was made for one high threshold at 200 volts and applied to other thresholds and bias voltages uniquely.

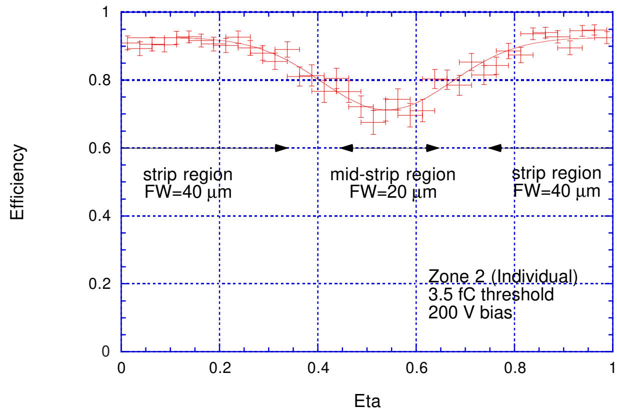

Fig.4 Efficiency plot between two strips. The minimum was obtained by fitting Gaussian. The mid-strip region was defined around the minimum with a full width of 20 µm. The strip region was defined around the complementary point to the minimum with a full width of 40 µm.

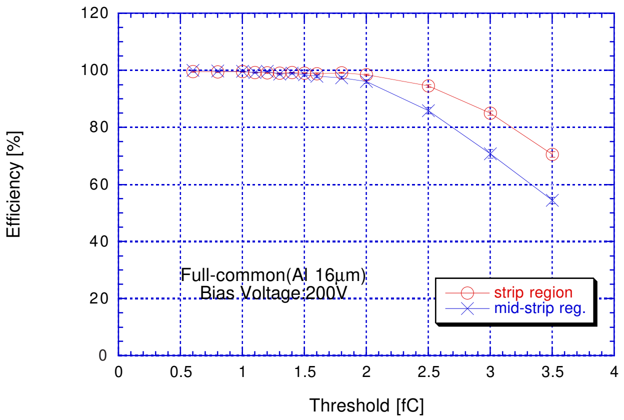

Fig.5 An example of the efficiency variation as a function of the threshold in strip (circle) and mid-strip (cross) regions.

An example of efficiency variations as a function of threshold is shown in Fig.5. The efficiency curve is an integrate of pulse height distribution above the threshold. The threshold of 50% efficiency is corresponding to the median pulse height of the deposit charge in one strip. In order to calibrate the gain of the electronics, the threshold of 90% efficiency was obtained by fitting an Error function, i.e., the integral of Gaussian function as an approximation of the integral of Landau distribution, to the efficiency variation. The gains of zones were normalized to the average threshold of the strip regions. Although the 90% efficiency threshold is not the median pulse height, it is a parameter expressing the collected charge.

D. Comparison of losses in the mid-strip regions

As seen in Fig.4 and Fig.5, there were losses of collected charges in the mid-strip regions. The losses were quantified with the threshold ratio of 90% efficiency of the mid-strip region over that of the strip region. The result is shown in Fig.6 for the end-tap module and at the bias voltage of 200 volts. Since we took the ratio, the gain variation was cancelled out even without the correction of the gains in the previous section. The statistical errors were as small as the size of the circles.

In general, there was about 20% less charge in the mid-strip region than in the strip region. The main source would be attributed to the sharing of charge into two strips. The charges observed in the strips are induced images of the drifting charges in the silicon. Since the efficiency in this analysis is that of a single strip, the observed charge is less when the image is doubled.

The ratios of Zone 2 (individual) and 1 (slit-common) are less than those of other zones. The ratios of Zones 3 to 6 are similar. The existence of the accumulation layer in Zone 2 and 1 would be the source of extra loss of the charge, and indicated that the continuous accumulation layer would be worse than the interrupted.

The bias voltage dependence of the ratios is shown in Fig.7 for Zones 1 to 4. Less charges were observed in Zone 1 and 2 at all voltages, although it was less clear at 120 volts. The other trend in the bias voltage dependence was that the loss became less as the bias voltage was decreased. This may indicate that more charge would be collected in the mid-strip region when the bias voltage is decreased.

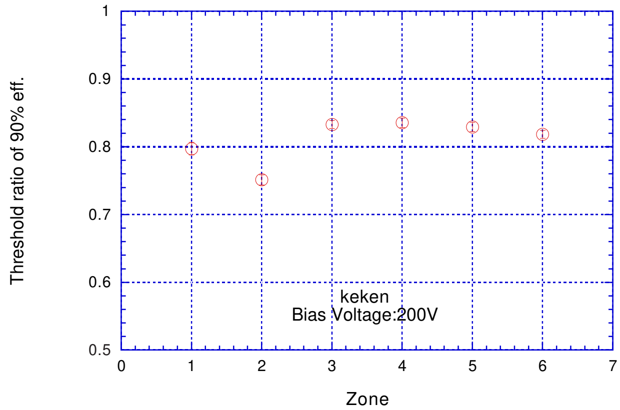

Fig.6 Threshold ratios of 90% efficiency of the mid-strip region over the strip region. The ratio corresponds to the ratio of collected charge in the region. A larger loss was observed in Zone 2, the individual p-stop structure.

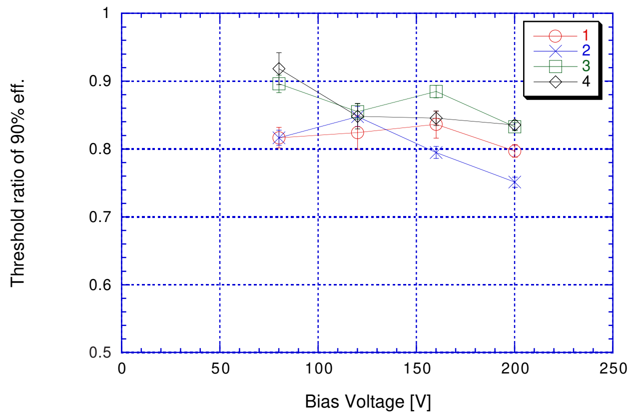

Fig.7 Bias voltage dependence of the threshold ratios of 90% efficiency. The charge collection was systematically lower in Zone 1 (slit-common) and 2 (individual p-stop).

The threshold ratios averaged over zones is plotted in Fig.8. The thresholds were divided by the threshold of the strip region of 200 volts. Both in the strip- and mid-strip regions, the collected charges increased as the bias voltage was raised, although the mid-strip region charge seemed to saturate over 160 volts. The data indicated that the charges collected were less at decreased bias voltages and the loss in the mid-strip region became less prominent.

E. Noise occupancy

Since the interstrip capacitance is a major contributor to the intrinsic noise, it is of interest how the capacitance relates with the noise in the modules. The noise was quantified as the occupancy in the strips. The occupancy was the fraction of the fired strips over the total number of strips accumulated in the triggered events, after eliminating the strips in the window twice-wider than that of the efficiency calculation around the triggered tracks.

In order to compare the trend in the bias voltage dependence, each threshold of 1 x 10^{-3} occupancy at 200 volts of zones was normalized to the average threshold of that occupancy. After scaling the gain with the 90% efficiency in the strip region and normalizing the 1 x 10^{-3} occupancy thresholds, the occupancy at 1 fC threshold is plotted in Fig.9 as a function of the bias voltage for Zones 1 to 4.

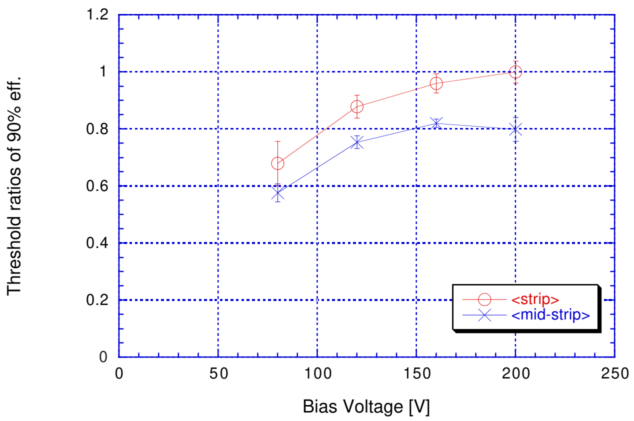

Fig.8 Threshold ratios of 90% efficiency averaged over zones in the strip and the mid-strip regions. The thresholds were divided by the threshold of the strip region at 200 volts.

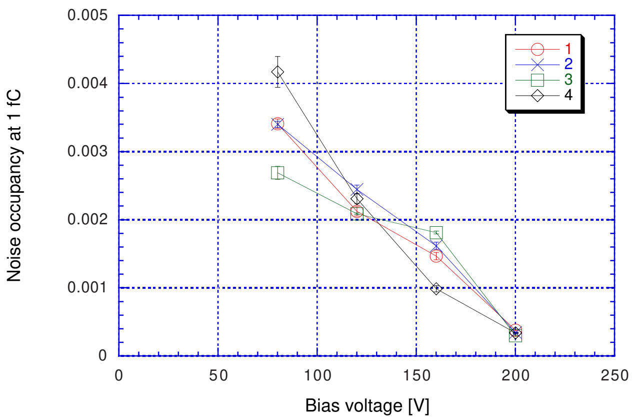

Fig.9 Bias voltage dependence of noise occupancy at 1 fC after re-scaling the gain and threshold

A gross feature of the bias voltage dependence is a near-linear dependence of the occupancy on the voltage. The occupancy increased about 8 times by decreasing the bias voltage from 200 to 80 volts. The interstrip capacitance was increased by about 1.5 pF and with a typical capacitance dependence of the intrinsic noise of electronics, the occupancy would increase about 4 times. Thus, the most of the increase of the noise occupancy was explained by the increase of the capacitance, but not all.

IV. Summary

Large area (63.6 mm x 64 mm) n-on-n silicon strip detectors have been fabricated, implementing various p-stop structures in the n-side for the n-strip isolation. A comparison was made for conventional full-common, individual, combined, and slit-common p-stop structures.

The detectors were characterized in laboratory and in beamtests. The inter-strip capacitance showed that the individual and the combined p-stop structure had the least capacitance. The beamtests showed that the individual p-stop structure collected less charge in the region between the strips than other p-stop structures. The loss of charge in the individual p-stop structure has been traced to the built-in accumulation layer surrounding the individual p-stop structure and covers the detector.

The increase of occupancy was not completely explained by the increase of capacitance, and supports the need for overdepletion found in the charge collection.

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