

Hybrid and Electrical and Mechanical Modules at KEK

(Updates in May 00 SCT week)

Y. Unno, et al.

KEK and ATLAS-Japan SCT group

- **Design documents**
- **A few reminders of the thermo-mechanical measurements**
- **Electrical modules**
- **Summary**

Design documents

- **“Design and fabrication of the ABCD Kapton Hybrid”, Sep. 30, 1998,**
 - **Text and figures are needed to be revised, however,**
 - **latest updates of figures and drawings are available from the web page**
- **A draft of the “stuffing and assembling into module” is also available**
 - **Simple and skeleton, but exits**
 - **Improvement is foreseen**

Design and Fabrication of the ABCD Kapton Hybrid

September 30, 1998

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Abstract

A hybrid plane with polyimide (Kapton) multilayers is designed and fabricated in order to demonstrate its feasibility for the application to the ATLAS barrel SCT modules using the ABCD chips.

1. Motivation

We propose to use a multi-layered flexible printed circuit technology based on Polyimide (Kapton) base material for constructing the hybrid of the ATLAS microstrip silicon detector. We think there are several advantages in using this particular technology:

1. The technology has been widely used in commercial products such as printers, note-type computers, video/photographic-cameras, portable music players etc.
2. The hybrid can be easily folded and so all-in-one hybrid structure (see Figure 1) is possible including everything from connector, connector extension, top-hybrid, interconnection, and bottom hybrid. In comparison with separate-hybrid structure, this all-in-one structure significantly reduces number of parts needed and simplifies the labor/time-consuming connection/assembly works. It helps also in reducing troubles in electrical connections.
3. Radiation length of the material can be smaller.
4. Production cost could be much reduced.

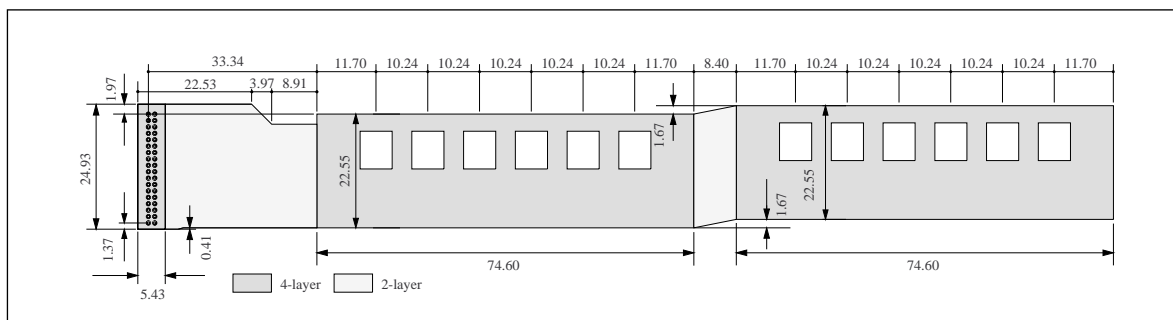


Figure 1. All-in-one structure of the ATLAS barrel SCT hybrid.

2. Manufacturer

We have made a contact with a manufacturer, Mektec Corporation which has branches at Tokyo, San Jose, Singapore, Weinheim. This company has a dominant marketing share in Japan in the field of flexible printed circuit.

Hybrid stuffing and assembling into module

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I. INTRODUCTION

The ABCD kapton hybrid is distributed with

- Carbon-carbon bridges glued
- Glass pitch-adaptor glued.

The stuffing and assembling steps of the hybrid are

1. solder passive components: resistors, capacitors, connector
2. glue ASICs with silver-loaded conductive epoxy
3. wire-bond ASICs and AGND-DGND pads
4. glue the hybrid on the sensor-baseboard assembly
5. wire-bond channels and HV bias connections

The web page, http://atlas.kek.jp/~unno/si_hybrid.html shows,

Kapton hybrid designs:

- Component loading diagram (pdf) (1 page)
- Circuit diagram (pdf) (2 pages, shows wire-bond locations)
- Glass pitch adaptor (pdf) (1 page)

The component loading shows where components are physically stuffed. The circuit diagram shows details of electrical connections and wire-bondings. The glass pitch adaptor drawing shows the detail of the wire-bondings around the pitch adaptor. These drawings are appended in Figure 2, Figure 3, Figure 4, and Figure 5. The pin assignment of the hybrid connector is listed in Table 1, and the components in Table 2. Details of the hybrid design can be obtained from the web page, <http://ccint1.kek.jp/People/kondo/sct/>.

II. MOD0 FABRICATION

In the Mod0 fabrication, we did the following.

A. ASIC gluing:

1. Silver-loaded conductive epoxy. We think the conductive epoxy is important although the backside of the chips is not metalized. Glue full area. We use a room-temperature curing one and do post-curing at 50 °C for 2 hrs. The viscosity is relatively low. The epoxy is made by a domestic company.

B. wire-bondings

1. GND (D-, A-, ring-a, det-,...), Vcc, Vdd pads == at least 2 wires per pad if possible,
2. AGND-DGND stitching pads == as many wires as possible, mod0 = 5 wires/pad,
3. Detector bias connections == at least 2 wires per pad. There are four corners of the hybrid which can be used to connect to the detector strip and backplane bias. The strip bias con-

nection is done at four corners. The backplane bias connection is done only on the top side two corners, since the baseboard has only those contacts.

C. Other technical recommendations

1. dry up the hybrid in a low humidity environment (<50% RH) before soldering
2. mask the wire-bonding pads when soldering in order not to contaminate the bonding surface
3. do not burn out the hybrid with a soldering iron. The spec is <10 sec at 260 deg.C. The higher the temperature, the shorter the time (than 10 sec).
4. when wire-bonding, keep in mind that the width of the pads on hybrid, which are mating with the output pads of the chip, is narrow
5. recommend to confirm the performance of the chips before wire-bonding between the chip and the pitch adaptor
6. keep the masking tape on the pitch adaptor until the wire-bondings between the chips and the pitch adaptor will occur.

III. ASIC REPLACEMENT

ASIC replacement has been tested. A jig of

- 8 mm x 8 mm x 12 mm Cu block
- trench of 6.5 mm width and 0.3 mm depth
- the Cu block attached to the tip of a soldering iron
- vacuum line for picking up the chip

was prepared. A photo of the jig is shown in Figure 1.

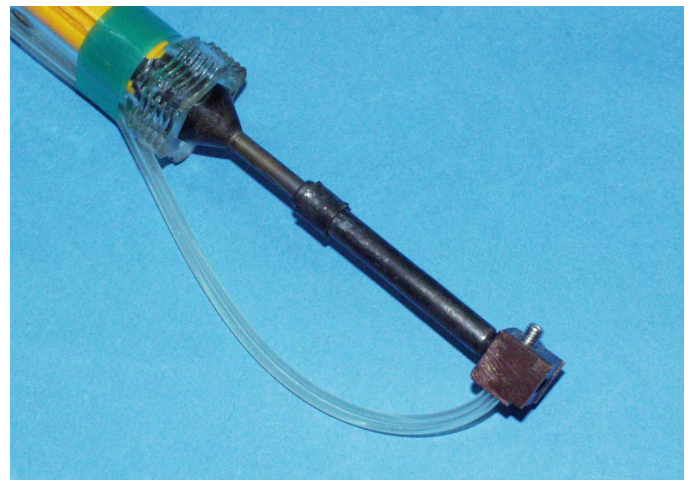


Figure 1: An IC heating and picking-up jig

Thermo-mechanical measurements

- **KEK's independent measurements**

- In addition to the common effort at RAL
- A few reminders of the results

- **Distortion of the hybrid in the module**

- Before and After (10 thermal cycles)
- After (20 thermal cycles) was also measured
- Temperature dependence: $\sim 0.5 \mu\text{m}/^\circ\text{C}$ sagitta
- E.g., $20 \mu\text{m}$ from 20°C to -20°C

- **Thermal fatigue in the module**

- 7.5 W power on-off in cold (-12°C cooling water)
- Before and After 100 cycles
- No disintegration nor crack
- No change in the temperature dependence of distortion of module

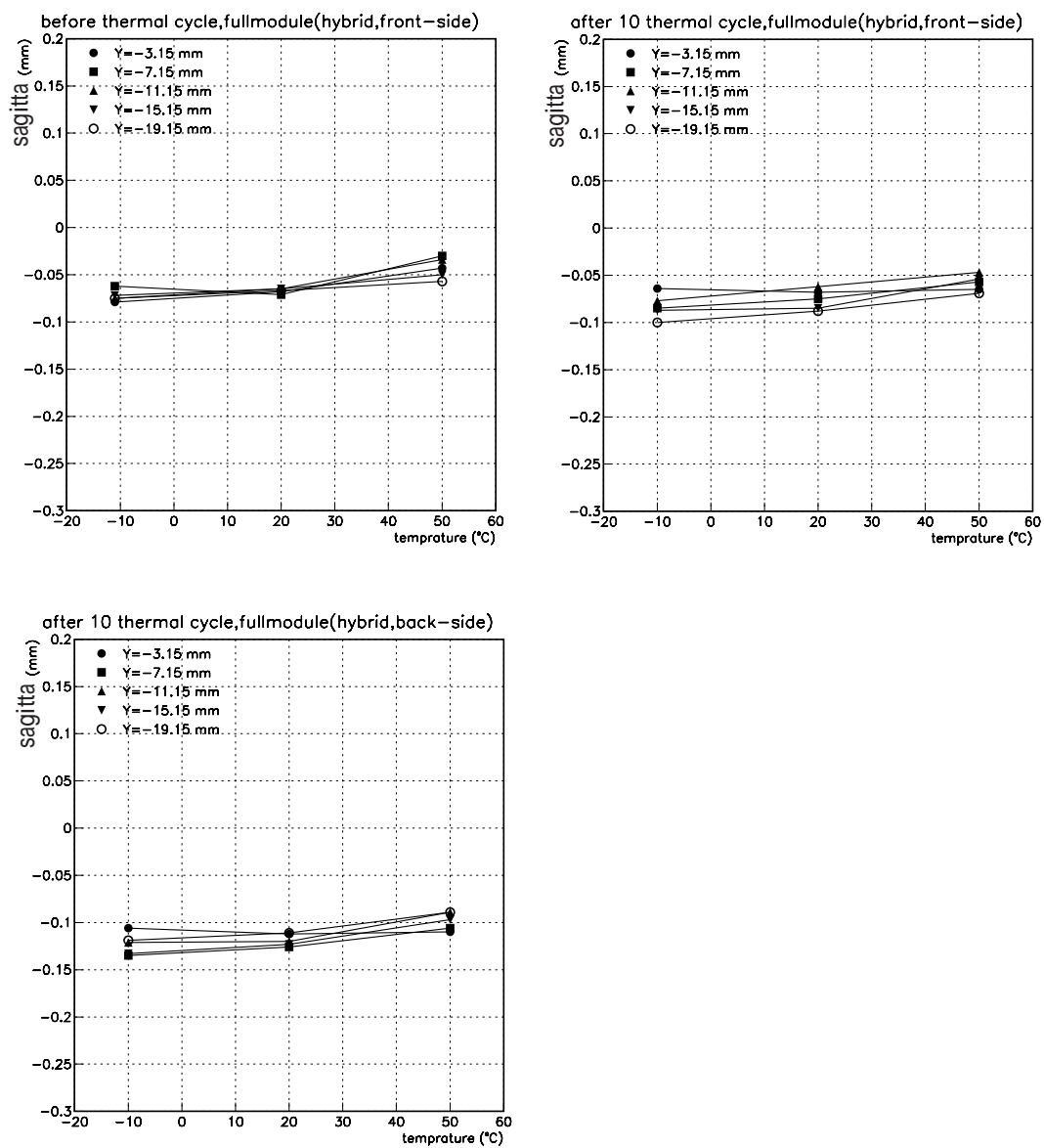


図 6.12: フルモジュールにしたときのカプトンハイブリッド基板の表側の熱サイクル前後での温度による変形率

Electrical modules

- **Barrel module program**
 - Proposed to the IB by Mike Tyndel in the Feb SCT week
 - Supported by the majority of the barrel clusters by e-mail correspondence
- **“Mod0” to experts in other clusters**
 - Sent to the US cluster, Santa Cruz
 - Set in the beamtest in May at CERN
- **Identical modules in UK, US, and Nordic clusters**
 - Hybrids were sent to the clusters in March
 - Reports from the clusters in this week (?)
- **Investigation modules at KEK**
 - E-mail correspondences among interested peoples
 - One module was built and tested by the SCT week

Barrel Module Program

- The barrel module program is in a difficult situation because of the limited number of ASICs (& other components available).
- There are a number of open technical issues and options which have not yet come to a mature conclusion. These concern the choice of hybrid technology, the electrical design of the module and assembly & rework issues.
- A special meeting was held of 1 representative/cluster to make a proposal on how best to proceed. There was a divergence of views within this group. Given the limited number of ASICs available & taking into account schedule, financial and political considerations, the following is proposed :
 - 1. Kapton hybrids are adopted immediately as the baseline technology.
 - 2. The first KEK Kapton module (Mod-0) is made available as soon as possible to experts within the other clusters to make measurements.
 - 3. Three more modules, identical to (Mod-0) are manufactured and tested in the UK, USA and Nordic clusters. These four modules will be sent to the system test for measurement
 - 4. The stability margin will be investigated by building 3 (Mod-0) variants at KEK using existing variants of the hybrid. The details of what is to be built is to be agreed by the ASIC engineers. Experts from all clusters will participate in the measurement and understanding of these variants
 - 5. In view of the potential benefits to be gained from the thin film hybrid, 2 modules are to be built.
 - 6. A detailed review of all measurements will be held in the May SCT week
 - 7. Finally, it is anticipated that a final prototype hybrid will need to be designed and manufactured and 4 modules built by end 2000.

Mod0

- **To remind you...**

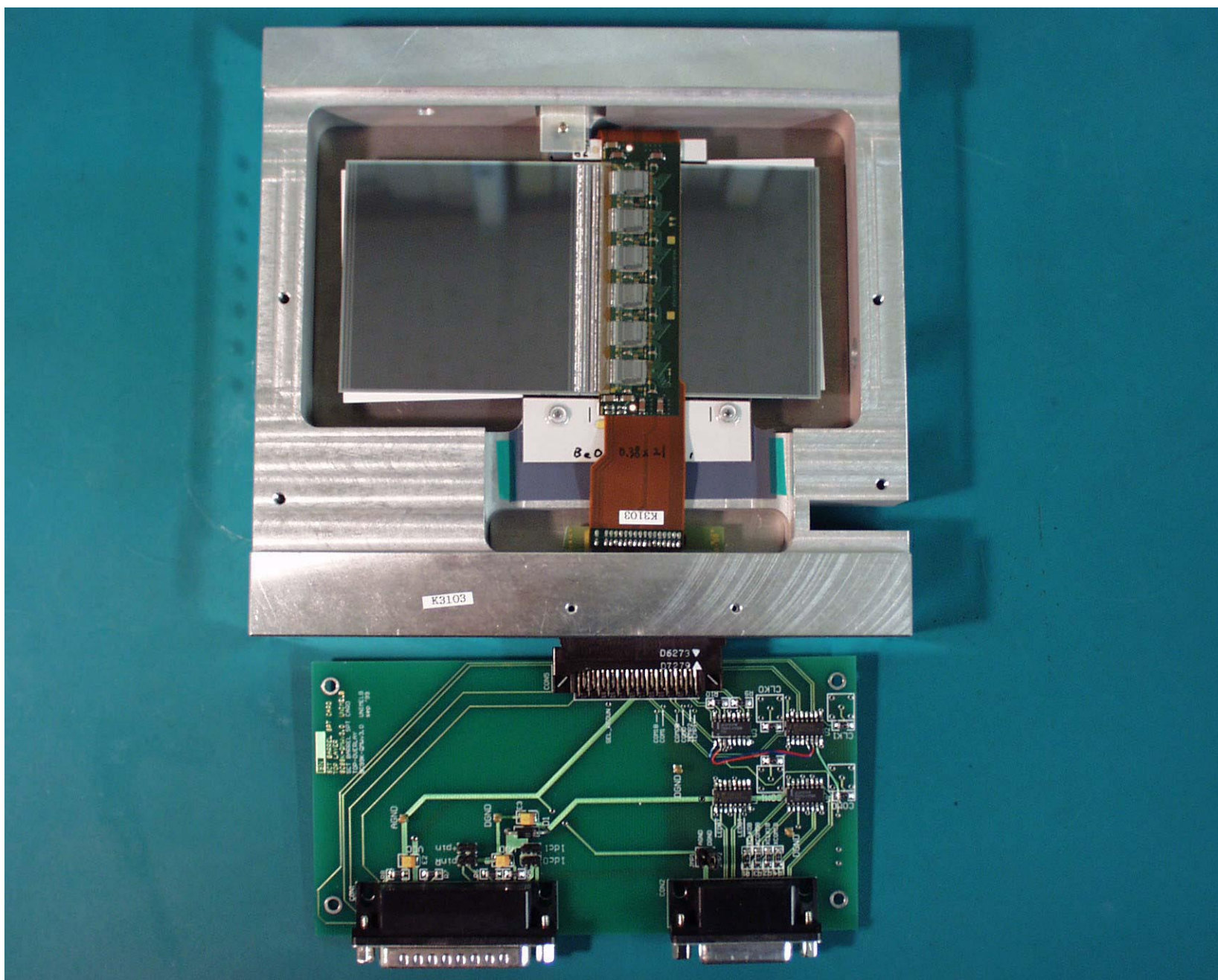
- This is an example of “stable” module
- Stable even after trimming: Trimmed at 2 fC = 200 mV

- **S-curves**

- Edge=off, Comp=X1X
- “Summed” displays
- Individual all channels per chip and cal lines
- All “clean”

- **Trim characteristics**

- Rather good (compared with the “End of March” distribution): 32 untrimmable channels
- Mod0 chip: wafer 30423
- Uniformity at trim threshold: 2.67 (front 6 chips) and 2.76 mV (back 6 chips), i.e., <3 mV

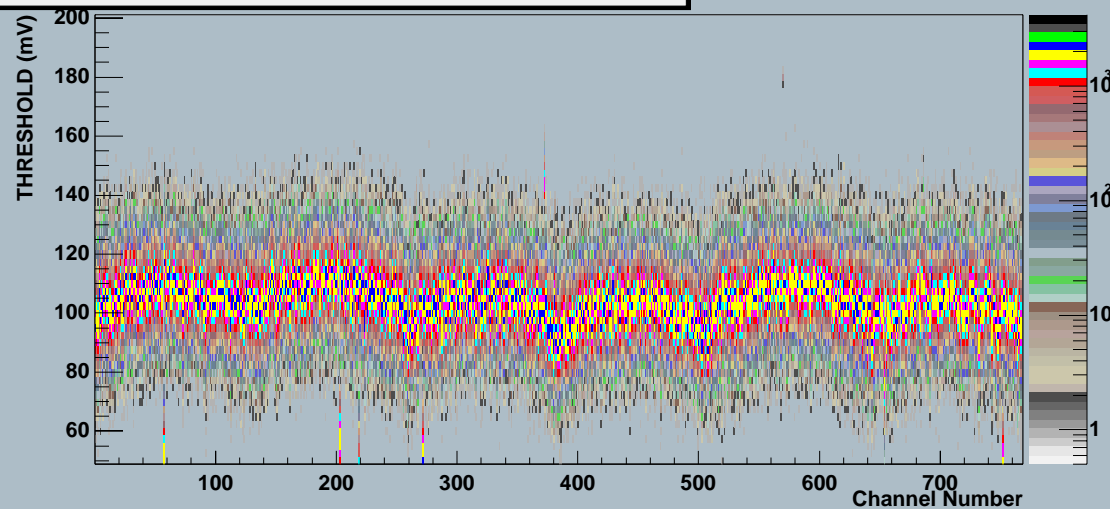


ATLAS SCT Scan Comparison - log scale

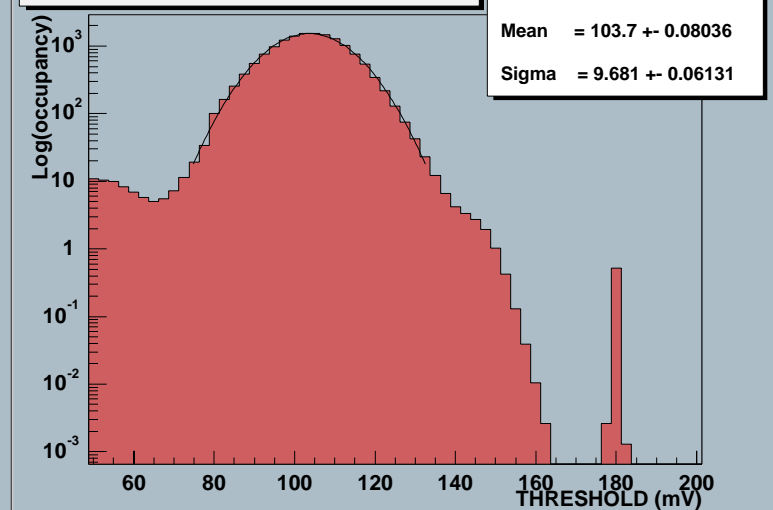
Run 242 Scan 2 Module 0 Stream 0 (Projection of ch 0 to ch 767) vs

Run 242 Scan 2 Module 0 Stream 1 (Projection of ch 0 to ch 767)

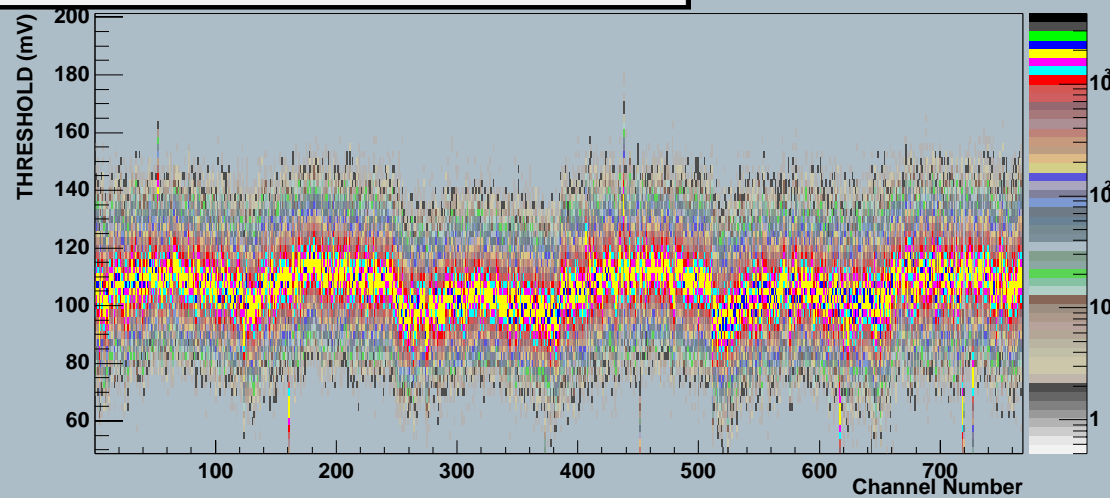
Module 0 Stream 0 THRESHOLD (mV) Scan



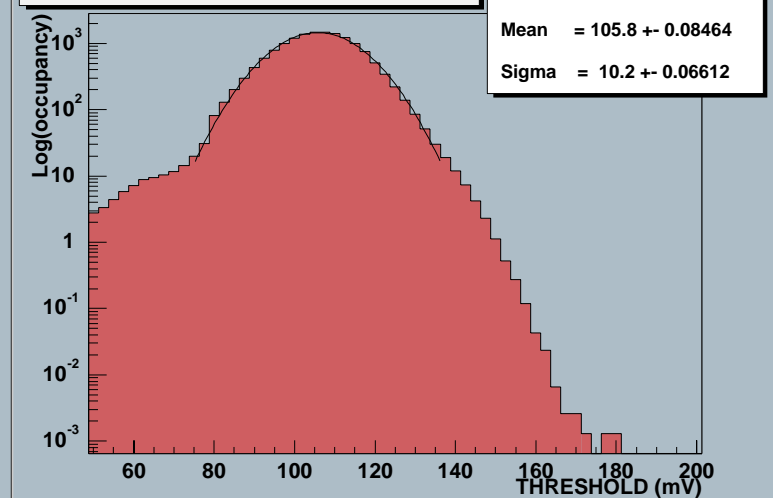
Module 0 Stream 0 THRESHOLD (mV) Scan



Module 0 Stream 1 THRESHOLD (mV) Scan



Module 0 Stream 1 THRESHOLD (mV) Scan

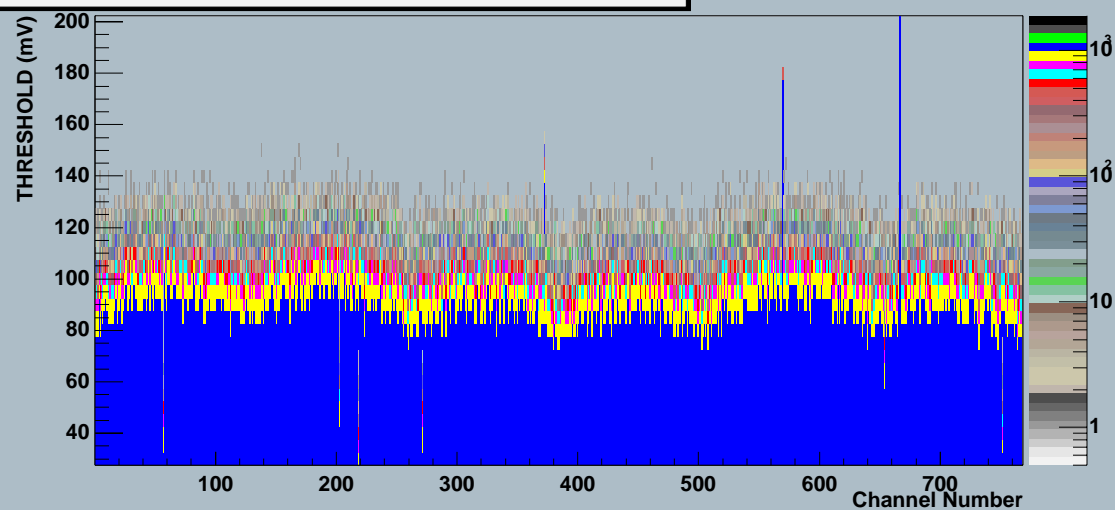


ATLAS SCT Scan Comparison - log scale

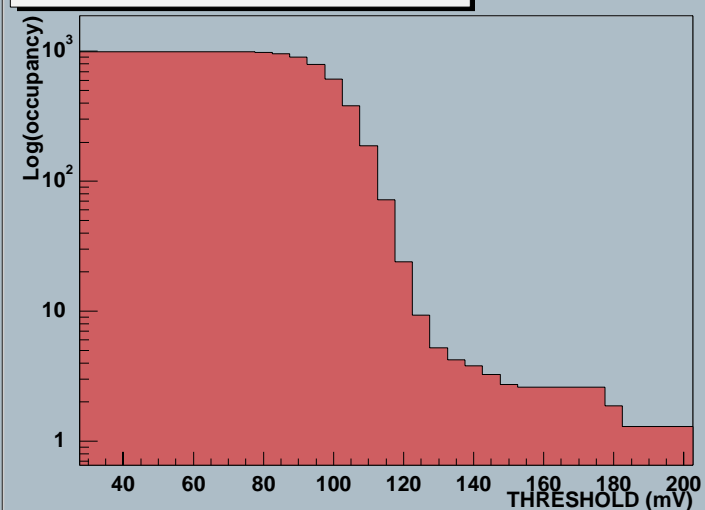
Run 238 Scan 1 Module 0 Stream 0 (Projection of ch 0 to ch 767) vs

Run 238 Scan 1 Module 0 Stream 1 (Projection of ch 0 to ch 767)

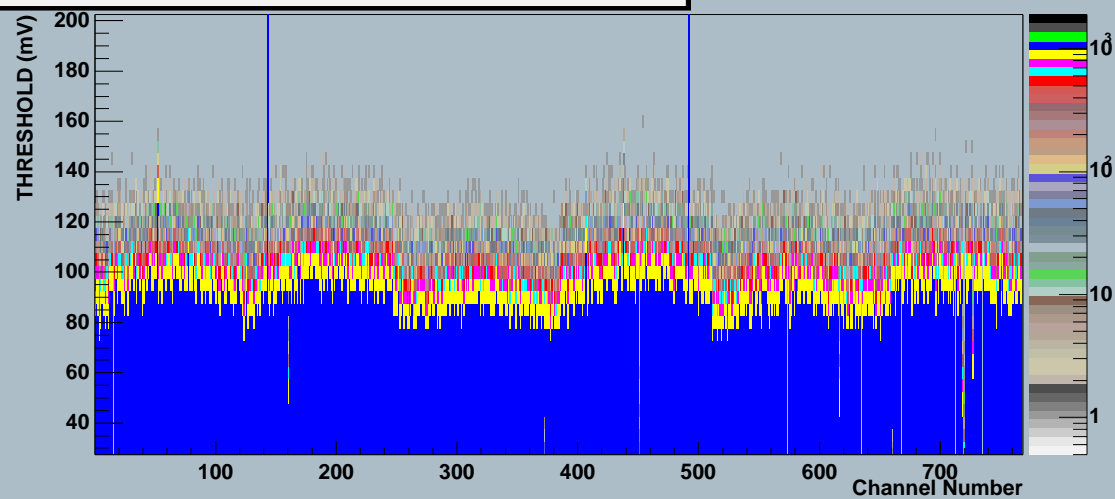
Module 0 Stream 0 THRESHOLD (mV) Scan



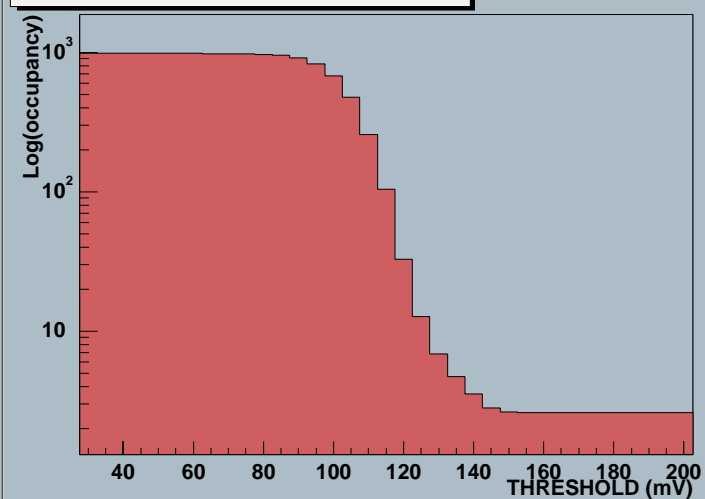
Module 0 Stream 0 THRESHOLD (mV) Scan



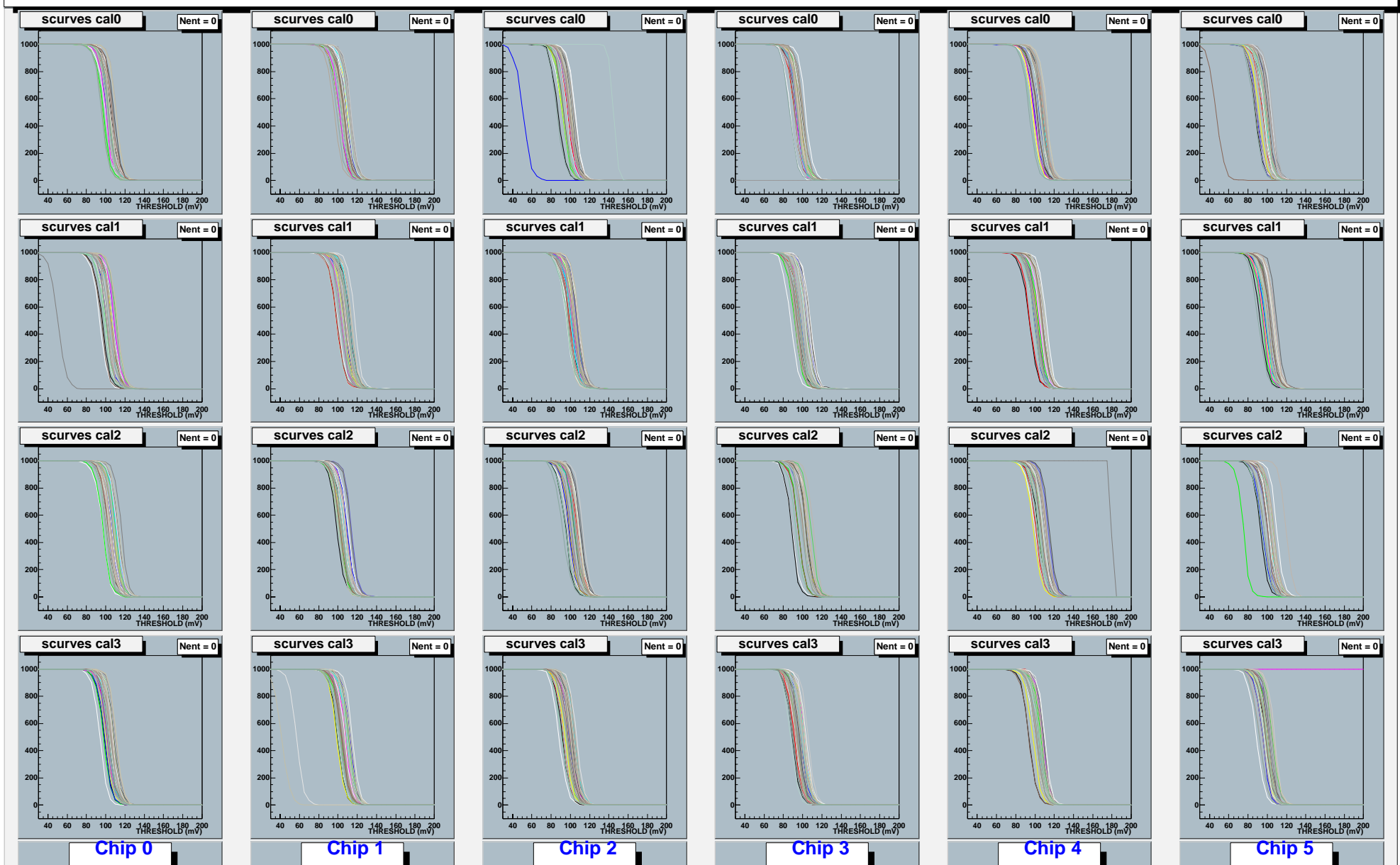
Module 0 Stream 1 THRESHOLD (mV) Scan



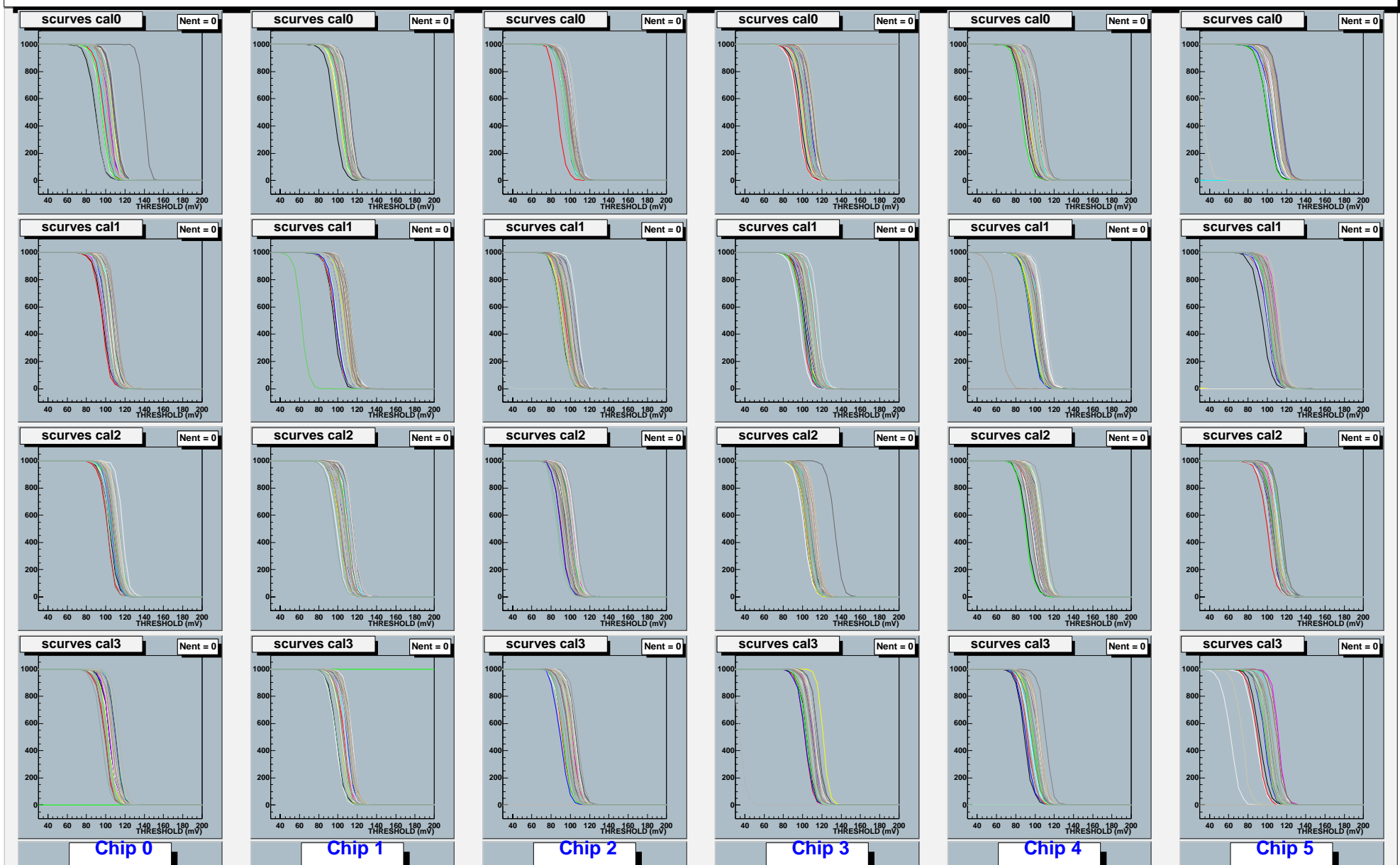
Module 0 Stream 1 THRESHOLD (mV) Scan



Module 0 Link 0 Run 238 Scan 1 - THRESHOLD (mV) from 30.00mV to 200.00mV in 5.00mV steps, total 35 points



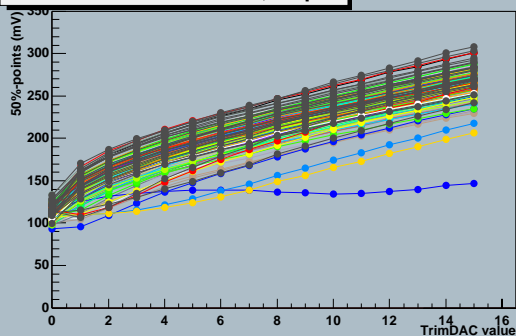
Module 0 Link 1 Run 238 Scan 1 - THRESHOLD (mV) from 30.00mV to 200.00mV in 5.00mV steps, total 35 points



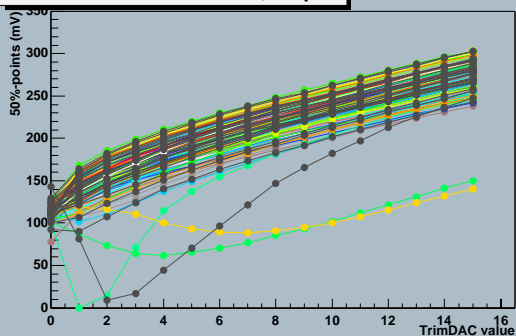
ATLAS SCT Module Test
 ATLAS SCT Module Test
 Run 236 Trim Scans Module 0 Link 0

Target value to be 200 mV
 This gives 1504 trimmable channels

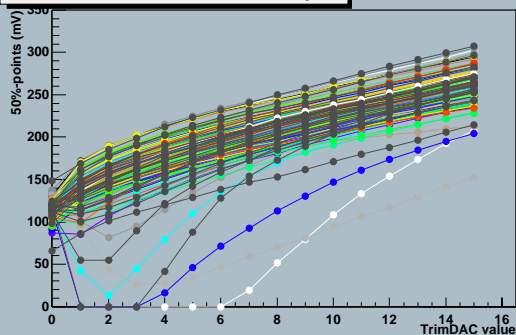
TrimDAC characteristics, chip 0



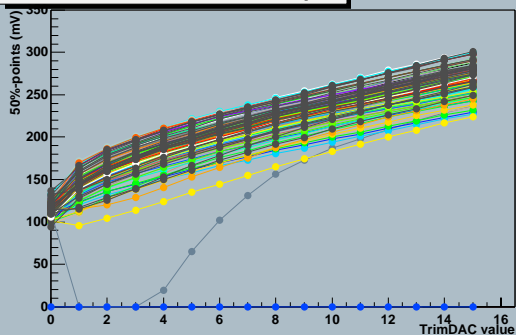
TrimDAC characteristics, chip 1



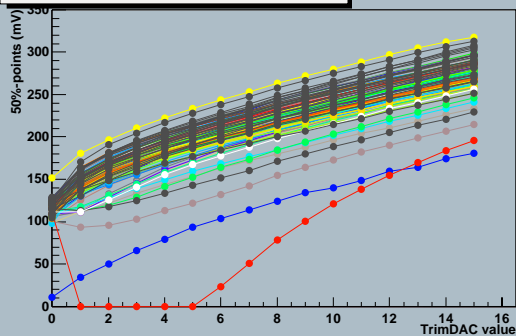
TrimDAC characteristics, chip 2



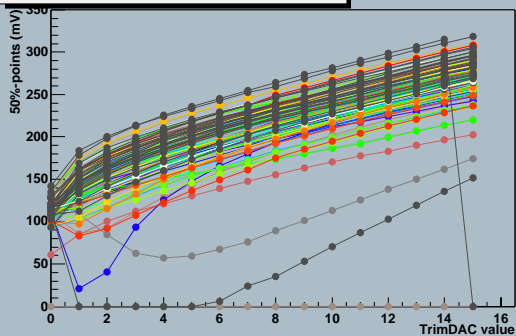
TrimDAC characteristics, chip 3



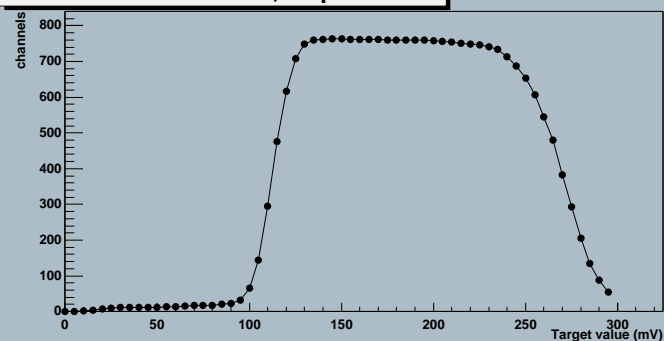
TrimDAC characteristics, chip 4



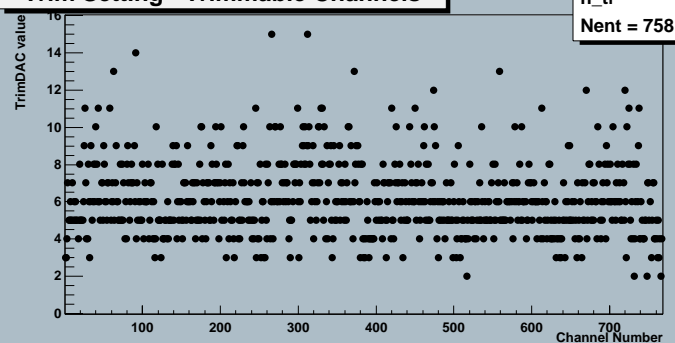
TrimDAC characteristics, chip 5



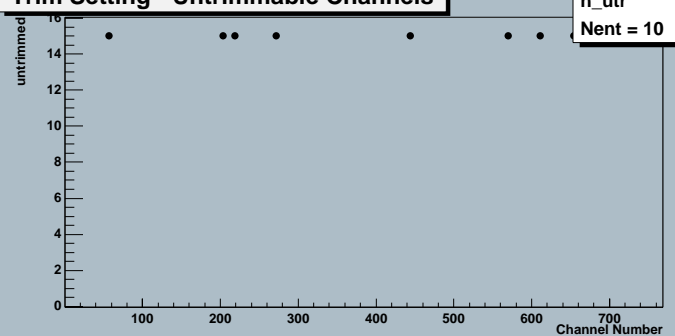
Trimmable channels, chip 0 to 5



Trim Setting - Trimmable Channels

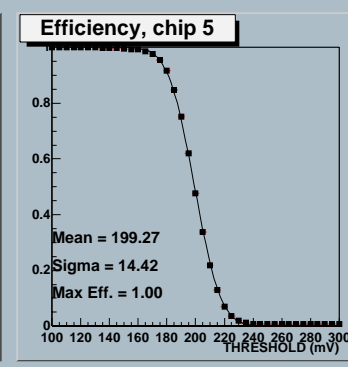
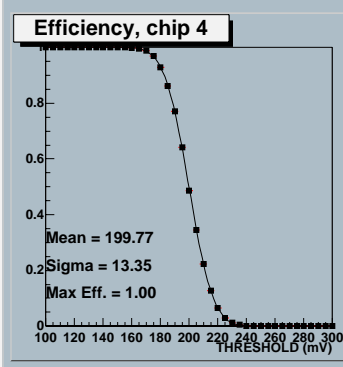
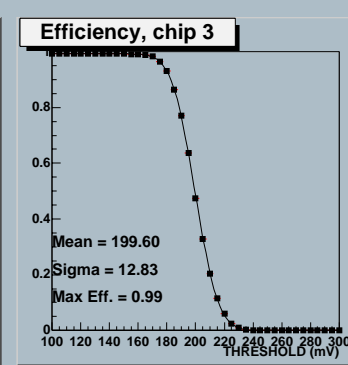
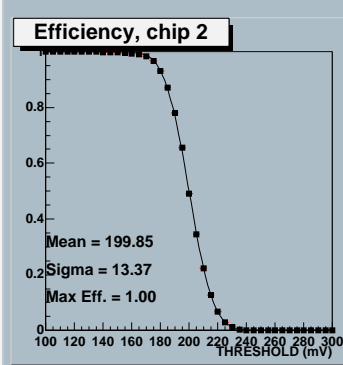
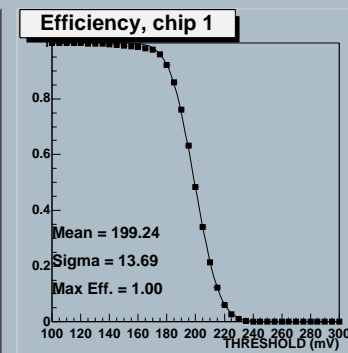
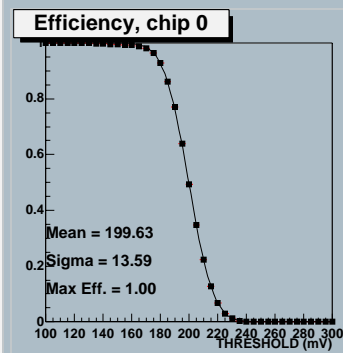
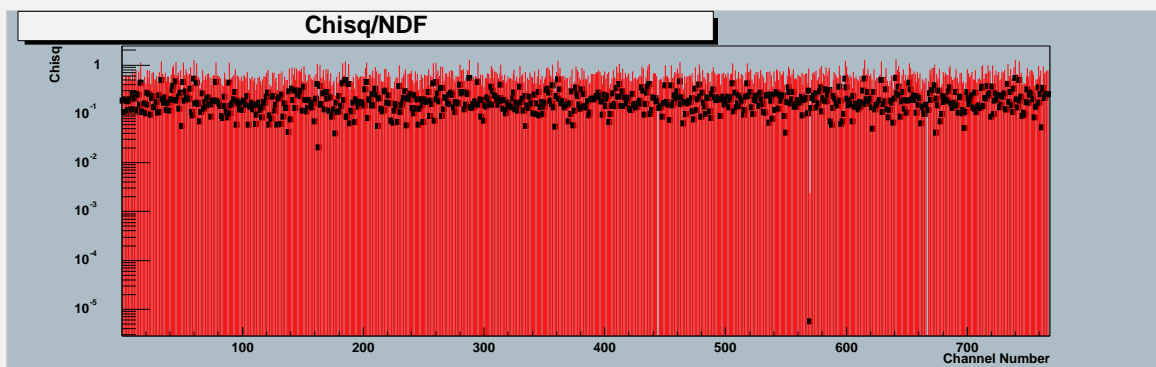
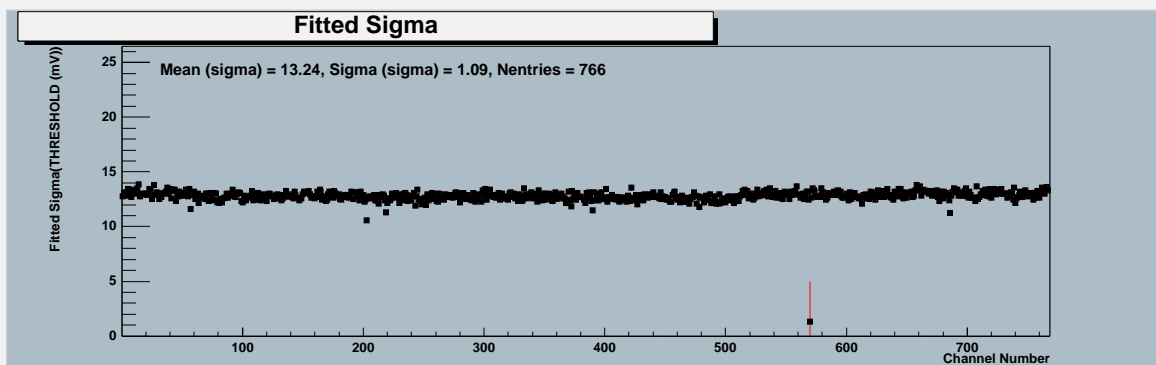
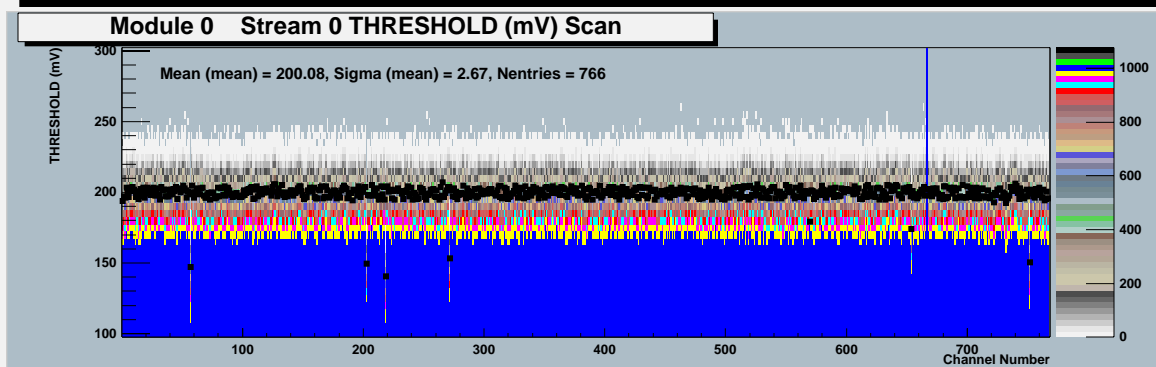


Trim Setting - Untrimmable Channels



ATLAS SCT Module Test

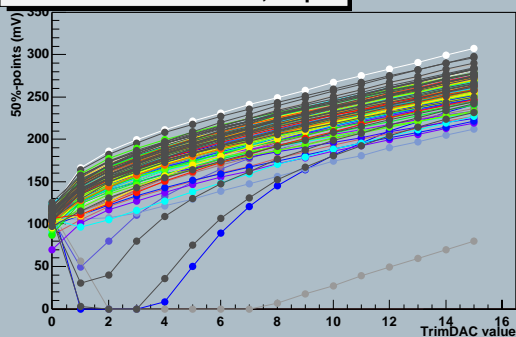
Run 238 Scan 4 Module 0 Stream 0 Scan type: THRESHOLD (mV)



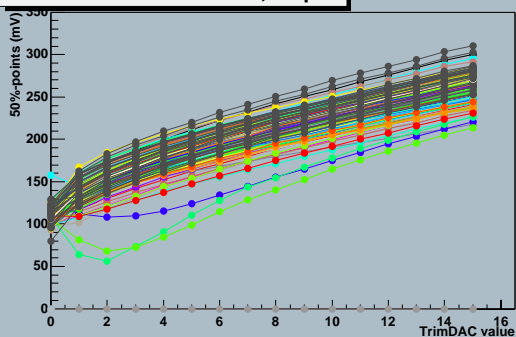
ATLAS SCT Module Test
 ATLAS SCT Module Test
 Run 236 Trim Scans Module 0 Link 1

Target value to be 200 mV
 This gives 1504 trimmable channels

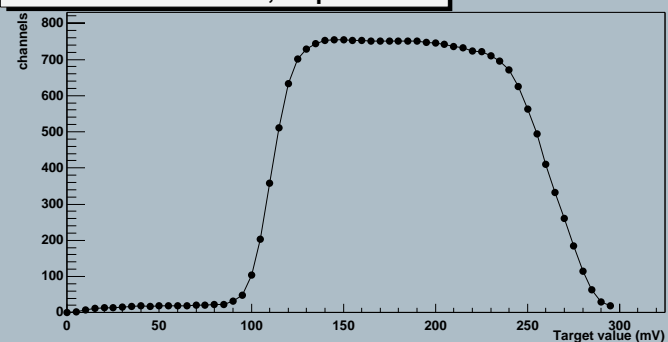
TrimDAC characteristics, chip 6



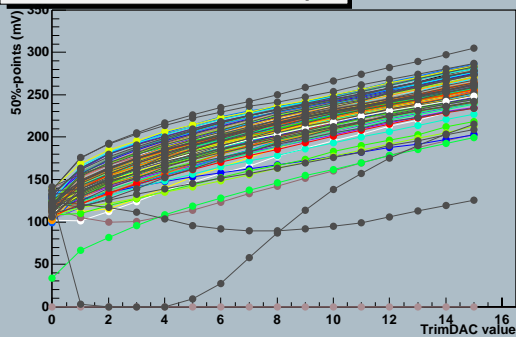
TrimDAC characteristics, chip 7



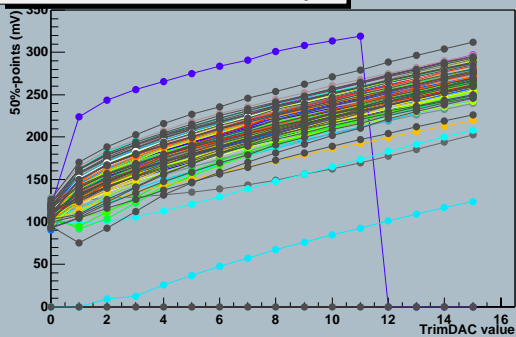
Trimmable channels, chip 6 to 11



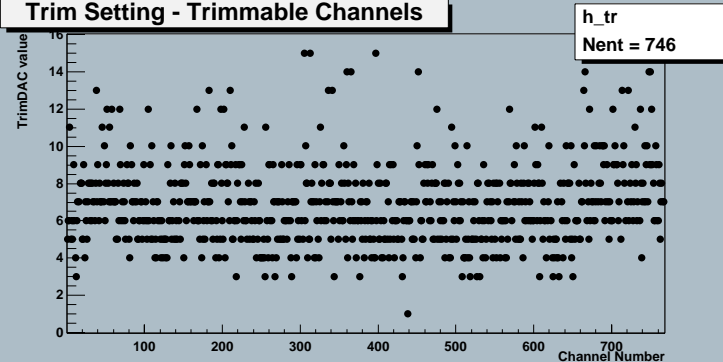
TrimDAC characteristics, chip 8



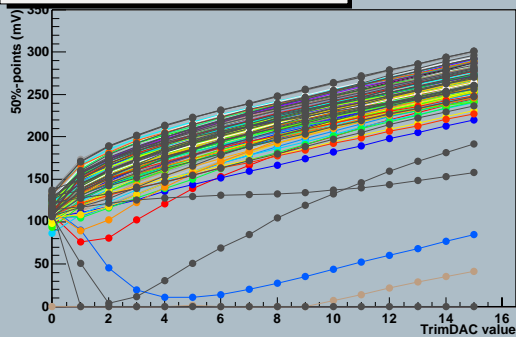
TrimDAC characteristics, chip 9



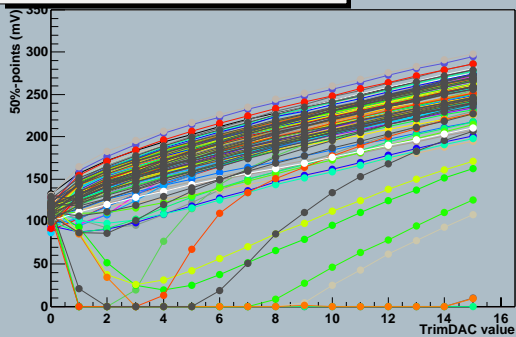
Trim Setting - Trimmable Channels



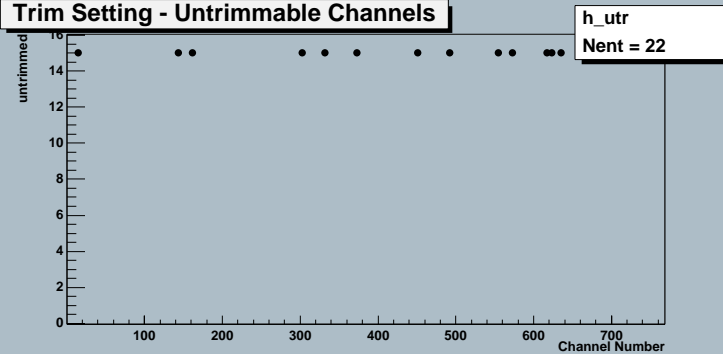
TrimDAC characteristics, chip 10



TrimDAC characteristics, chip 11



Trim Setting - Untrimmable Channels



Module name	k3104mod	k3103		
Strip sensors:	Type	Thickness [um]	Vendor	
Top	ATLAS98 narrow-m	285 um	Hamamatsu	
Bottom	ATLAS98 wide-poly	285 um	Hamamatsu	
Baseboard id.	???			
ASICs:	Type	Lot	Wafers	
M0-E13	ABCD2T	30423	3	
Hybrid:	Substrate	Substrate Surface finish		
Kapton ABCD v3	Carbon-carbon	metalized		
Capacitors:	C [nF]	Type	Reso freq [MHz]	Vendor
Vcc, Vdd	100	GRM39-X7R-104-K-25	~26	Murata
Common Vcc, Vdd	330	GRM42-6-X7R-334-K-25	~15	Murata
HV decoupling	10	GHM1530-B-103-K-630	~70	Murata
HV connections:	No. locations	No. bonds/location		
Strip	4	2		
Backplane	2	2		
AGND-DGND connections:	14	5		
Bias [V]	Leak current [uA]:	Env. temp [deg.C]	Condition	
100	~0.8?	18?	fan circulation	
ASIC currents [A]:	V(sense) [V]	Vth>offset+200 mV	Vth=offset	
Vcc	3.5	0.92		
Vdd	4	0.48	~0.8	
Trimming:	Chage [fC]	Threshold [mV]	Trimmable ch	Untrimmable ch
	2	200	1504	32
Threshold uniformity [mV]	Edge=off		Edge=on	
at trim threshold	link0	link1	link0	link1
	2.67	2.76		
Offset threshold [mV]:	Edge=off	(2~8fC, 2nd-poly)	Edge=on	(2~8fC, 2nd-poly)
Chips	Vt50	Intercept	Peak	Intercept
link0 average	102.4	81.8	103.7	
link1 average	104.8	83.2	105.8	
Gain (@2fC) [mV/fC]:	Edge=off		Edge=on	
Chips	Linear(0,2,3fC)	2nd poly(2~8fC)	Linear(0,2,3fC)	2nd poly(2~8fC)
link0 average	50.4	55.8	XXX	
link1 average	49.3	55	XXX	
Noise (@2fC) [e]	Edge=off		Edge=on	
Chips	Linear(0,2,3fC)	2nd poly(2~8fC)	Linear(0,2,3fC)	2nd poly(2~8fC)
link0 average	1590	1437	XXX	
link1 average	1637	1465	XXX	
Instability thresholds:	Edge=off		Edge=on	
Chips	Lower [mV]	Upper [mV]	Lower [mV]	Upper [mV]
link0	none	none	none	none
link1	none	none	none	none