

ABCD chips+Kapton hybrid testing

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Abstract

The n-ABCD chips were tested on the ABCD Kapton hybrids prototyped for the SCT Barrel module. Out of several hybrids assembled, the results from one 6 chips and one 12 chips hybrids are reported here.

Assembled hybrids and test setup

- **As of Sep. 98, 4 hybrids are assembled,**
 - **Khybrid1: one “untested” n-ABCD chip, reported in the June SCT week, verifying the digital function of the ABCD Kapton hybrid**
 - **Khybrid2: 6 chips hybrid with “tested” n-ABCD chips. Chips were mounted and checked one-by-one, investigating effects of adding more chips. The chips were those with “Quality factor” about 2. Assembled into -- “Single-detector Module”**
 - **Khybrid3: 12 chips hybrid with “tested” n-ABCD chips, the top 6 chips were “Q-factor” about 2 and the bottom 6 chips “Q-factor” 1. Assembled into -- “Full Electrical Module”**
 - **Khybrid4: Recycled from the Khybrid1, removing the chip and stuffing 2 chips with “Q-factor” 1 on the top side, to cross-check the data quality in the top and the bottom side**
- **In addition to these assembled and test at KEK, there are several ABCD Kapton hybrids assembled and tested in Melbourne for the forward module**
- **The report is for the Khybrid2 and Khybrid3**

Data acquisition setup

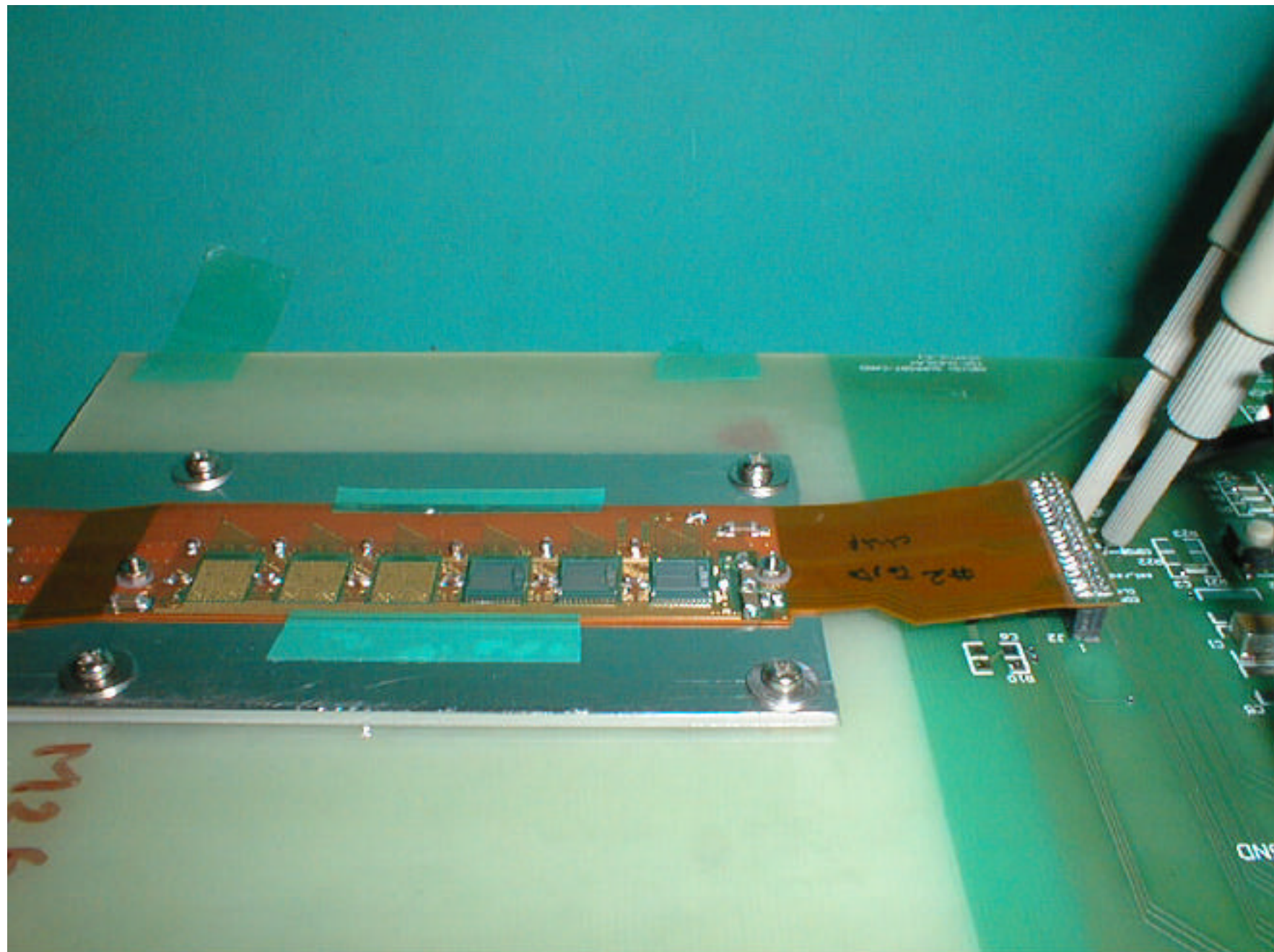
- **The setup used was the UCI DSP based hardwares,**
 - **Melbourne SC97**
for interfacing the hybrid and the cable to the backend electronics
 - **Cambridge BC96**
for supplying powers to the hybrid, merging the data cable from SLL and the bias power supply to the detector
 - **UCI SLL (Strip Low Level) card**
for the communication between the SC97 and the DSP
 - **UCI VME-DSP module**
for the data processing and communication with VME
 - **266 MHz Pentium II PC with Windows NT4.0 OS**
- **PC-DAQ (abcdaq by P.W. Phillips) software for the data acquisition**

Troubles and Solutions

- In order to get the data to be collected, there were problems and solutions with the helps from many collaborators, especially, from P.W. Phillips (RAL), G.F. Moorhead(Melbourne), D. Macina(Geneve), S. Pier, T. Fahland(UCI), W. Dabrowski (Crakow) et al.
- ABCD chip bugs:
 - Clock phase reversal -- This was solved by using a short jumper cable on the JP? of SLL but cable leads inverted
 - Delay value -- only works for odd DAC values
 - End-chip datain/datainB pulled to DGND/Vdd
- ABC GAL's:
 - SLL requires a new GAL (Gare Array Logic) programmed for ABC protocol (and timing?) called "ABC GAL"
- SLL link jumpers:
 - This is not a real bug but the abcdaq is not programmed yet to handle 2 (or 4) links automatically which SLL can handle
 - The abcdaq works either one link with one SLL link jumper or two links with two SLL link jumpers. The jumpers were put and removed by hand for the 6 chips, one link, and the 12 chips, two links, hybrids
- For others, consult with the web pages...

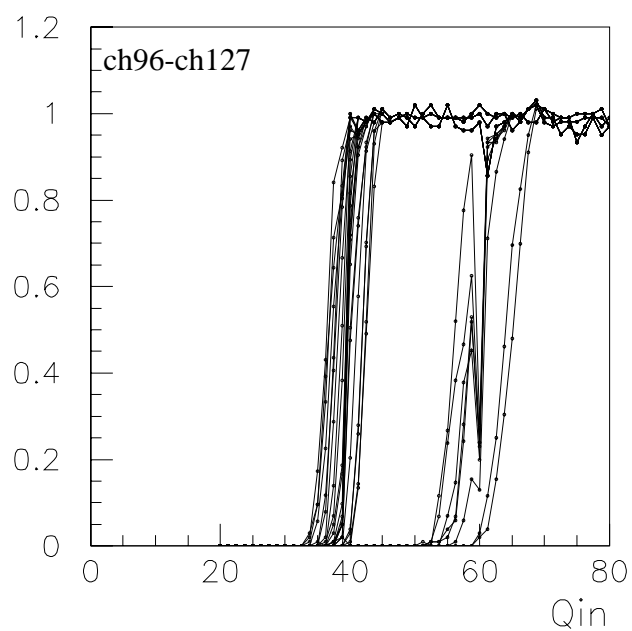
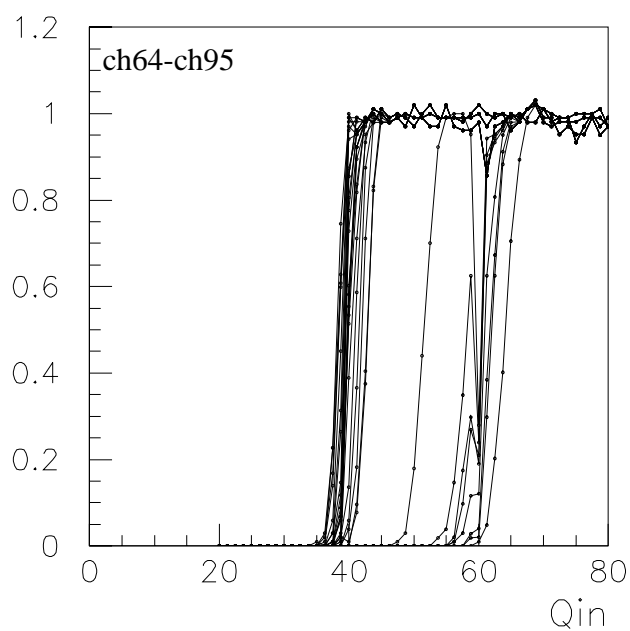
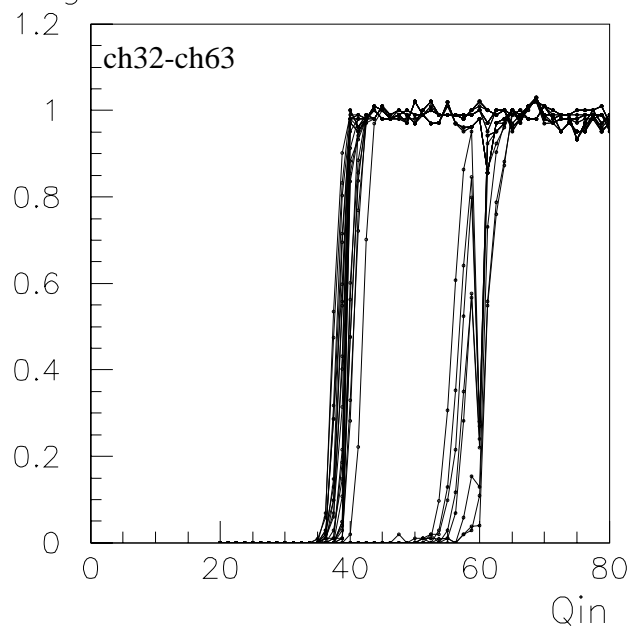
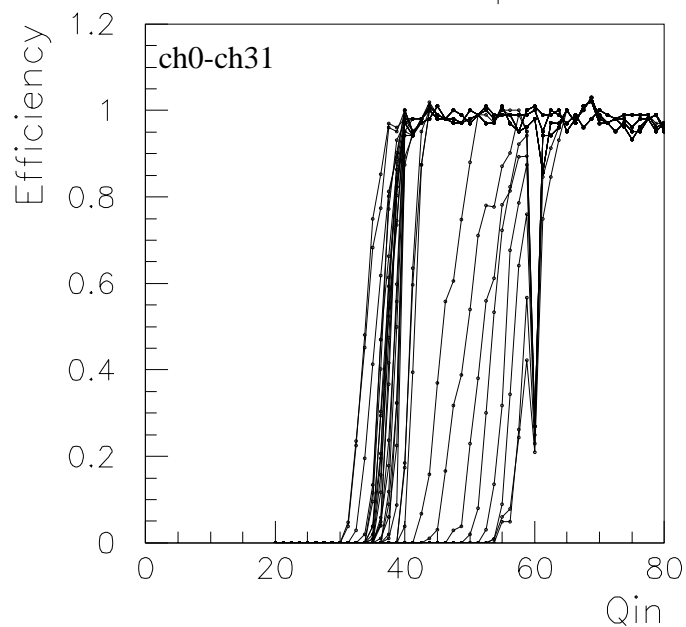
6 Chips Hybrid

- **Khybrid2: Good quality (2) n-ABCD chips**
- **Step-by-step mounting and testing**
- **Charge injection scan (with the internal DAC)**
- **Amplifier response is non-linear, but for the current analysis we took a linear function**
- **FE bias current:**
 - **Vcc = 3.5 V, Vdd=4.2 V -- These values were varied, say $\pm 20\%$, but did not change performance in general**
 - **Two “good quality” regimes, around 73.6 μA (Lo-regime) and 211.6 μA (Hi-regime)**
 - **Hi-regime had more gain spread and larger noise**
 - **Mostly operated at Lo-regime, 73.6 μA (or 82.8 μA)**
 - **Data taking with LEVEL mode (12 chips hybrid was EDGE mode)**



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qinb74t300edge.dat- zz



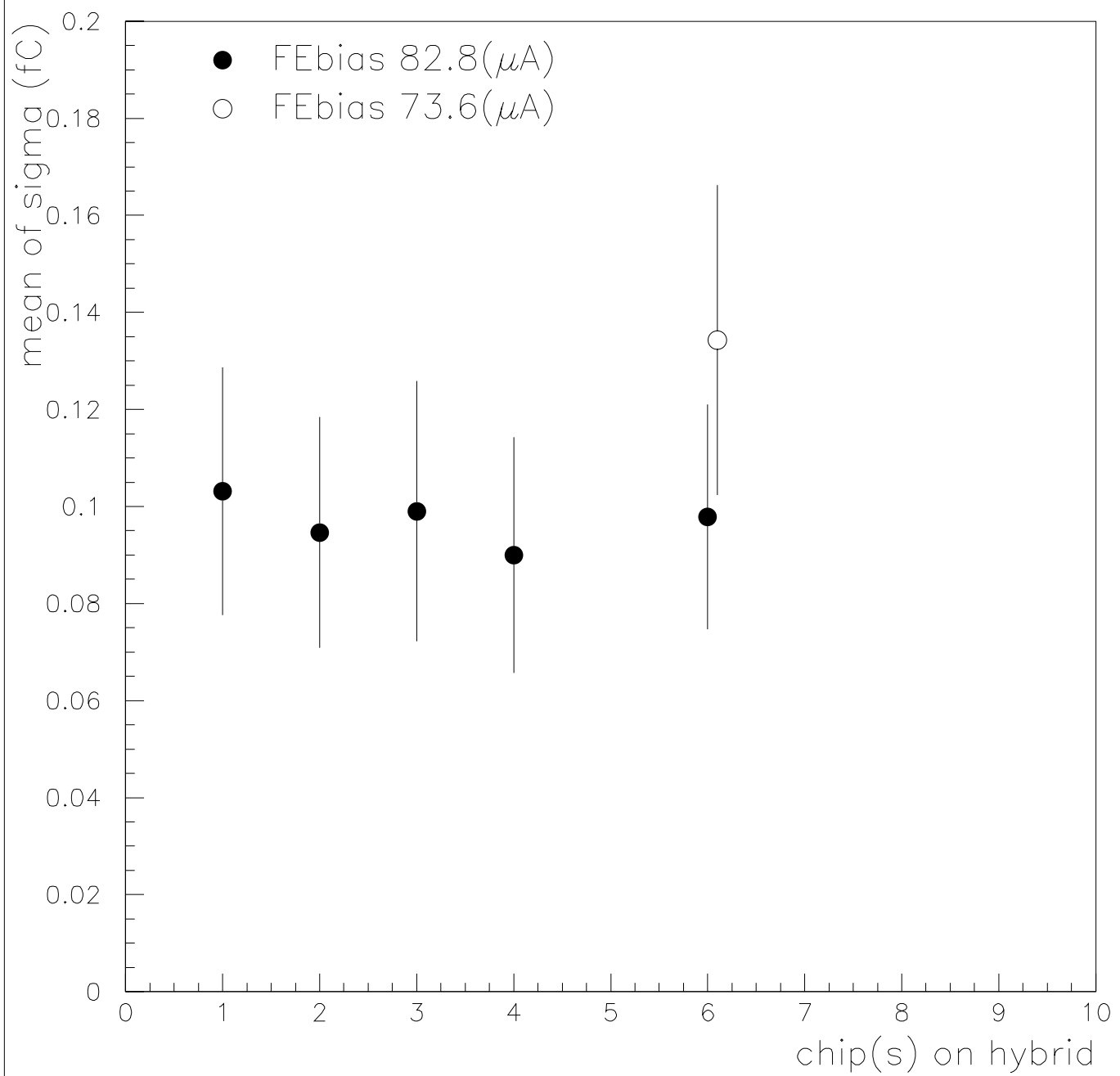
Noises in the 6 chips hybrid

- **Channel map and histograms**
 - Noise sigma is about 0.1 fC
 - There was a distinct pattern of failed channels -- every 4th ch.
- **Noise summary as a function of number of chips**
 - 1st chip: ~ 0.1 fC (at Lo-regime)
 - 2nd chip: ~ 0.1 fC (at Lo-regime)
 - The rest: very much the same
- **There was no increase of noise observed in the 1st chip as adding chips**
- **There were “failed” channels, every 4th channels**

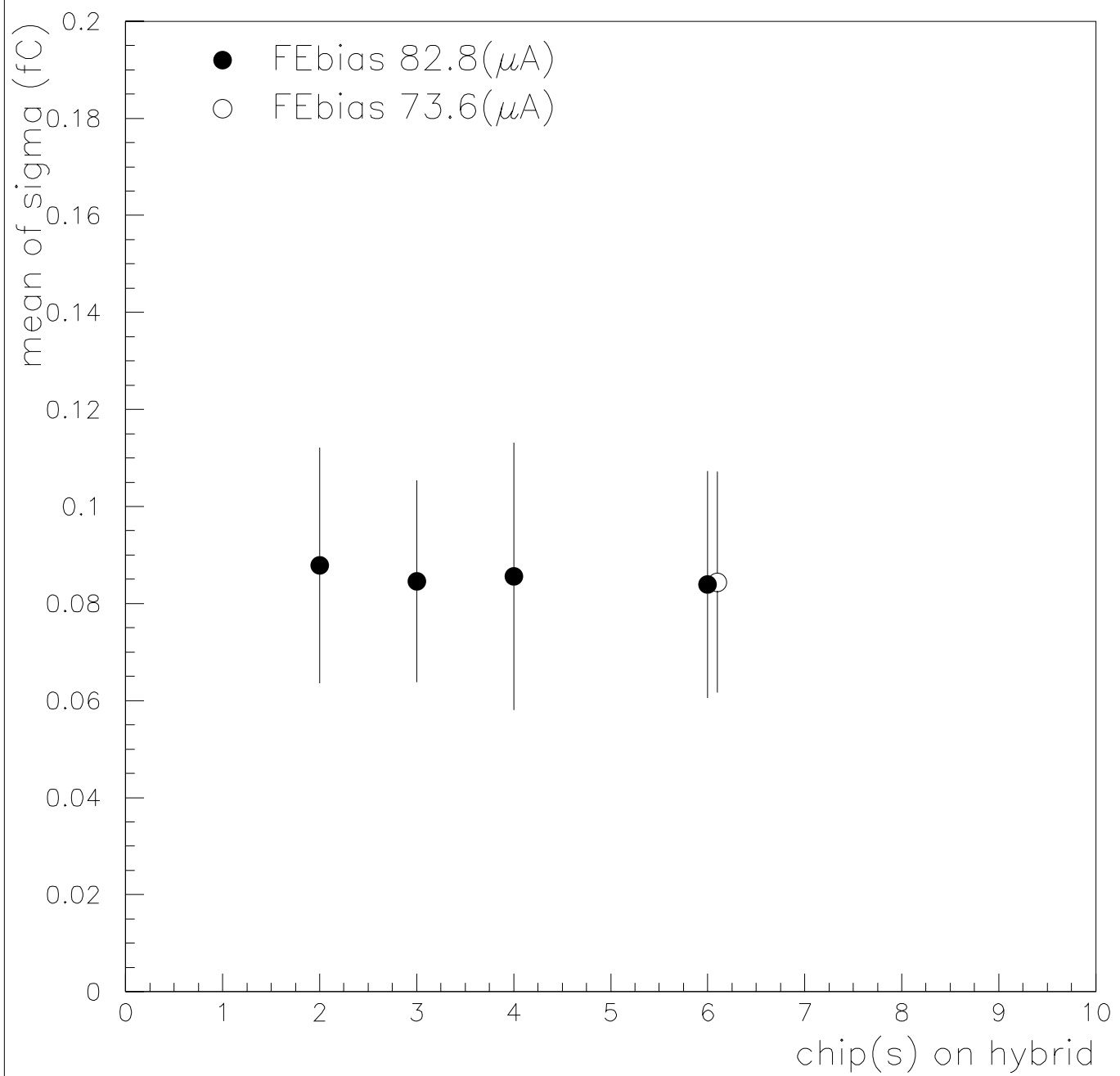
Gains and Offsets

- **Gains ~ 70 mV/fC, Offset 0**
 - The current offset values should be taken as an indicative of the non-linearity of the amplifier
- **Lower spread of the gains at the FE bias current at 73.6 μ A, although the amp became more non-linear...**

CHIP-1(threshold=300(mV))

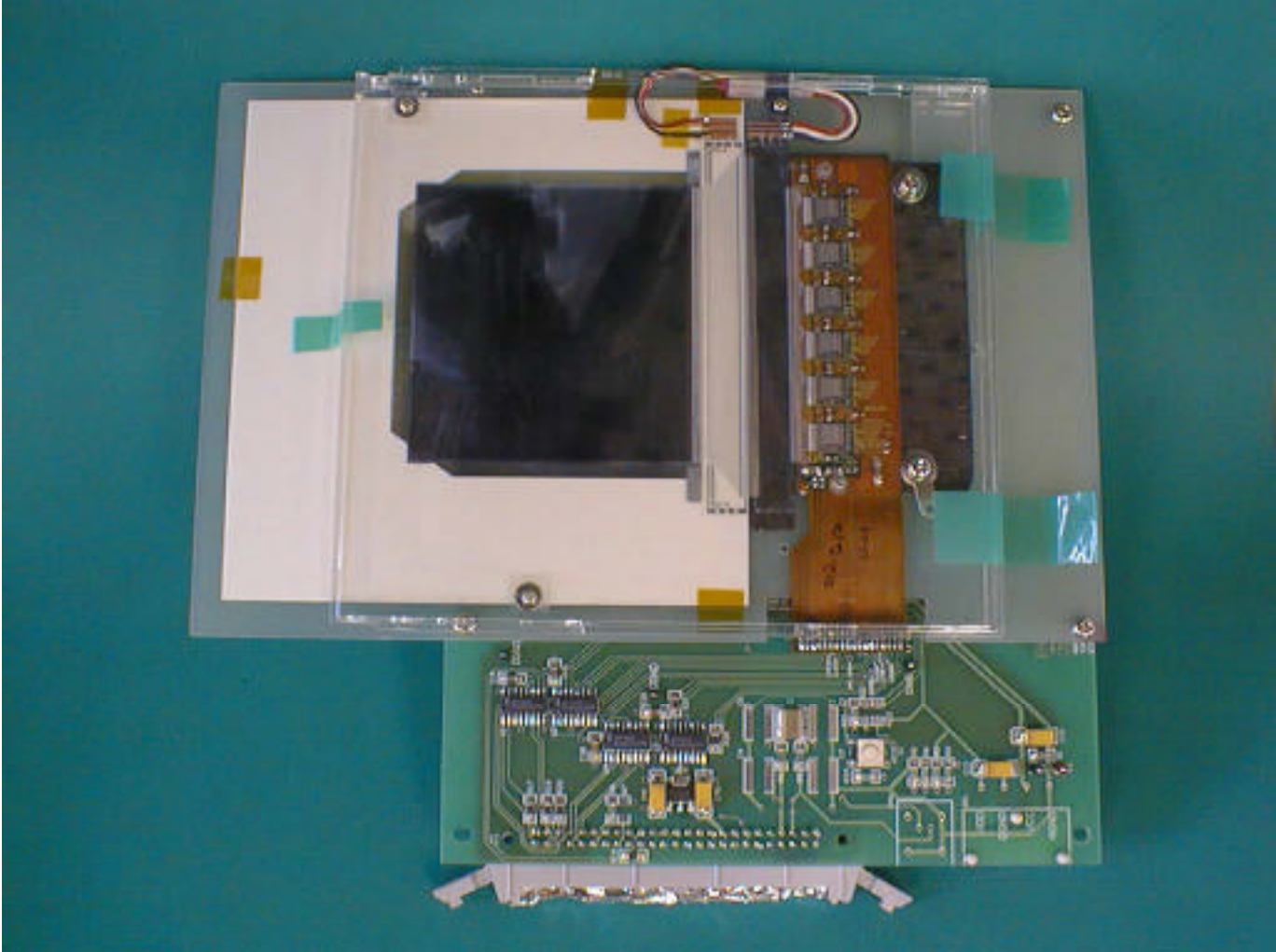


CHIP-2(threshold=300(mV))



Single-detector module with the 6 chips hybrid

- **One detector was bonded to the 6 chips hybrid**
- **There were 3 pitch adaptors involved, in total adding 2 to 2.5 cm of inter-strip capacitances**
- **The noise was much smaller in the FE bias current at 73.6 μA (Lo-regime), compared to at 211.6 μA (Hi-regime)**
 - **Bias voltage at 200 V**



12 Chips Hybrid

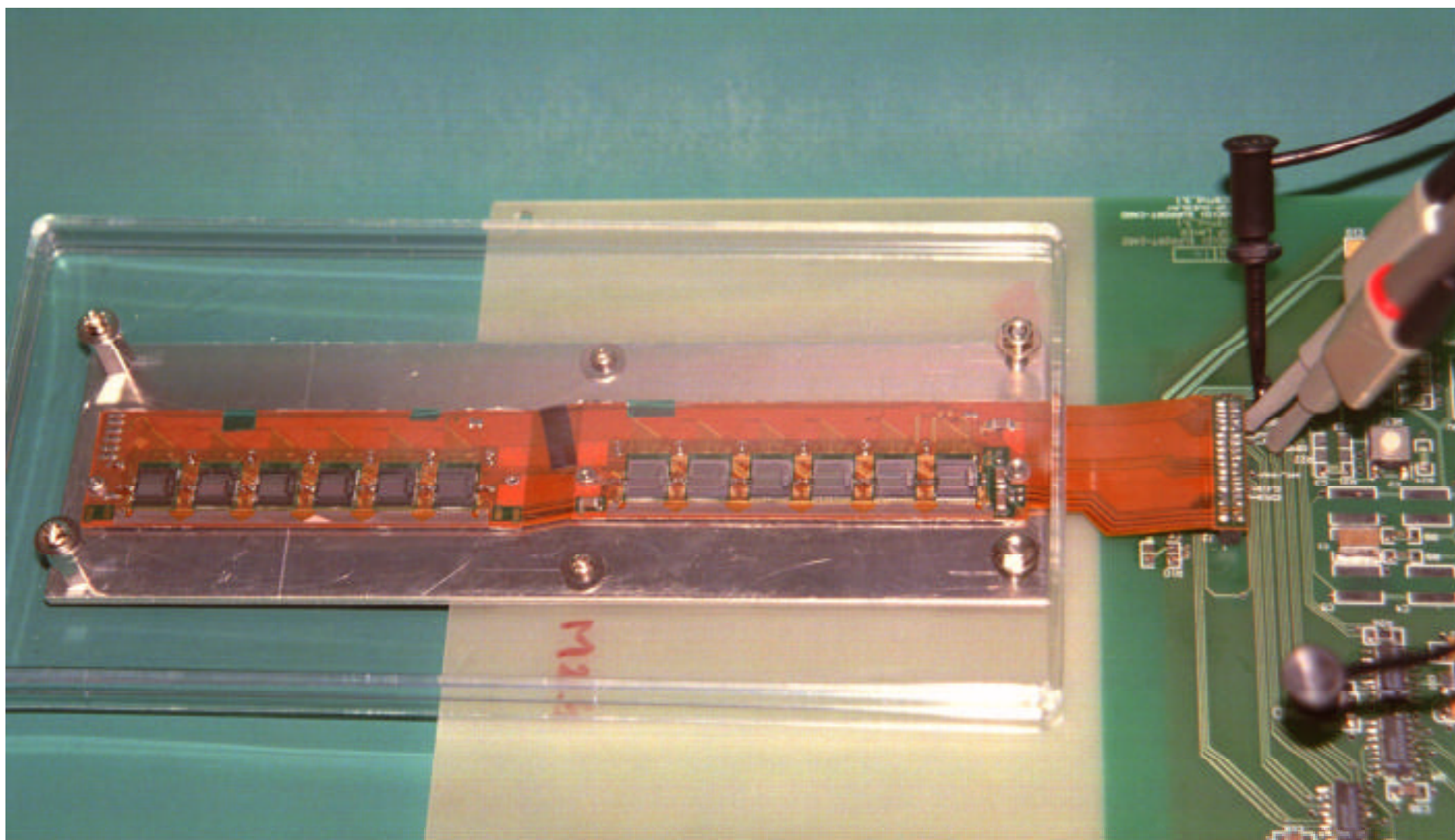
- **Loaded chip quality:**

- 6 “Good” chips -- Q 2 (first 6 chips, top hybrid)
- 6 “Poor” chips -- Q 1 (last 6 chips, bottom hyb.)

- **Charge injection scans**

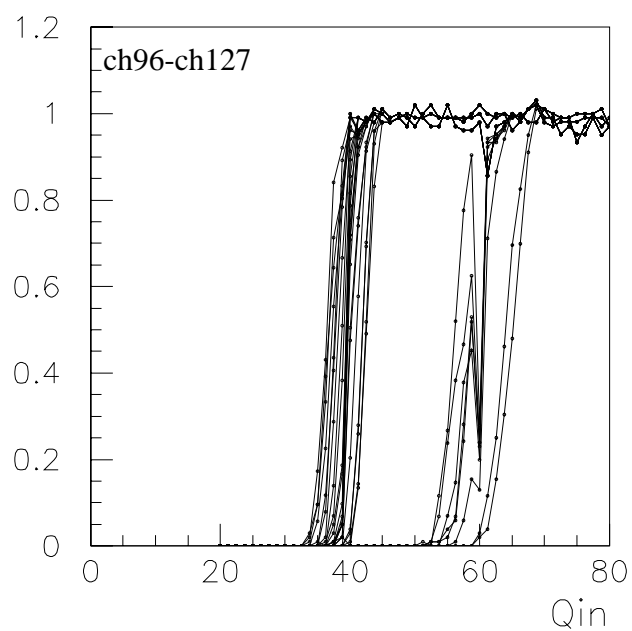
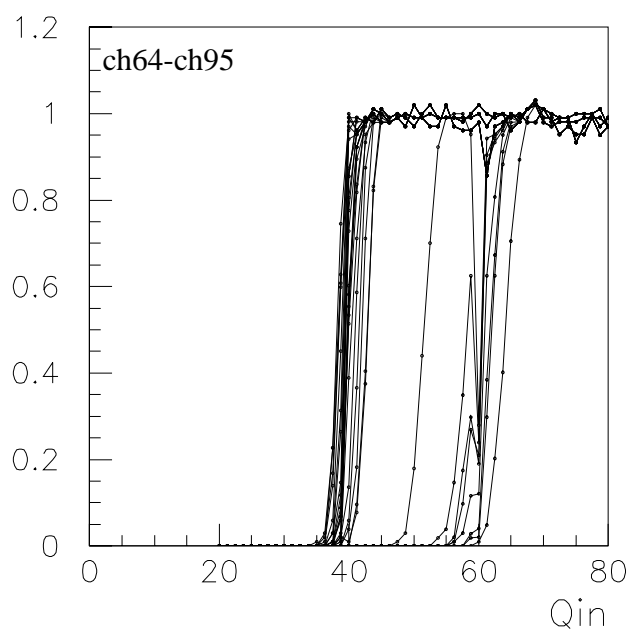
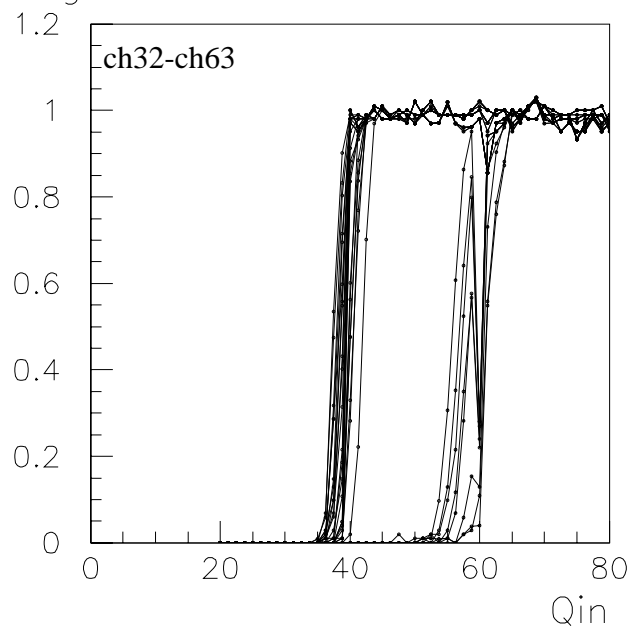
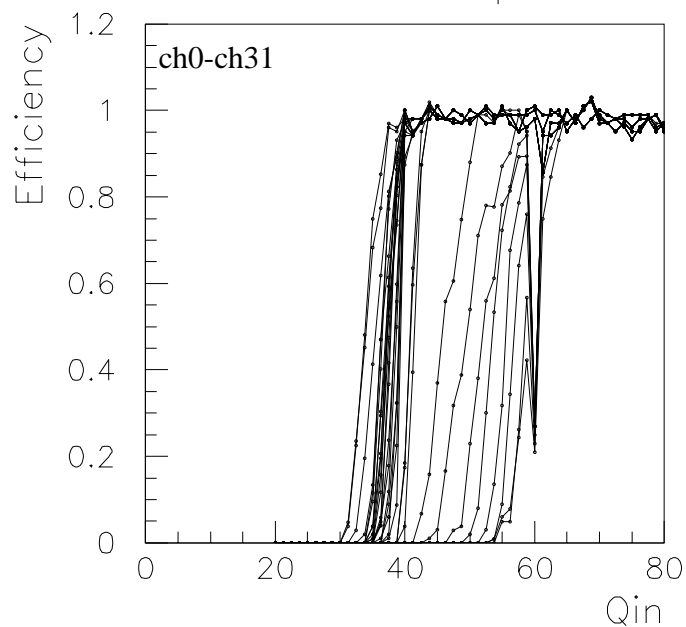
- EDGE mode
- Looked reasonable in the “Good” chips
- “Quantized efficiency saturation below 1” was observed in the “Poor” chips, which was attributed to the point defects in the 12 cell pipeline for multiplexing
- There were 2 reasonable chips in the “Poor” group, and possibly reasonable number of channels which are “12 cell defect” free.

- **Noises, Gains, Offsets were obtained from the charge injection scans**

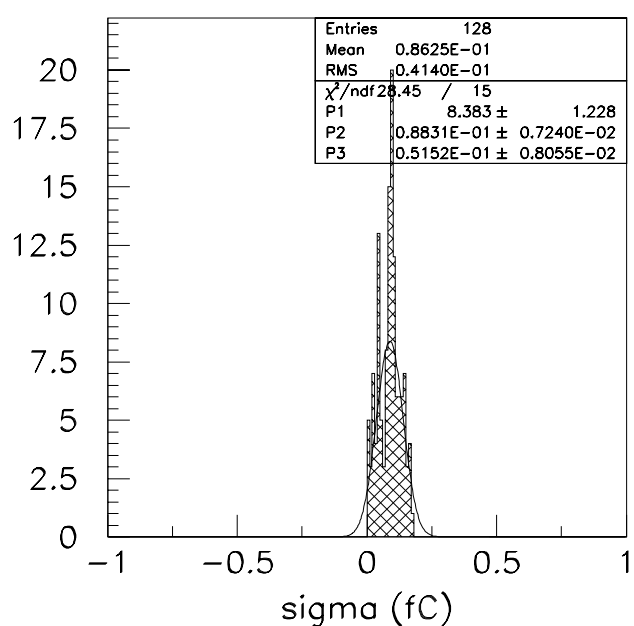
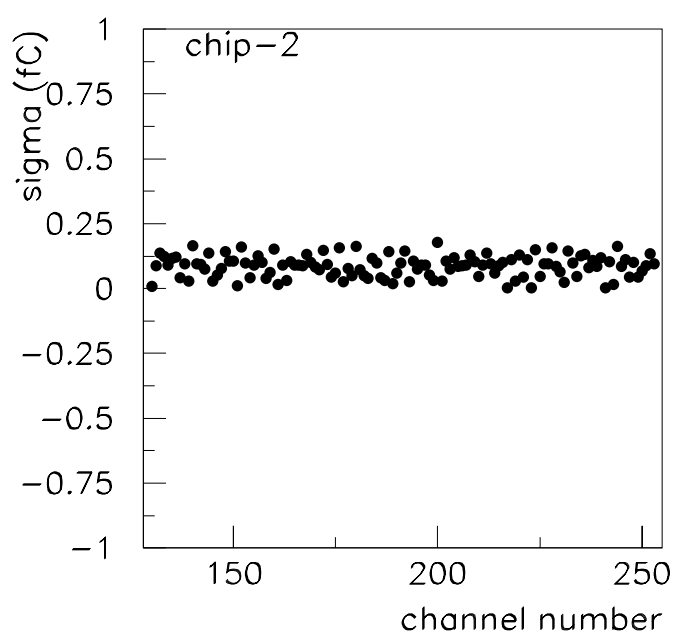
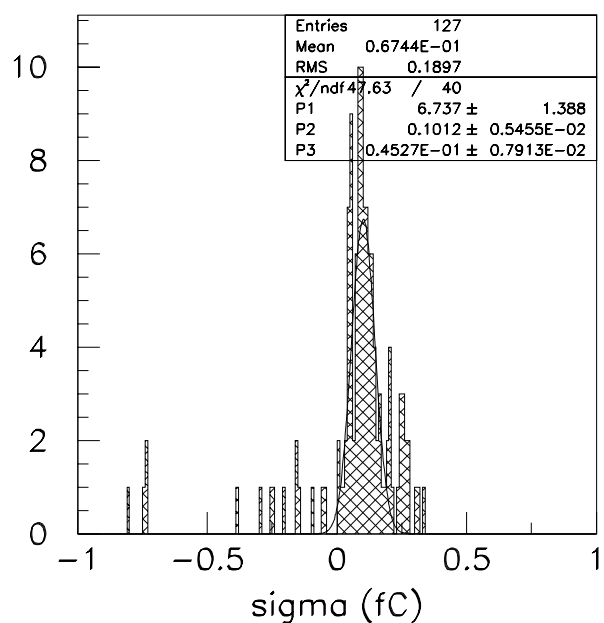
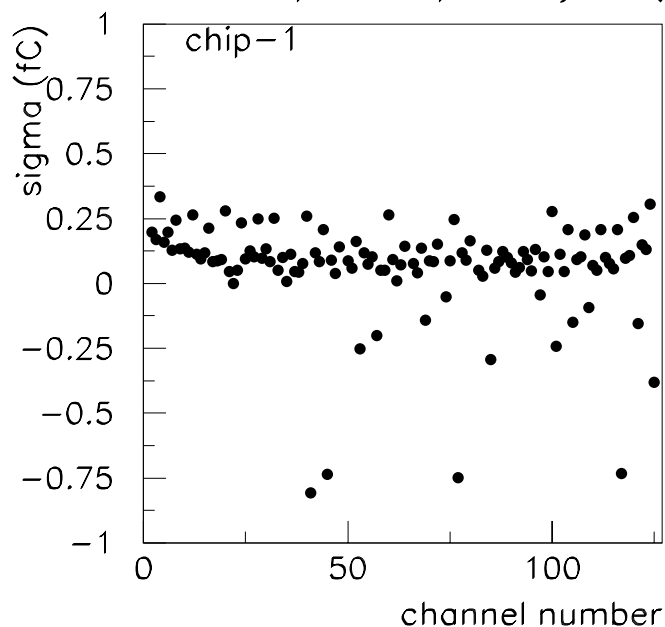


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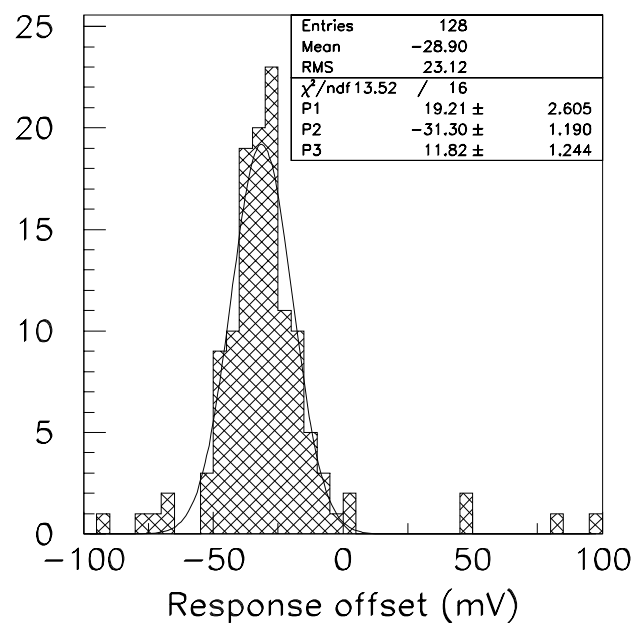
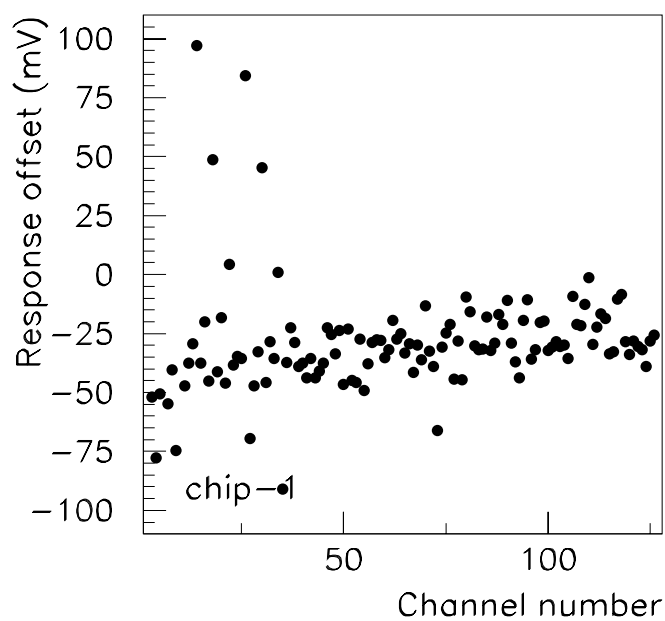
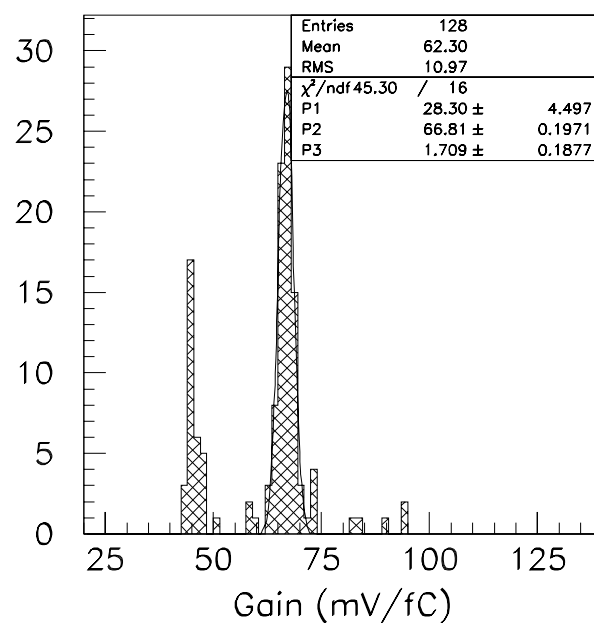
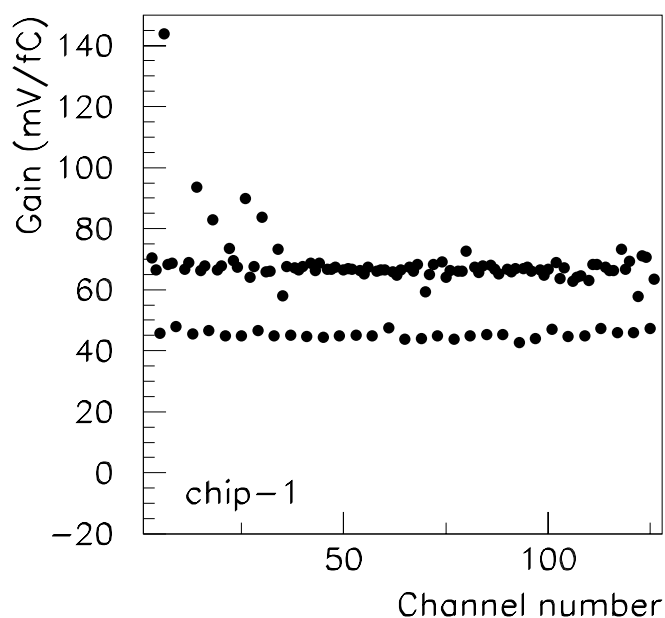
qinb74t300edge.dat- zz



12chips on Kapton-Hybrid (FEbias 73.6(μ A), threshold 300(mV))

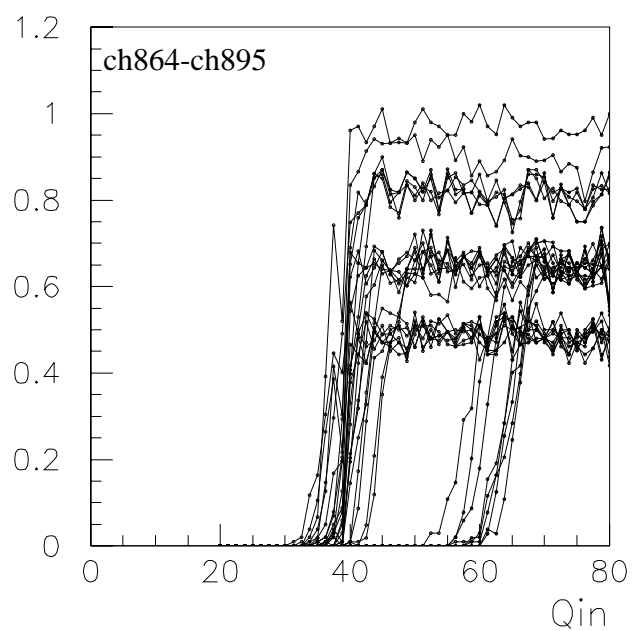
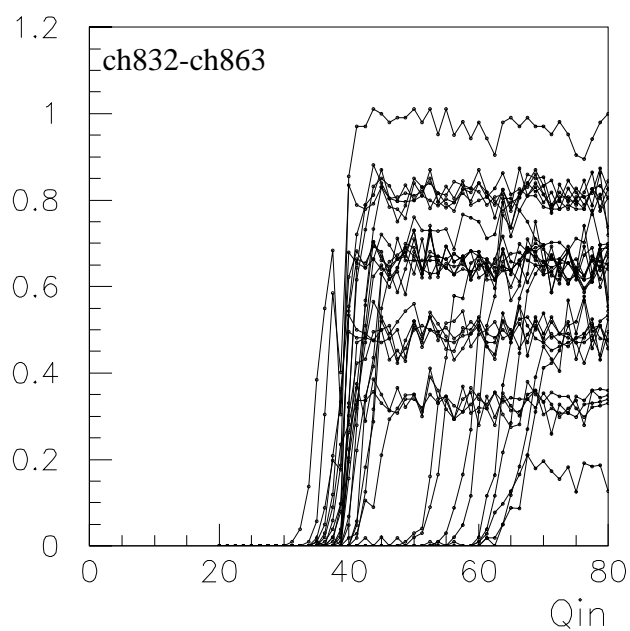
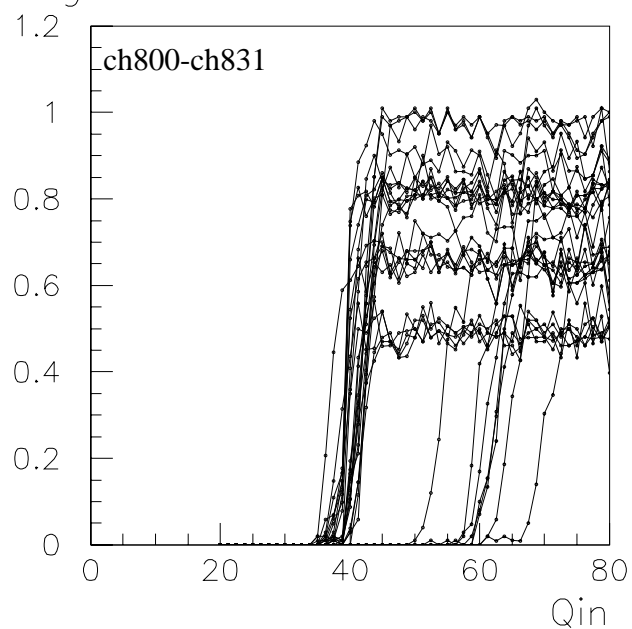
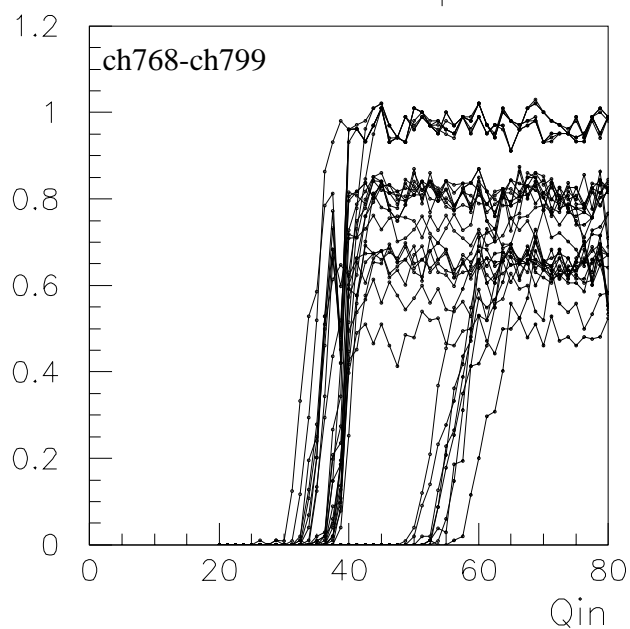


12chips on Kapton-Hybrid (FEbias $73.6(\mu\text{A})$)



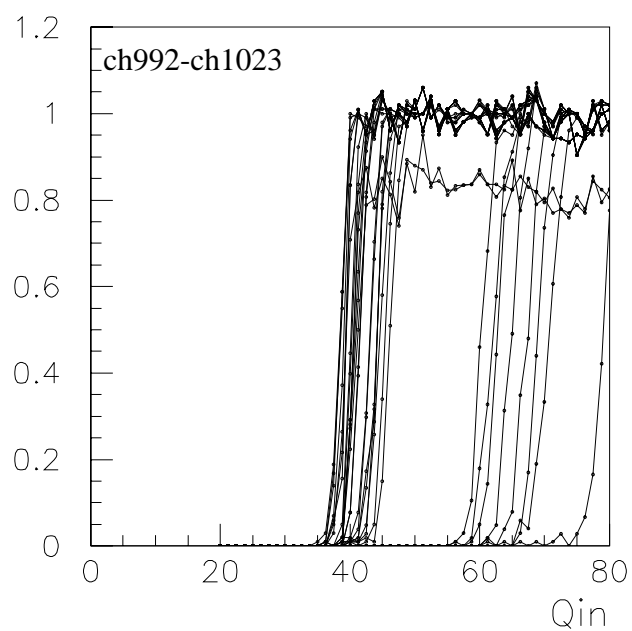
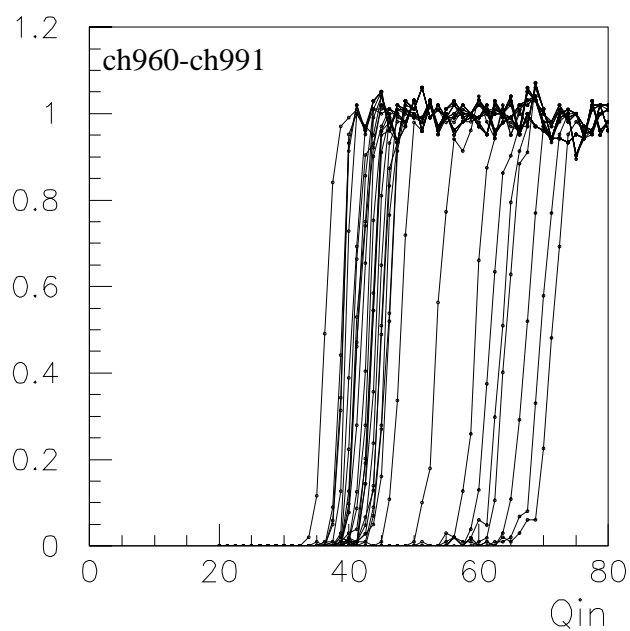
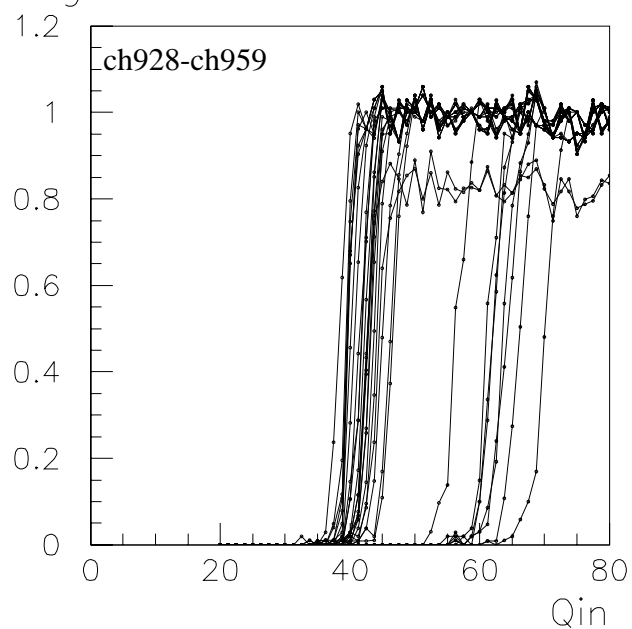
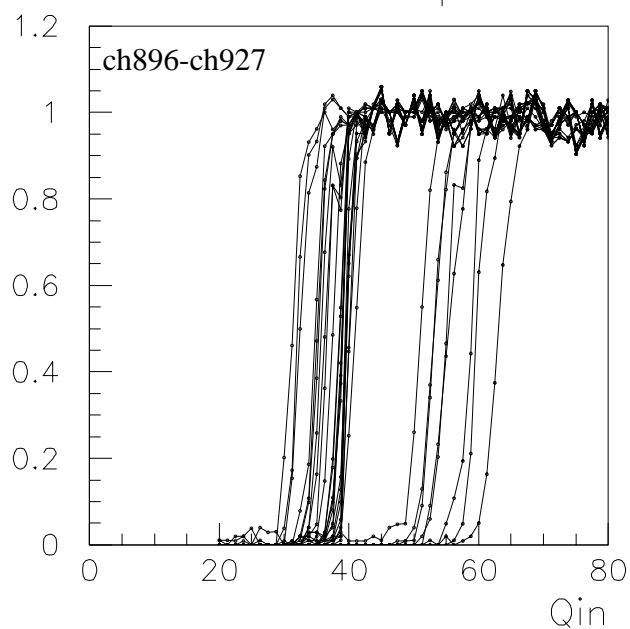
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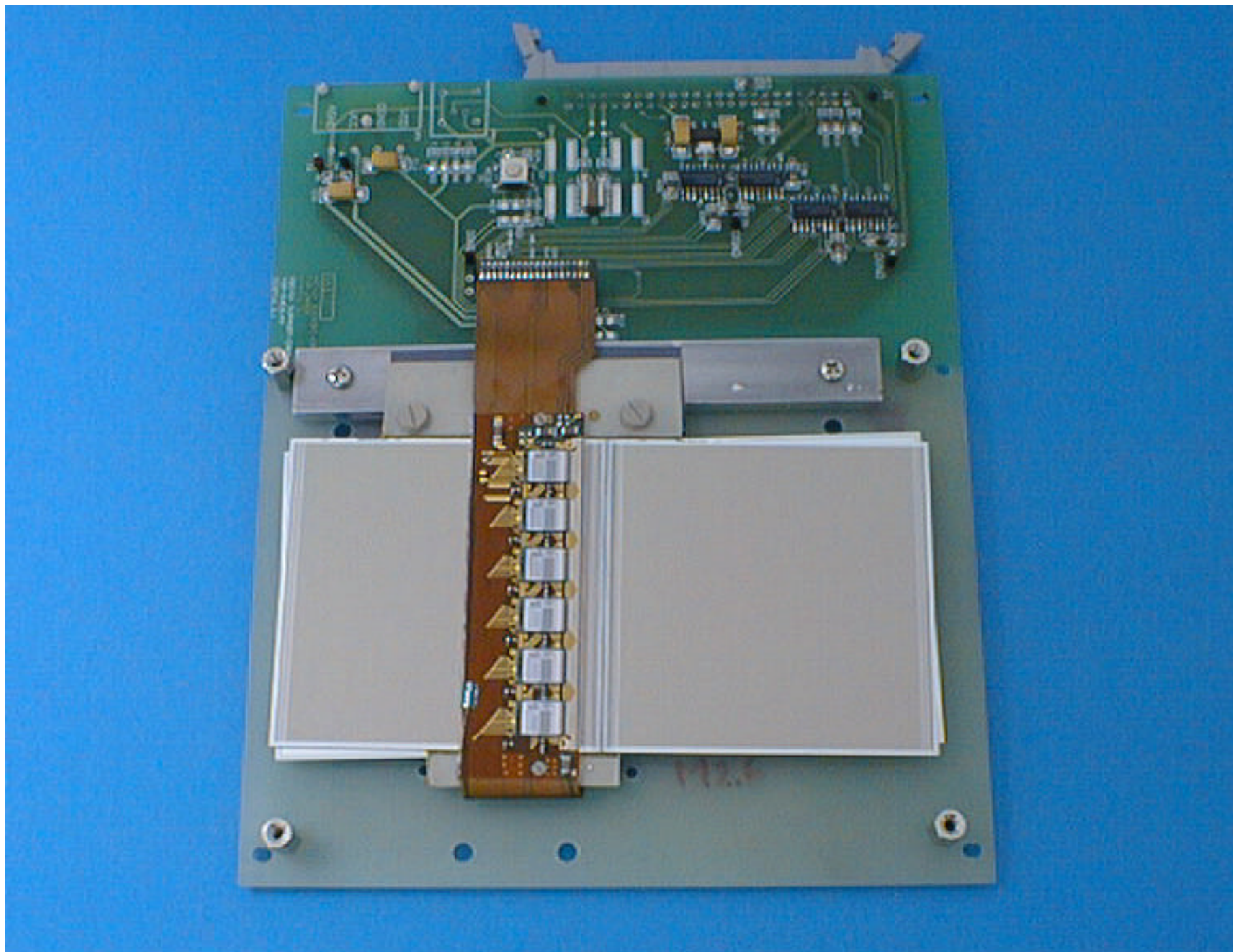
qinb74t300edge.dat- zz



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qinb74t300edge.dat- zz





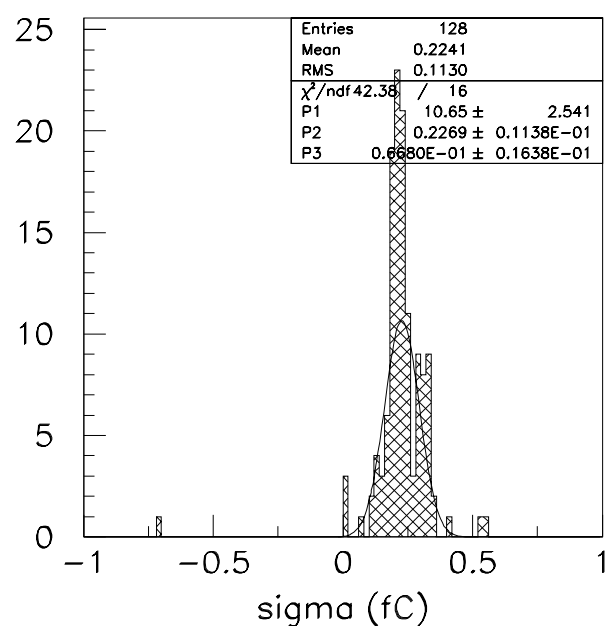
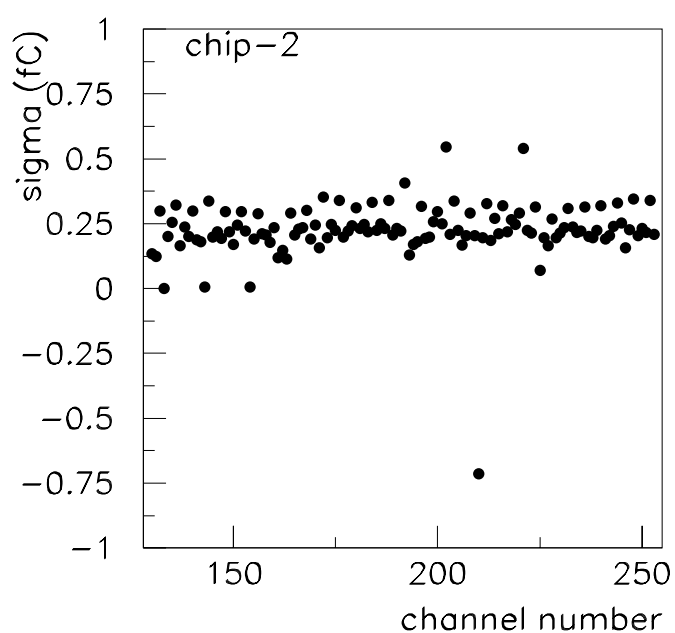
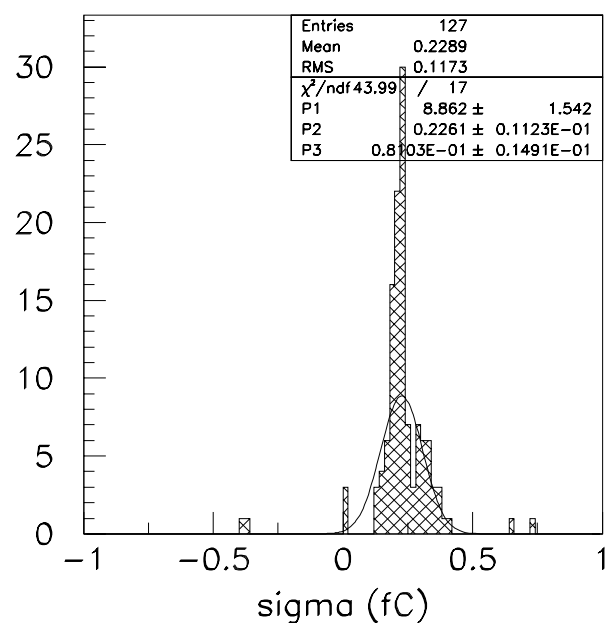
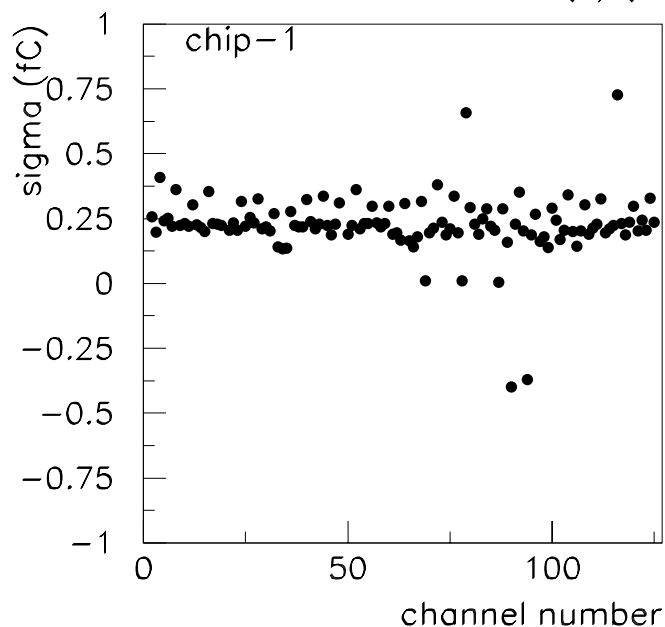
12 Chips Full Electrical Module

- **4 n-on-n ATLAS97 novel p-stop detectors, matching the n-ABCD chips**
- **Double-side instrumented**
- **First 4 channels were un-bonded out of 32 channels in each chip**
- **Charge injection scan, with the bias voltage at 200 V**
 - Done only on the top hybrid, (failed on the bottom hybrid by missing to selecting the link)

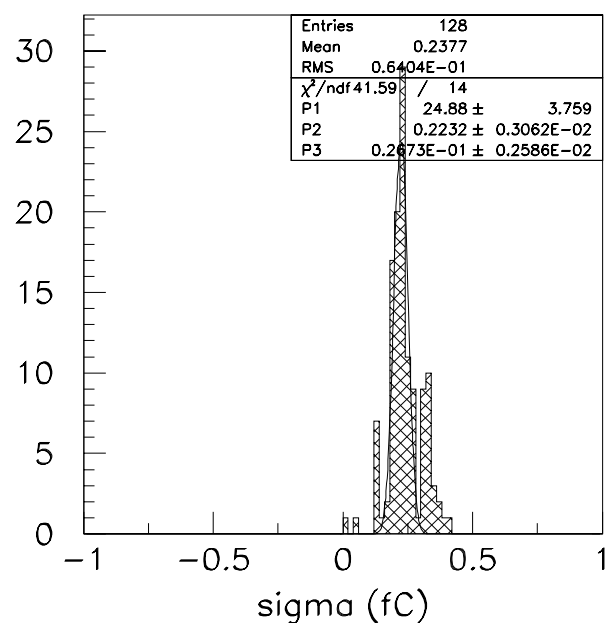
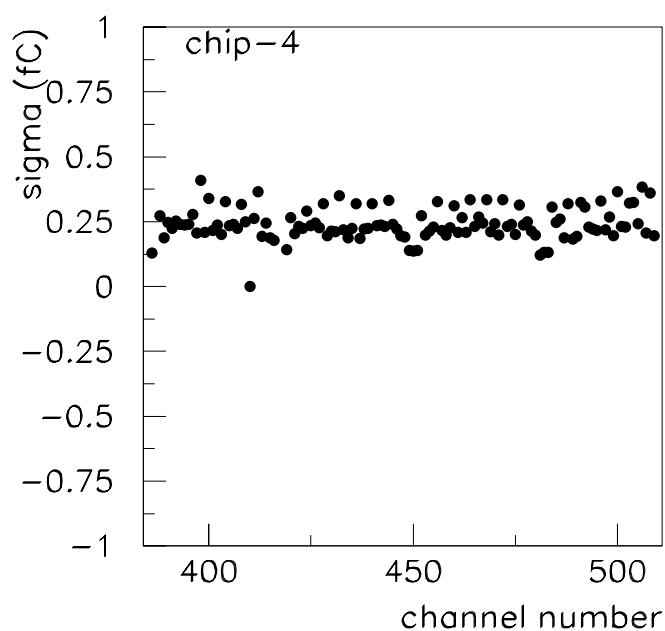
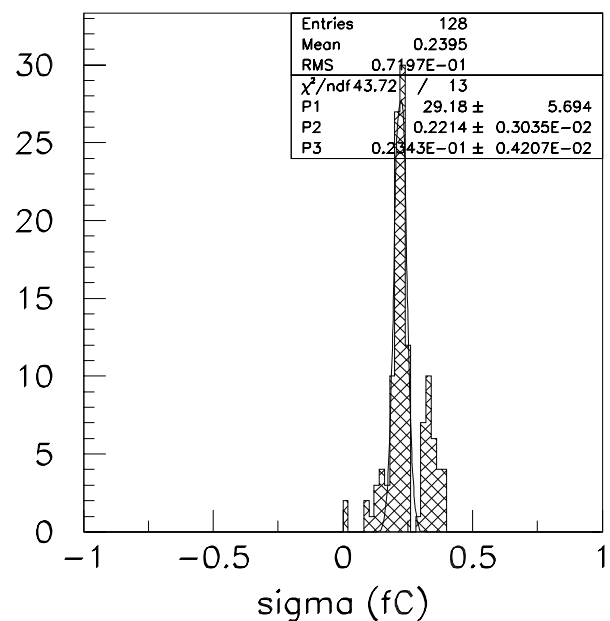
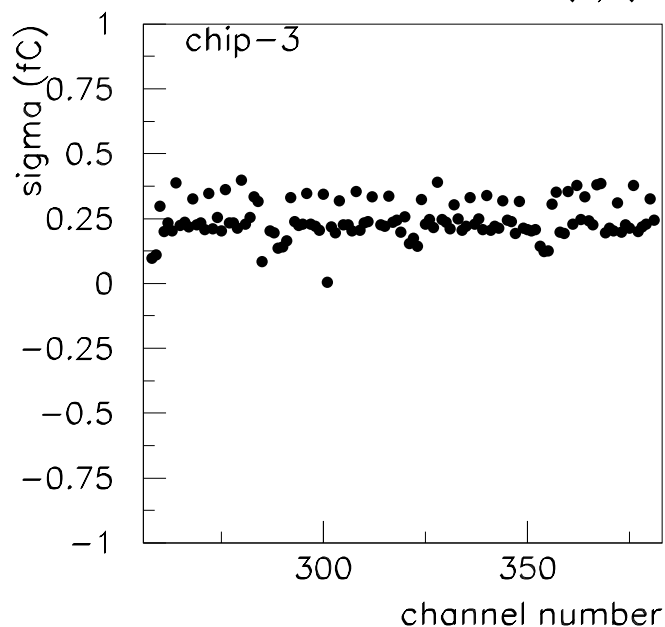
Noise, Gain, Offset

- **Noise increased (from about 0.1 fC) to 0.23 ~ 0.25 fC, because of the detector capacitance**
 - The noise sigma of 0.25 fC = 1563 e, which is within the electronics specification (TDR)
- **Gains and Offsets (from linear fit)**
 - Gain increased a bit (compared to the hybrid only)
 - Offset became more negative (compared to the hybrid only)
 - These can be understood as a result of non-linearity of gain curve -- being investigated
- **Gain was reasonably uniform, within the chips, and over the chips**
- **Repetitive pattern of every 4th channels**
 - Low gain
 - Unclear whether they were “offset”

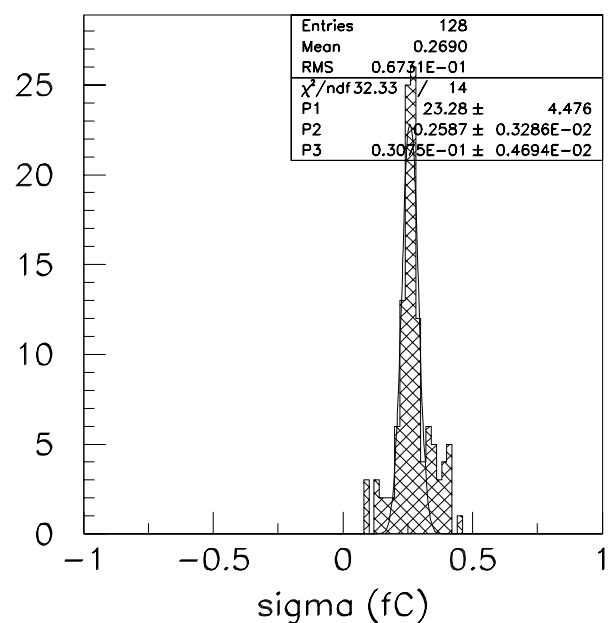
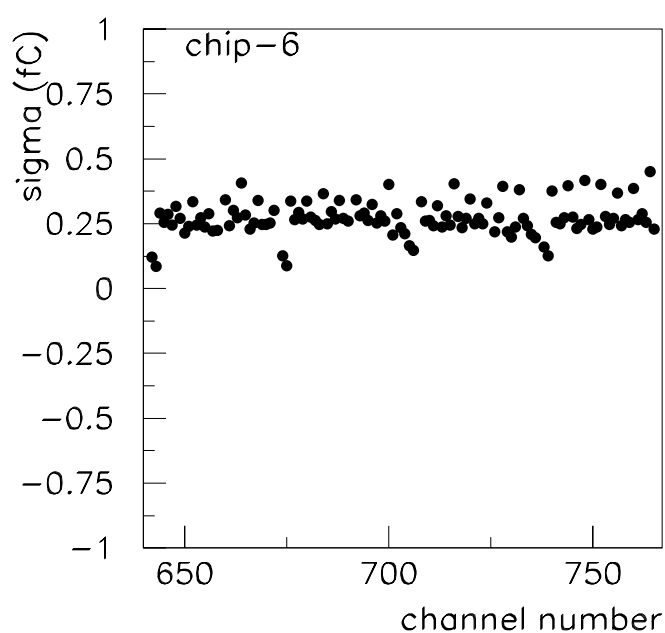
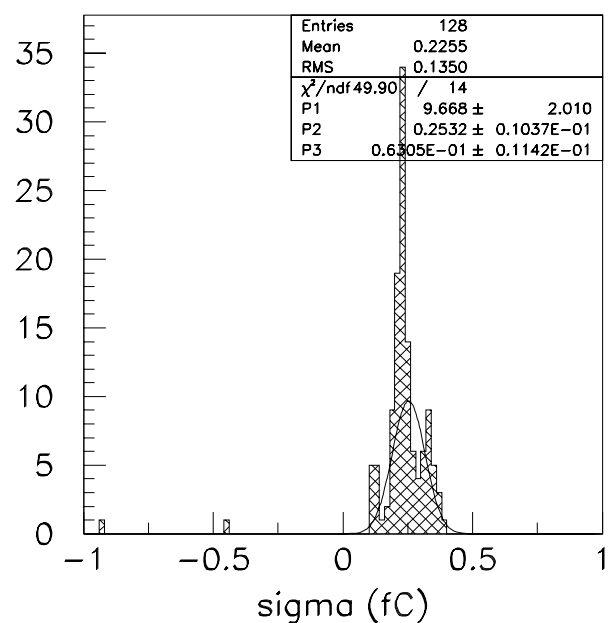
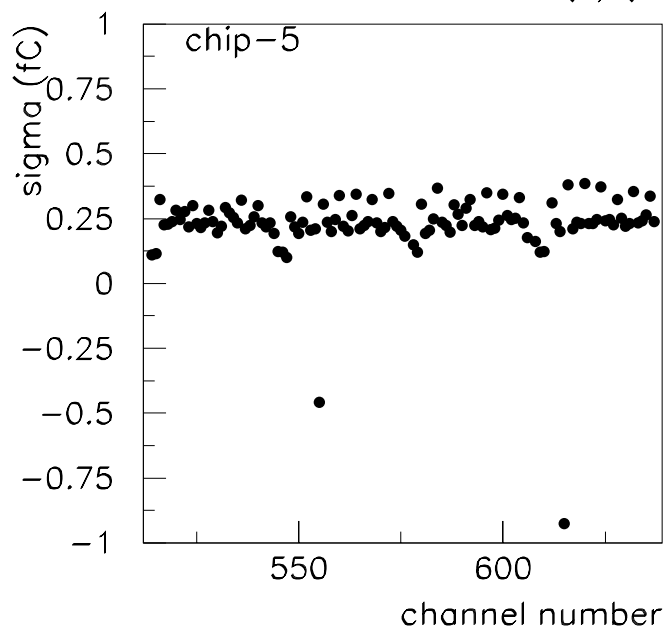
Fullmodule Bias 200(V) (FEbias 73.6(μ A), threshold 300(mV))

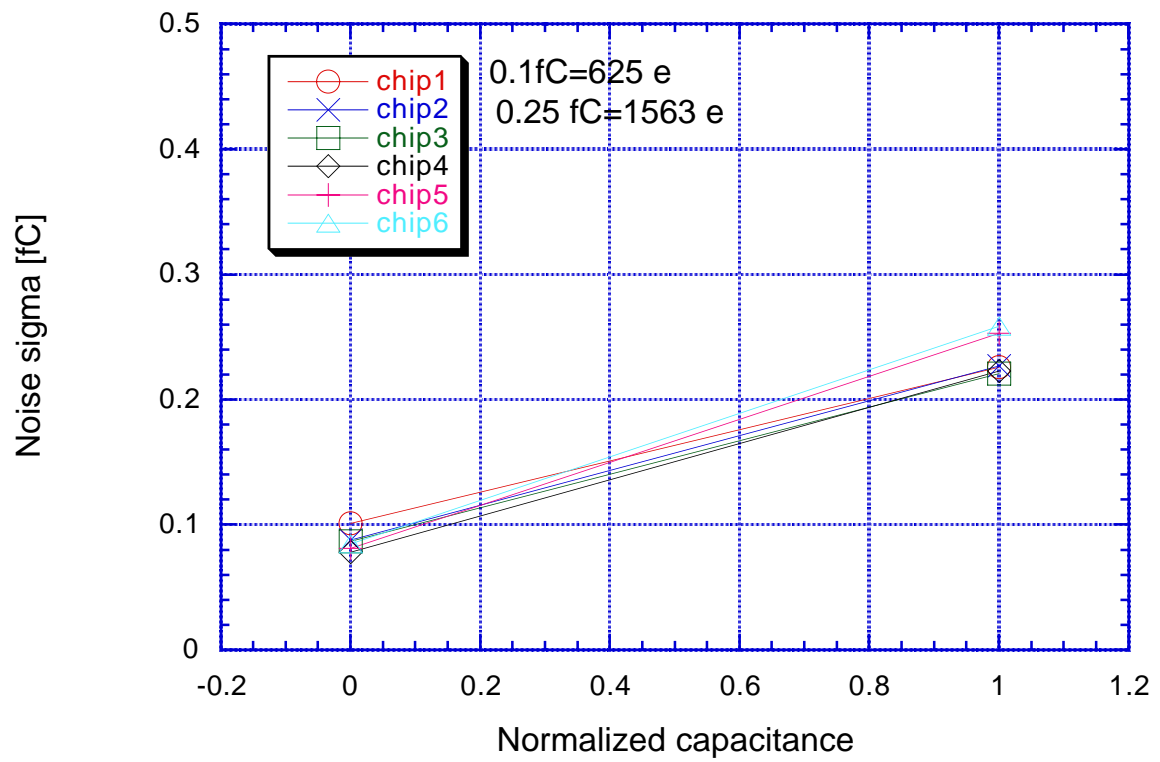
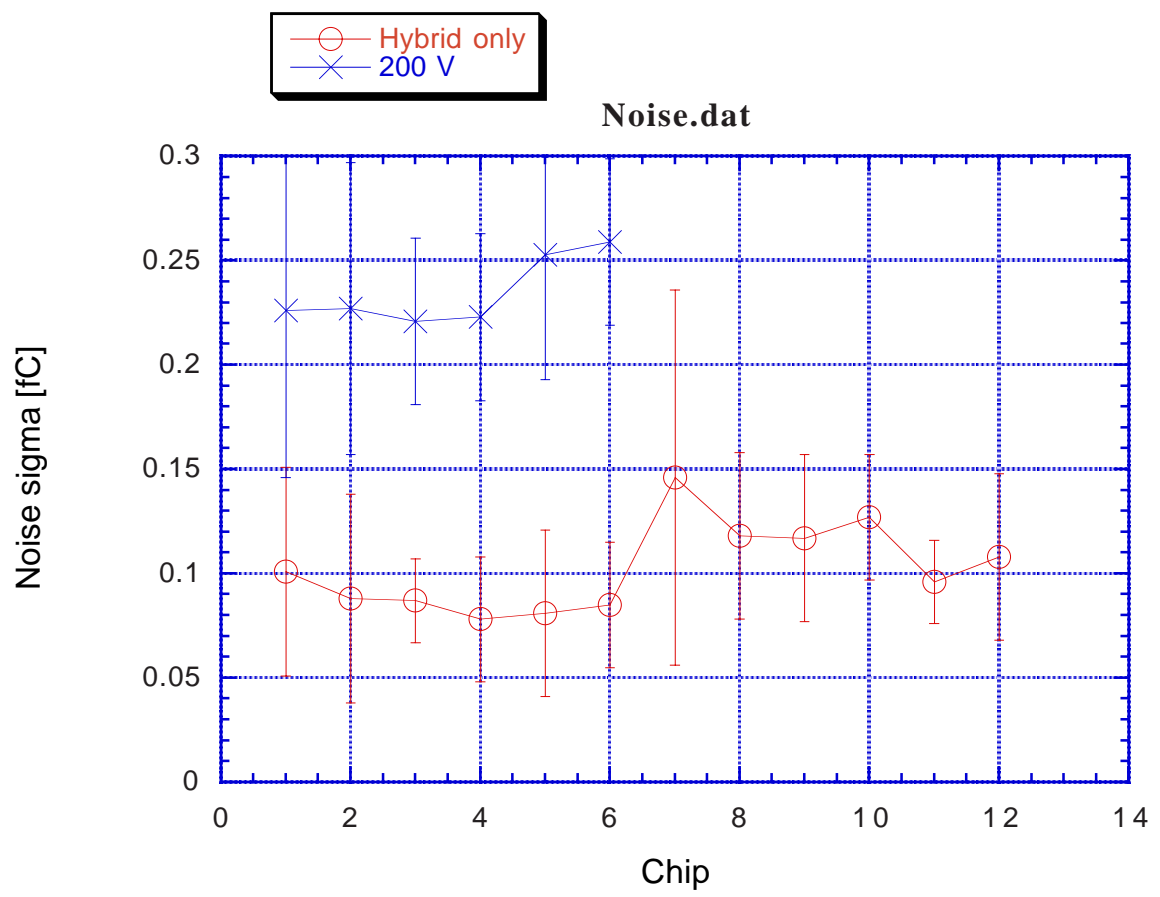


Fullmodule Bias 200(V) (FEbias 73.6(μ A), threshold 300(mV))

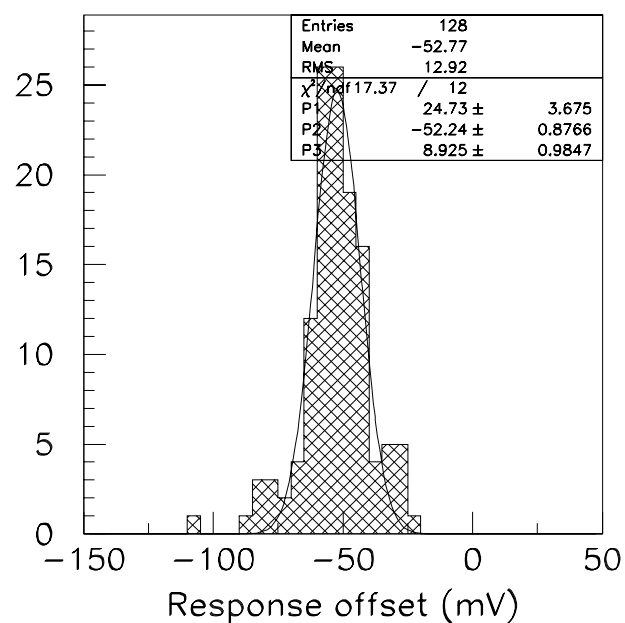
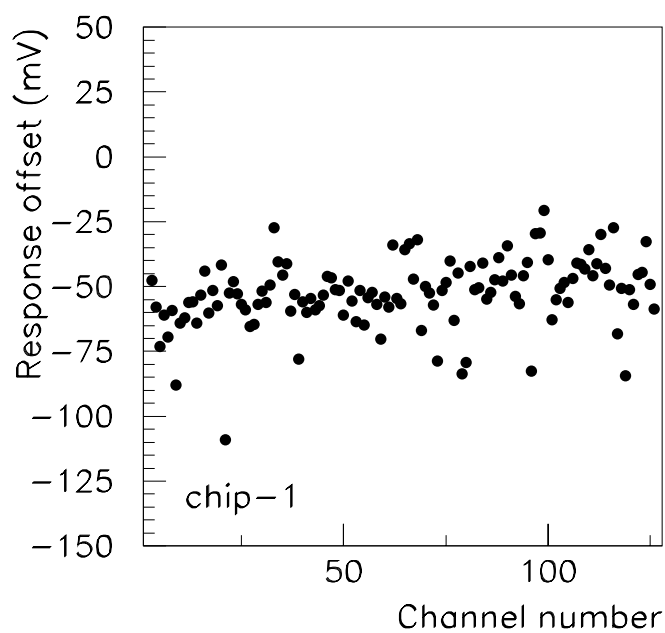
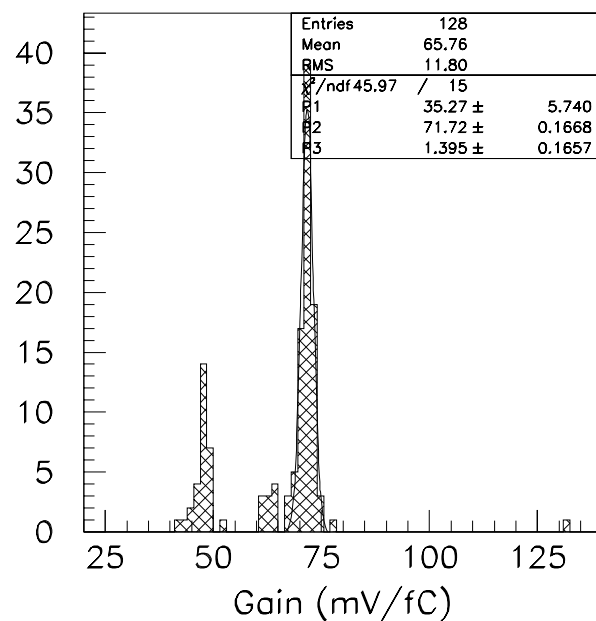
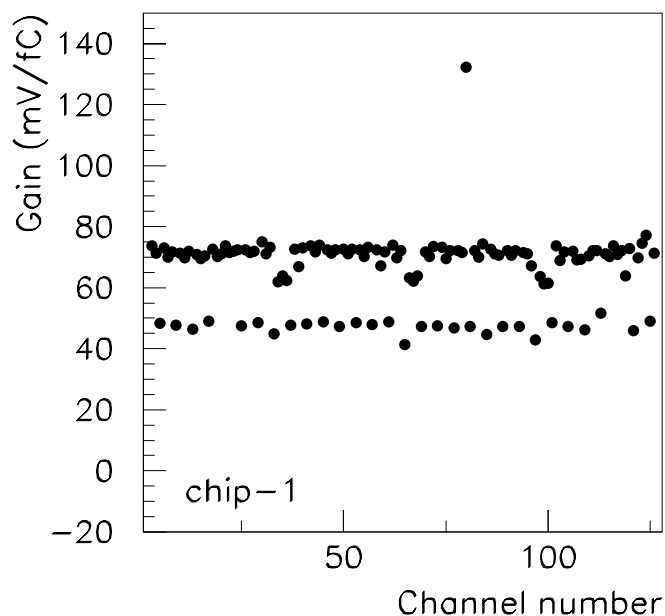


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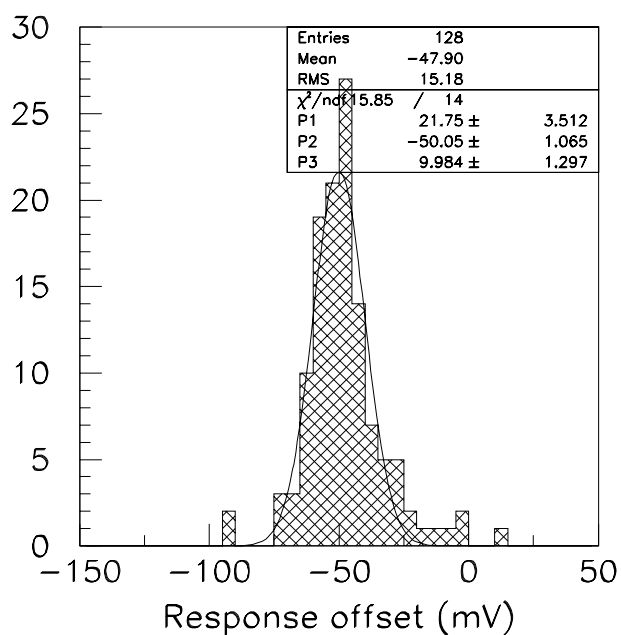
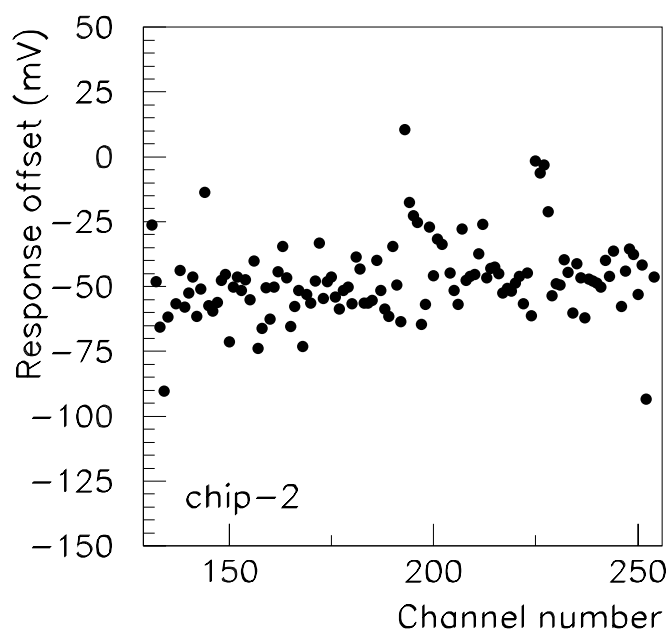
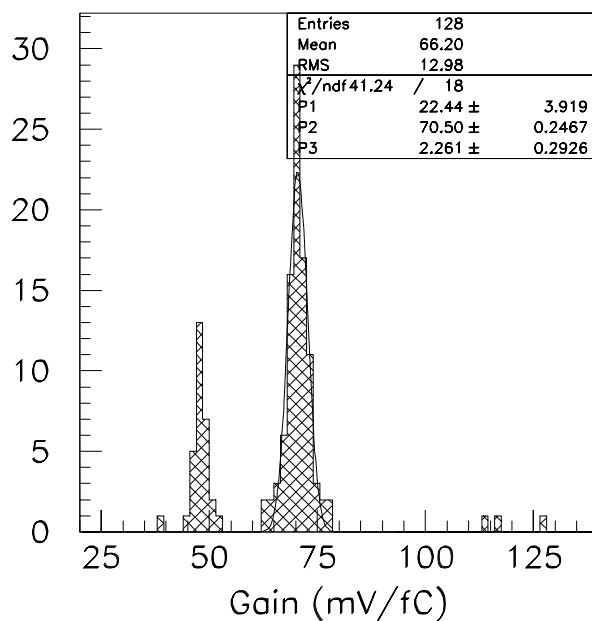
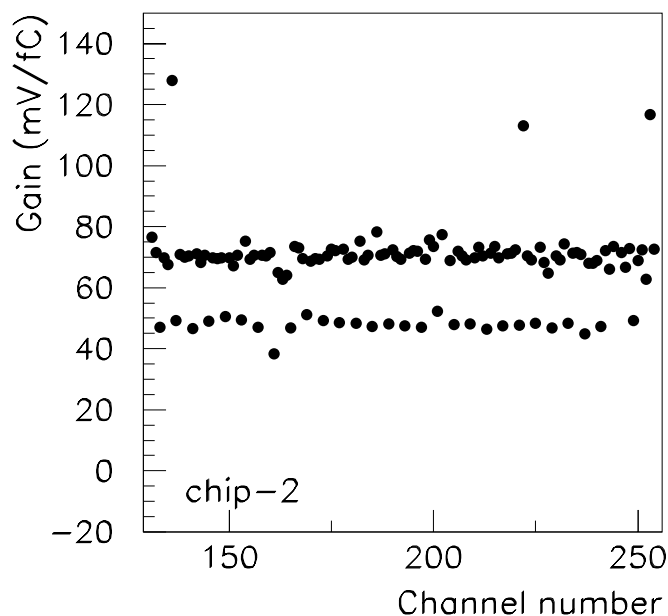




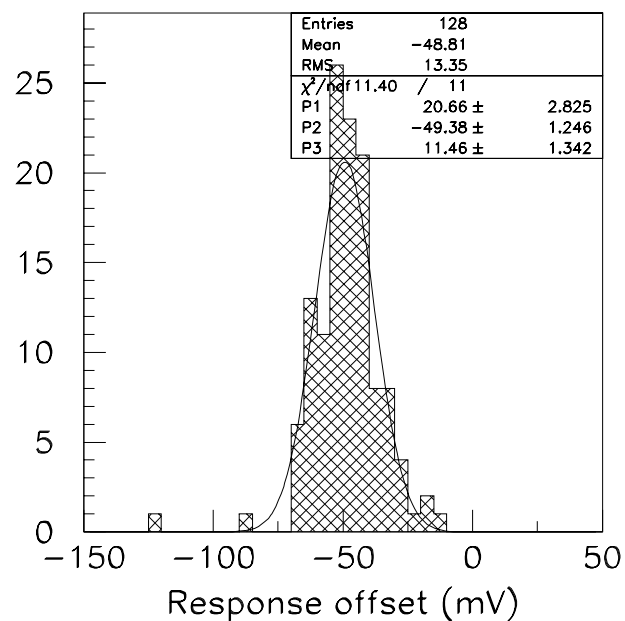
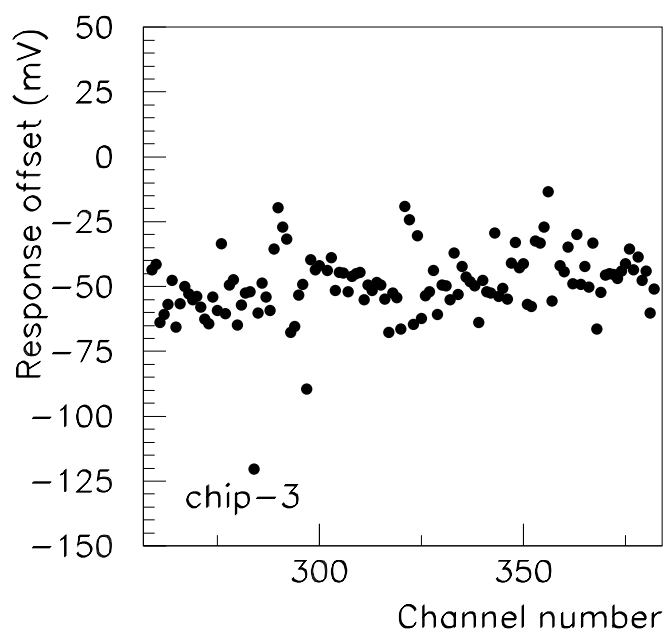
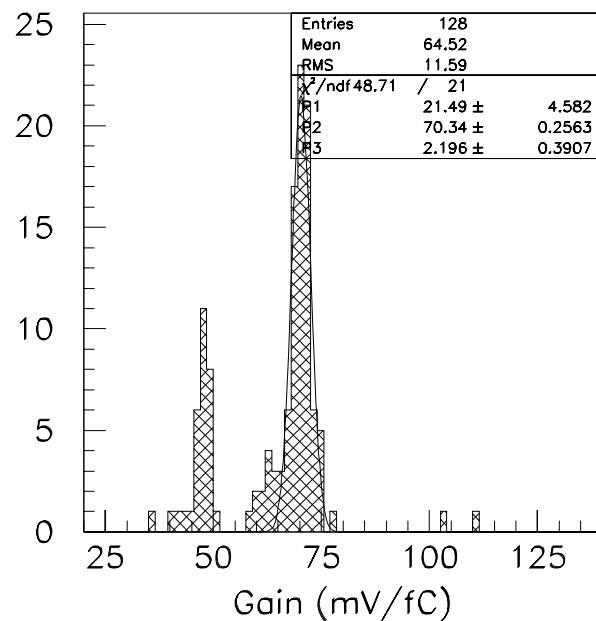
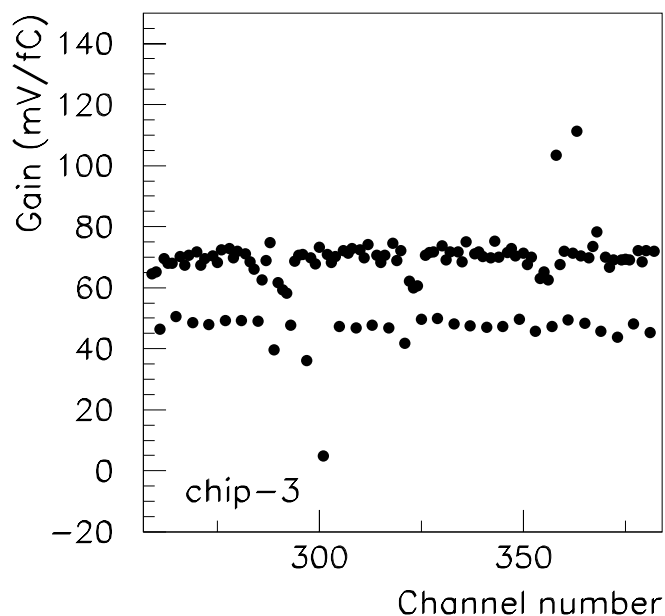
Fullmodule Bias 200(V)(FEbias 73.6(μ A))



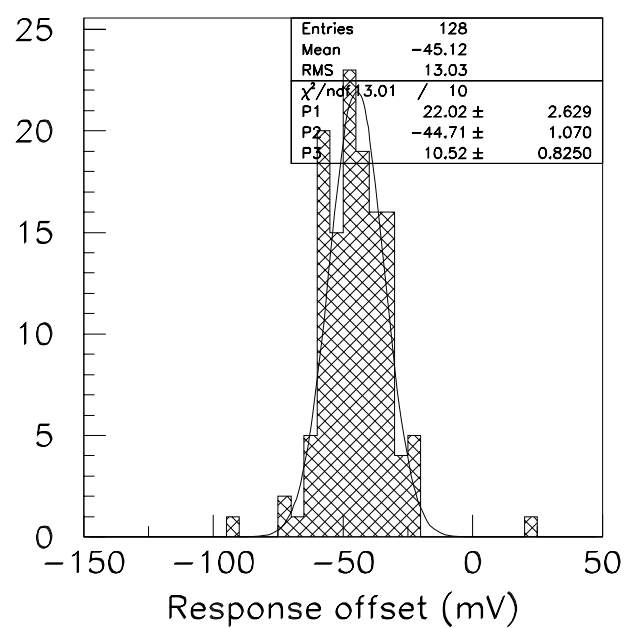
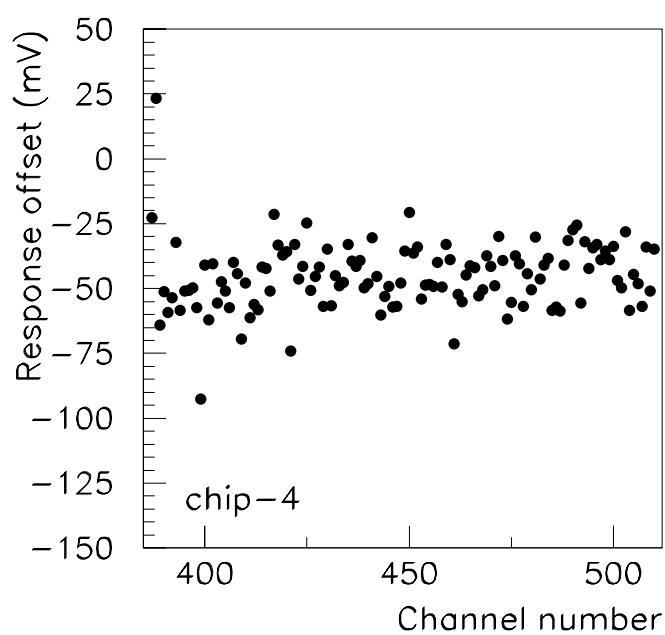
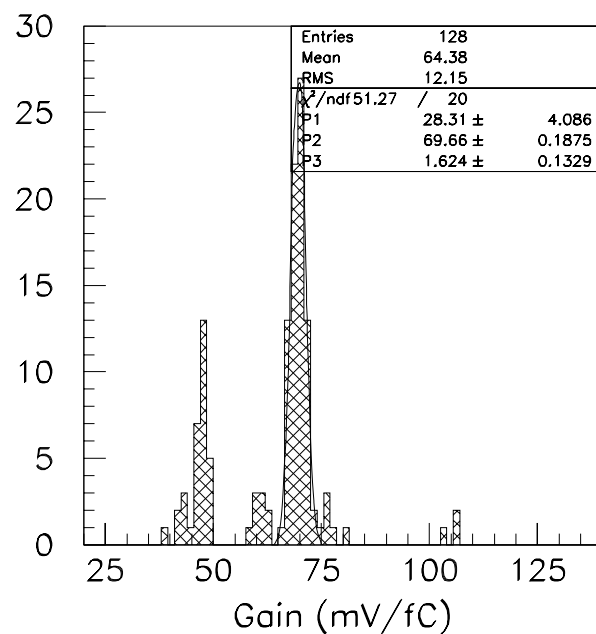
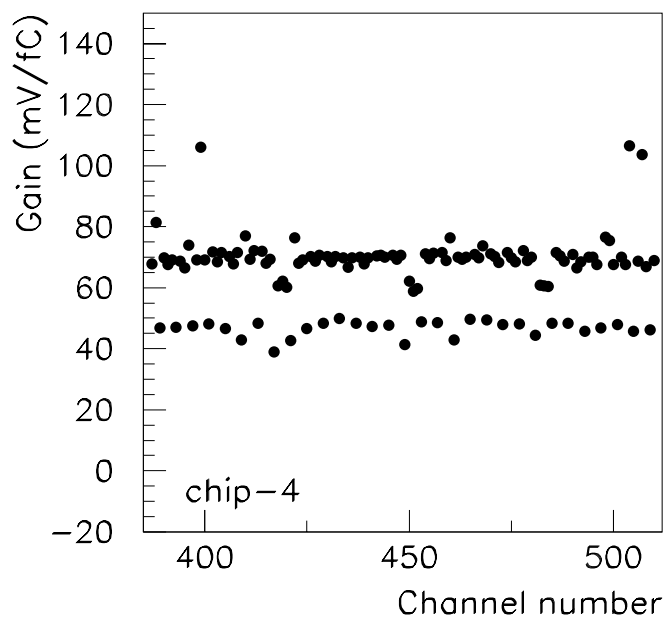
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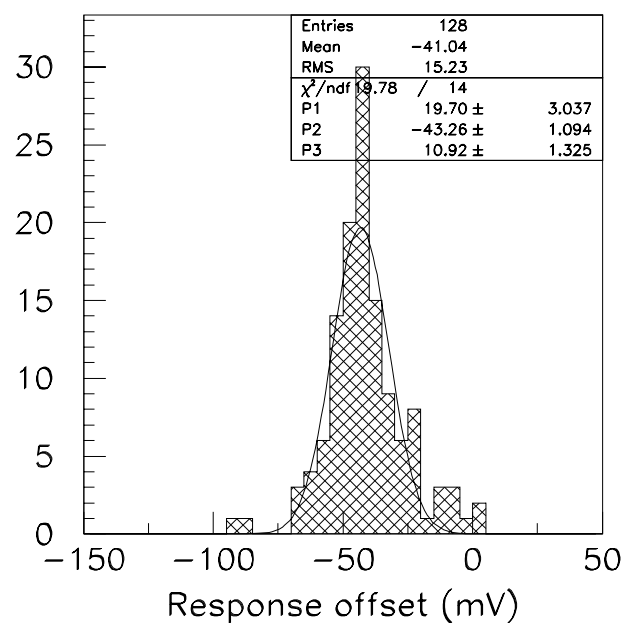
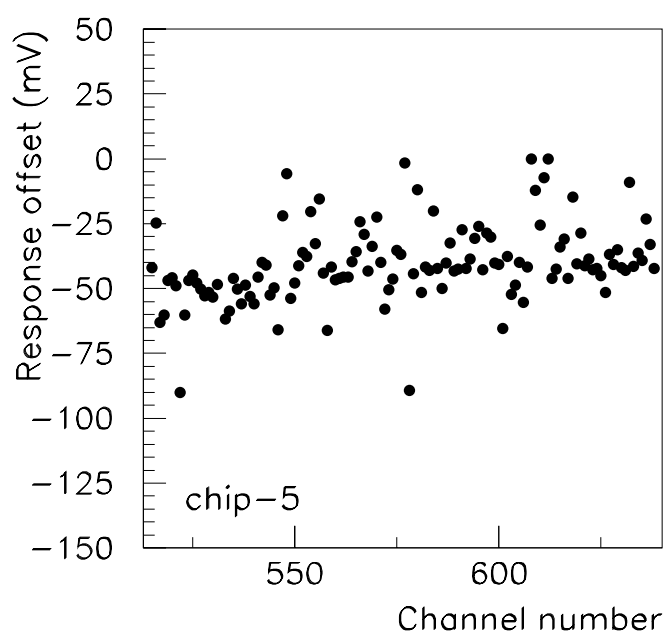
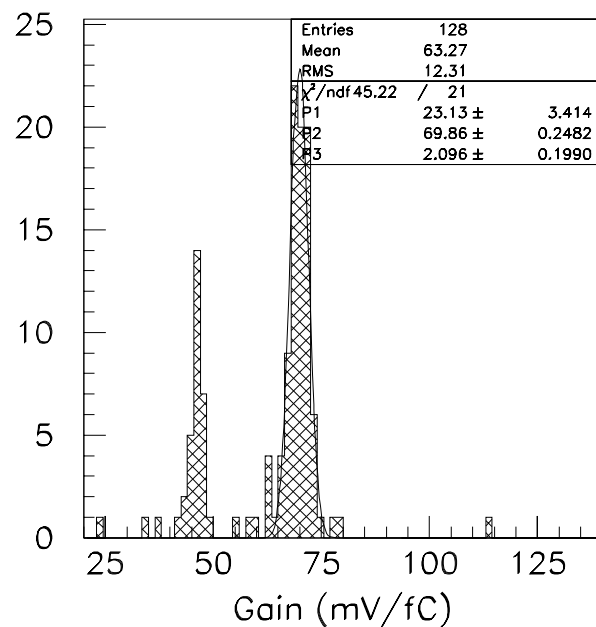
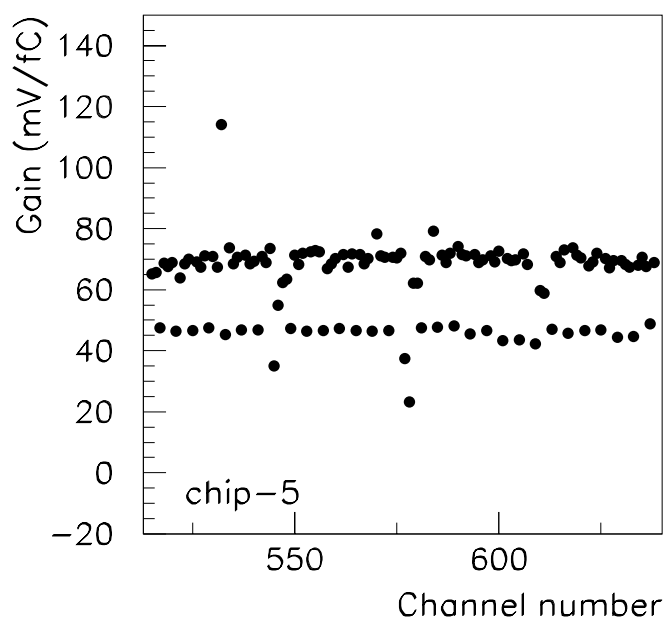
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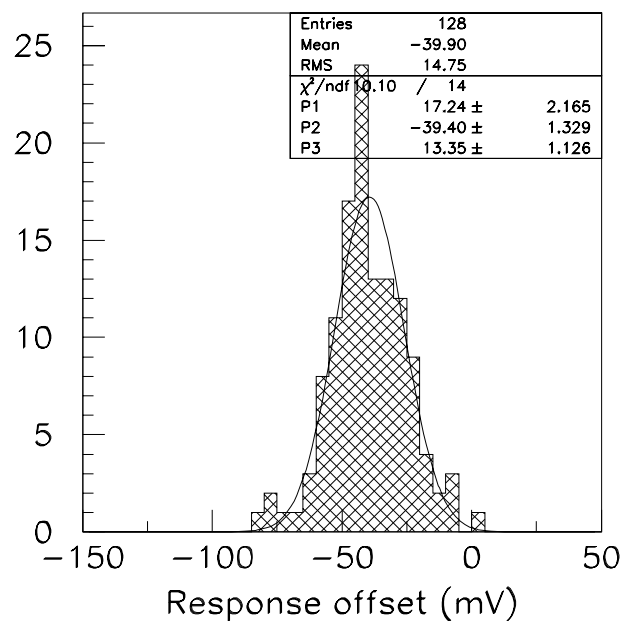
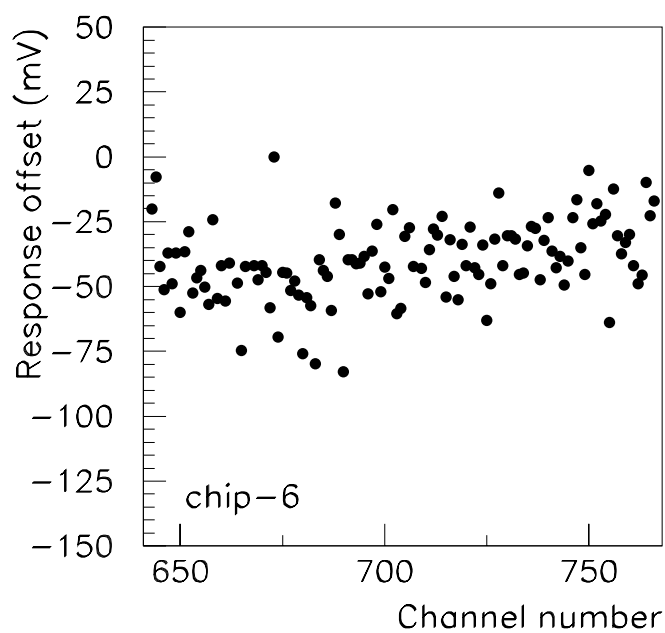
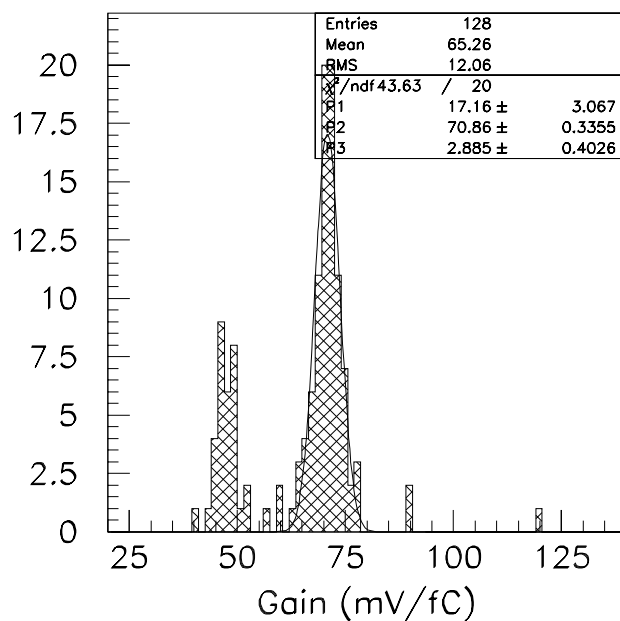
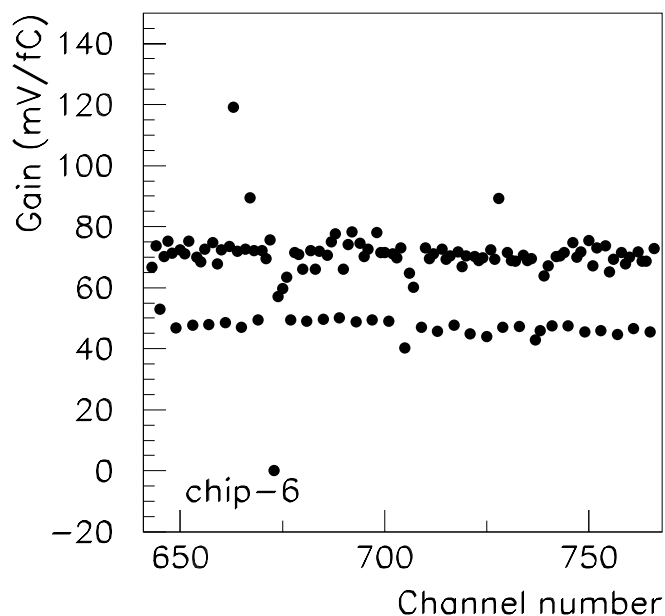
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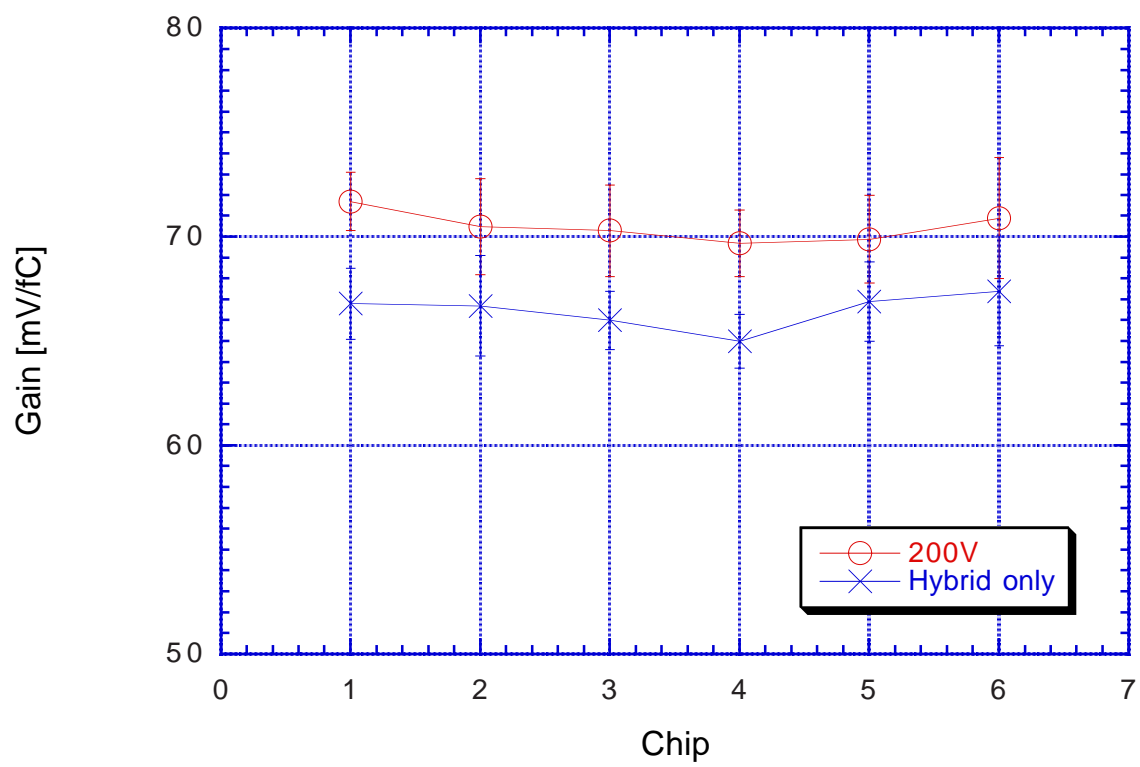


Fullmodule Bias 200(V)(FEbias 73.6(μ A))



Fullmodule Bias 200(V)(FEbias 73.6(μ A))





Summary

- **n-ABCD chips were successfully readout in the ABCD Kapton hybrids**
- **A 6 chips and a fully loaded 12 chips were fabricated into modules**
- **Noise, Gain, and Offset were evaluated with Charge injection scan with the internal DAC**
- **Lo-regime of the FE bias current, 73.6 μ A, was the least noisy operation point, which also seemed to work with the detectors connected (6 cm, 12 cm), although the gain might be more non-linear**
- **Gain seemed reasonably uniform (preliminary!)**
- **Two possible defect patterns were observed: (1) Quantized efficiency saturation, and (2) Low gain (could be larger offset) in every 4th channels**