SCTA - A Rad-Hard BiCMOS Analogue Readout ASIC for the ATLAS Semiconductor Tracker

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Abstract

Two prototype chips for the analogue readout of silicon strip detectors in the ATLAS Semiconductor Tracker (SCT) have been designed and manufactured, in 32 channel and 128 channel versions, using the radiation hard BiCMOS DMILL process. The SCTA chip comprises three basic blocks: front-end amplifier, analogue pipeline and output multiplexer. The front-end circuit is a fast transresistance amplifier followed by an integrator, providing fast shaping with a peaking time of 25 ns, and an output buffer. The front end output values are sampled at 40 MHz rate and stored in a 112-cell deep analogue pipeline. The delay between the write pointer and trigger pointer is tunable between 2 μs and 2.5 μs. The chip has been tested successfully and subsequently irradiated up to 10 Mrad. Full functionality of all blocks of the chip has been achieved at a clock frequency of 40 MHz both before and after irradiation. Noise figures of ENC = 720 e^- + 33 e^-/pF before irradiation and 840 e^- + 33 e^-/pF after irradiation have been obtained.

I. INTRODUCTION

The readout of silicon tracker systems for the LHC experiments requires high density multichannel mixed signal ASICs combining several analogue processing functions with high speed digital circuits. The analogue readout of tracker systems with several millions of channels requires the use of low power design techniques such as the analogue memory CMOS circuit which locally store analogue signals during the level 1 trigger latency [1], [2], [3], [4], [5], [6]. The analogue memory technique performs simultaneous read and write operations enabling detector readout without dead time. We present here an approach based on the same architecture principle as developed before, but the analogue front end has been designed with bipolar devices available in the DMILL technology [7]. The DMILL technology offers an excellent radiation hardness performance [8], [9] for a wide variety of devices: MOS transistors, fast bipolar *npn* transistors, junction field effect transistors and high value resistors with low stray capacitance. It is therefore suitable for mixed signal chip architectures and offers a unique possibility to integrate fast low noise analogue circuits and digital functions on a single chip.

In the DMILL technology we have at our disposal all three types of transistors, JFET, MOSFET and BJT, which can be used as input devices. The *npn* bipolar transistor offers the highest g_m/I_c ratio and the lowest input capacitance. For this reason, the *npn* bipolar transistor is intrinsically the best input device for a low noise preamplifier when the series noise contribution dominates. This is a particularly relevant issue for silicon strip trackers at the LHC with a typical strip capacitance of 20 pF and signals with a peaking time of 25 ns in the front-end signal processor.

For comparison of the noise performance between front-end systems with the bipolar and the MOS transistor we assume triangular shaping offering an effective noise suppression for both series and parallel noise sources. For a readout system using a bipolar input device biased with collector current I_c the equivalent noise charge (ENC) is given as

$$ENC = \sqrt{\frac{4kT\left(r_{bb} + \frac{kT}{2qI_c}\right)\left(C_a + C_d\right)^2}{T_p} + \frac{2qI_cT_p}{3\beta}} \qquad (1)$$

where r_{bb} is the base spread resistance and β is the current gain factor of the input transistor, C_a is the amplifier input capacitance, typically below 0.5 pF, C_d is the detector capacitance and T_p is the peaking time of the filter. The parallel noise contribution from the feedback resistor is ignored here since for an optimized preamplifier this contribution is negligible.

For a given peaking time, detector capacitance and current gain factor one can find an optimum value of the collector current which gives the minimum noise. Degradation of the β factor due to radiation damage of the bipolar transistors should be taken into account as this will result in some degradation of noise and a different optimum value of the collector current. The contour plot of constant ENC as a function of the collector current and β factor is shown in fig. 1.

The plot shown in fig. 1. indicates that a noise below 1200 e^- rms can be obtained for a detector capacitance of 20 pF and a relatively low collector current, about 200 μA. A degradation of β, even down to 50 as expected for DMILL transistors irradiated up to 2×10^{14} p/cm^2, causes only a minor increase in noise (up to 1300 e^- rms). Accepting this increased noise one can then use the transistor with a lower collector current, about 150 μA. The low value of the optimum collector current matches the low power requirements of the Atlas Semiconductor Tracker readout very well.

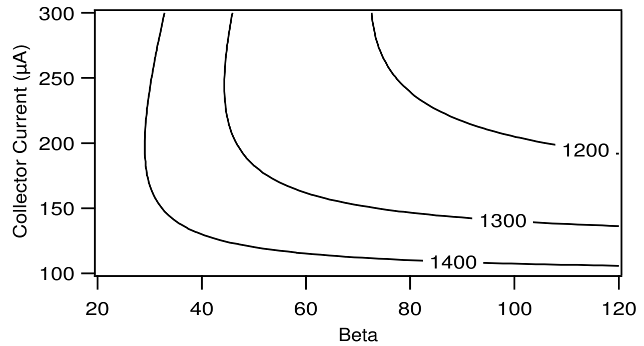

Figure 1: Constant noise contours for a bipolar input transistor and ideal triangular shaping of 25 ns peaking time. Base spread resistance of 50 Ω and detector capacitance of 20 pF is assumed.

For a MOS input device and triangular shaping the equivalent noise charge is given as

$$ENC = \sqrt{\frac{4kT\frac{2\Gamma}{3g_m}\left(C_a + C_d\right)^2}{T_p}} \qquad (2)$$

where g_m is the transconductance, Γ is the excess noise factor and C_a is the input capacitance of the input MOS transistor. Compared with a bipolar transistor the amplifier input capacitance is not negligible since a large Width/Length ratio (W/L) for the input transistor is required to give a high transconductance. Given a minimum length allowed by the technology and short channel effect a large W/L can be obtained by increasing the width and so the total gate area. For a comparison of the noise vs power figure of merit, it is important to notice that transconductance is proportional to collector current in a bipolar transistor while for a MOS transistor it is proportional only to the square root of the drain current. Thus for a given detector capacitance and shaping time there are two parameters, the width of the input transistor and the drain current which should be optimized in a system using MOS input transistors.

The constant ENC contour plot for typical parameters of a PMOS transistor in a submicron technology is shown in fig.2.

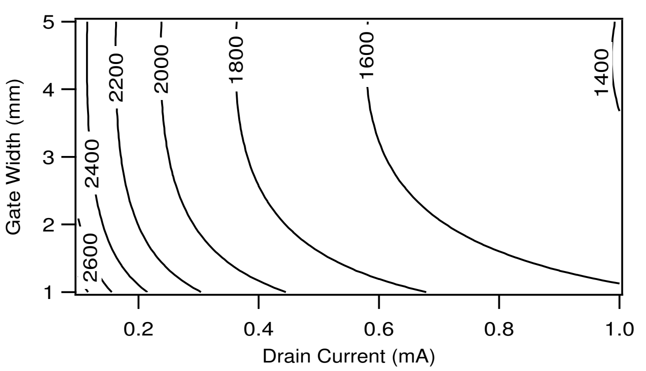

Figure 2: Constant noise contours for a PMOS input transistor, ideal triangular shaping of 25 ns peaking time and a detector capacitance of 20 pF. Minimum gate length of 1.5 µm, gate capacitance of 1.5 fF/µm^2 and Γ factor of 1.5 has been assumed.

The contour plot shows that an ENC of 1800 e^- rms is achieved for a drain current of 400 µA and a gate width ranging from 2000 µm to 4000 µm. This result indicates that with a bias current twice as high in the MOS device, the minimum achievable noise is still 60% more than for a bipolar device. The lower series noise factor, 1/2 for a bipolar device compare to 1 for a p-channel MOS, and the lower input capacitance, 0.5 pF for a bipolar device and 5 pF for a large p-channel MOS input device explain this significant difference in noise performance.

In addition, radiation damage increases the series noise factor of the MOS transistor whereas bipolar series noise is unchanged. The additional parallel noise caused by the beta drop of an NPN device in the DMILL process, typically 100 to 60 after 2×10^{14}protons/cm^2, is not significant when compared to the detector shot noise after irradiation.

The measurements of ENC versus C_d for a bipolar transistor as shown later in sect. IV indicate that the contributions from parallel and series noise add almost linearly. This indicates that the two noise sources in a bipolar transistor are significantly correlated for high frequencies. For a relatively large detector capacitance, about 20 pF, this effect does not play a major role since the total noise is dominated by the series noise.

II. CHIP ARCHITECTURE

Fig. 3 shows the block diagram of the SCTA chip architecture which has been designed in two versions, 32 channels and 128 channels. The chip comprises four basic blocks: front-end amplifier, analogue pipeline, control logic including a derandomizing FIFO, and an output multiplexer. The front-end circuit is a fast transresistance amplifier followed by an integrator, providing a semi-gaussian shaping with a peaking time of 25 ns, and an output buffer. The peak values are sampled at 40 MHz rate and stored in the 112-cell deep analogue pipeline. The mean amplitude obtained for a 1 MIP input signal is about 100 mV. It is sufficiently high that analogue signal processing after the front end does not contribute significantly to the overall noise figure.

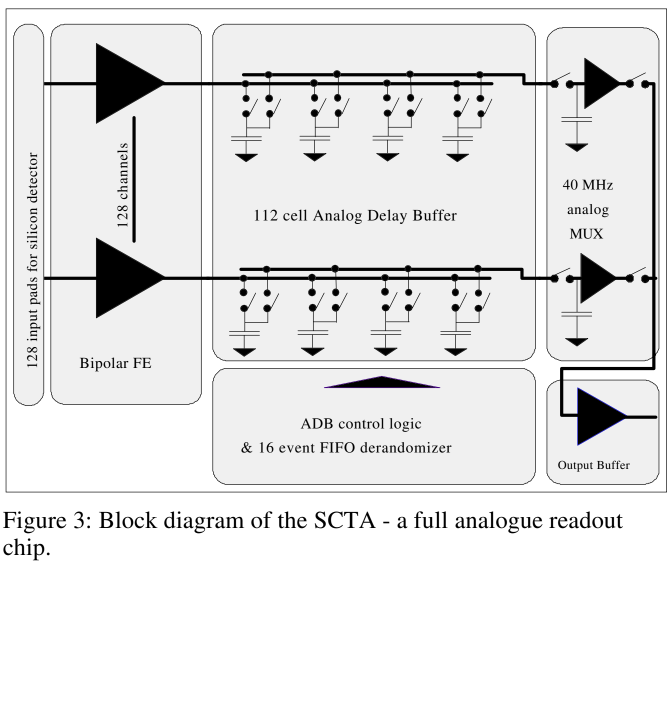

Figure 3: Block diagram of the SCTA - a full analogue readout chip.

A. BiCMOS preamplifier Shaper

The front-end circuit is based on a transresistance amplifier with a bipolar input transistor for the reasons presented in sec. I. The schematic diagram of the preamplifier-shaper circuit is shown in fig. 4. The input stage designed as a BiCMOS transimpedance amplifier is followed

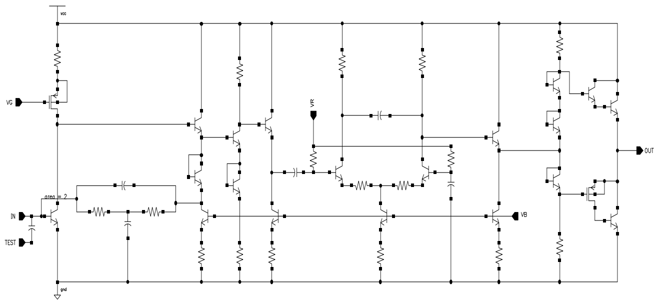

Figure 4: Schematic diagram of the front-end circuit implemented in the SCT128A chip.

by a single gain stage and an integrator providing the proper peaking time. The output stage is designed as a class AB amplifier and provides sufficient capability to drive the analogue pipeline at a relatively low quiescent current of 100 μA, so no extra write amplifier is needed in front of the analogue pipeline.

The transresistance preamplifier is built around a single ended NPN feedback pair circuit configuration which offers a low noise characteristic associated with a sufficient gain-bandwidth product. A phase margin of about 70° is achieved by a compensation network associated with the feedback resistor. The load of the input device is built with a p-channel MOS degenerated current source which offers a low output conductance and parasitic capacitance.

B. Analogue memory

The SCT128A memory samples the analogue signal voltage from the front end every 25 ns into a storage capacitor of 310 fF. The system performs a very simple and reliable voltage sampling. The readout need only retrieve the sample belonging to the peak of the pulse to recover the full time and amplitude information. Once the trigger signal arrives, the analogue values from the pointed physical address of the 128-channel memory column are read out via the output multiplexer. The delay between the write pointer and trigger pointer is tunable between 2 μs and 2.5 μs in the present version of the circuit.

C. Control logic of the analogue memory

Refering to fig. 5. the pipeline control of the memory allocation is done by two registers clocked at 40 Mhz, the Write column Register WR and the Trigger column Register TR, and one buffer, the Unused column Buffer UB. Register pointers have a delay between them such that the TR pointer passes memory cells later than the WR pointer by a delay equal to the trigger latency. The WR pointer controls writing of data into unused columns. The TR pointer sets a flag in the UB buffer at the request of an external trigger signal. The UB buffer thus holds flags to memory columns belonging to successive triggers. Because the readout time is generally longer than the loop pointer time, WR and TR pointers skip over columns where flags are set in the UB buffer. Each time a trigger generates a flag in the UB buffer, the Address Encoder generates the 7-bit binary address of the column. The encoded words are stored in the Read Address FIFO. Once a read signal is received, the first available address in the FIFO is decoded through the Address Decoder, enabling the readout of the column. The decoding of this address is used to free the corresponding flag in the UB buffer.

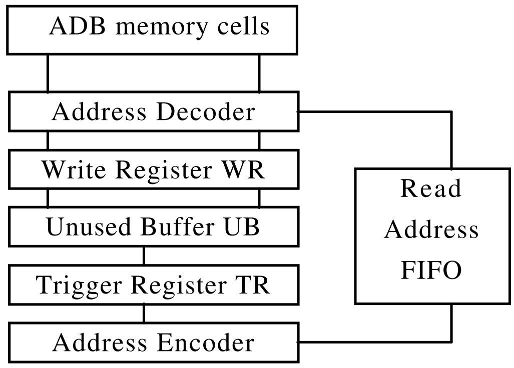

Figure 5: Block diagram of the memory control logic.

D. Analogue Multiplexer

The multiplexer chip contains 128 channels with sample-and-hold circuits and the output buffer. Each channel consists of an input switch, a storage capacitor and a sample-and-hold buffer designed as a source follower based on an NMOS transistor biased with 50 μA. In the readout phase this current is increased in the readout channel up to 600 μA which is sufficient to drive the parasitic capacitance of the internal bus line of the multiplexer. To provide a driving capability for 40 MHz operation of the chip placed on the final hybrid when the load capacitance is in the range of 60 pF, an additional output stage was necessary. A PMOS source follower biased with 5 mA current has been employed as an output buffer. The multiplexing function is implemented as a simple array of 128 NMOS switches controlled by a shift register. The 32-channel SCTA version has a moderate speed multiplexer working up to 10 MHz.

III. CHIP LAYOUT

The two versions, 32 channels and 128 channels, have essentially the same floor planning. Fig. 6 shows a photo of the 128 channel version, SCT128A. The front-end channels and the analogue pipeline are laid out with a pitch of 50 μm. The BiCMOS circuitry implemented in the front-end results in a very compact layout so that the front-end channel is only 800 μm long. The input bonding pads are laid out with 50 μm pitch. The die size is $9.3\times6.9\text{mm}^2$.

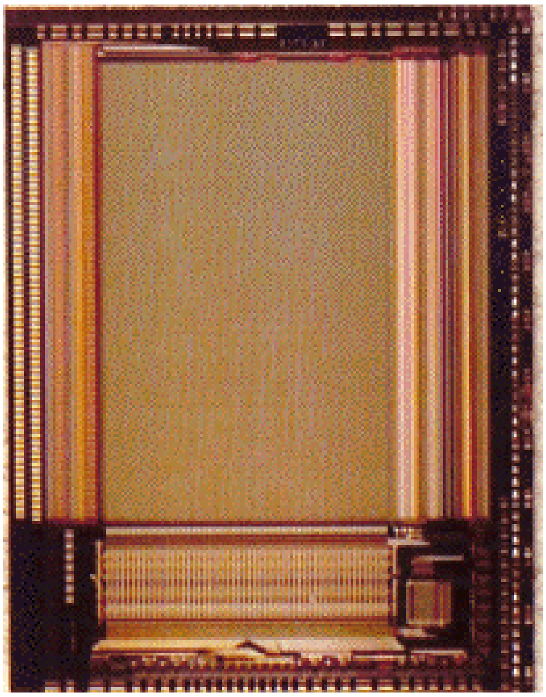

Figure 6: Photo of the SCT128A chip implemented in the DMILL BiCMOS process

IV. Experimental results and performances

A. Output Signal

The response of the full chain to a 4 fC (≈1 MIP) charge impulse was measured by injecting a known voltage step across an on-chip calibration capacitor at the input. The pulse shape was traced by varying the time of the injected pulse with respect to the readout time so that a different time slice of the pulse is readout for each delay. The result is shown in fig. 7, whence it can be seen that the peaking time is indeed 25 ns, including the loading effect of a 6 cm strip detector bonded at the input.

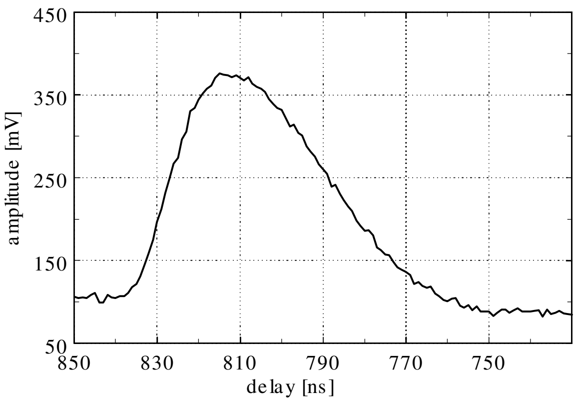

Figure 7: Output signal traced through the full processing chain, demonstrating the 25 ns peaking time. The injected charge was 4 fC and an additional external gain of 2.6 was applied.

B. Noise performance

Noise measurements have been performed for the front-end circuit alone and for the full chip operating at a clock frequency of 40 MHz. For the front-end amplifiers alone, a noise figure of ENC = 620 e^- + 33 e^-/pF has been obtained before irradiation and ENC = 840 e^- + 33 e^-/pF after 12 Mrad of gamma irradiation for a collector current of 220 µA in the input transistor. Measuring the noise through the complete readout chain, including the pipeline clocked at 40 MHz and the multiplexer, a figure of 720 e^- was obtained for zero input capacitance. The noise was measured by randomly reading the cells of the pipeline so the measured value includes cell-to-cell variations in the pipeline. Comparing the results of the measurements with and without the pipeline, we obtain a cell-to-cell amplitude variation of about 1 mV rms, to be compared with 100 mV signal amplitude for 1 MIP input.

The results indicate that additional sources of fluctuations, i.e. the pick-up of digital noise and the non-uniformity of pipeline storage cells, add only a marginal contribution to the noise of the front-end amplifier. For detector capacitances of the order of 20 pF, as foreseen for the ATLAS Semiconductor Tracker, we do not expect any significant contribution from these additional noise sources.

The results of various noise measurements are shown in fig. 8. The noise figure obtained for the chip connected to a 6 cm long strip detector is consistent with other measurements performed with discrete capacitors connected to the input.

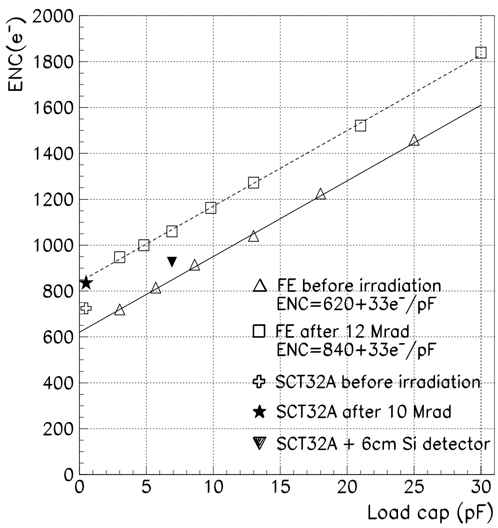

Figure 8: Summary of noise measurement performed for the BICMOS front-end alone, or with the full chip running.

C. Detector readout with ^{106}Ru beta source

The chip was bonded to a 6 cm long 280 µm thick n type detector with n^+ strips at 112 µm readout pitch with one intermediate strip to optimize charge sharing. The strips were isolated by individual p^+ implanted boxes. The detector was biased to 140 V and a scintillator trigger was used to initiate the readout control sequence of the SCTA. In order to ensure only the peak of the pulses was read, an 8 ns time window was defined in phase with the 40 MHz clock and used as a veto against all events falling outside of this time. A ^{106}Ru beta source was placed above the detector and the multiplexed data read into a digital oscilloscope and stored for further analysis. The histogrammed result of cluster signal/noise is shown in fig. 9.

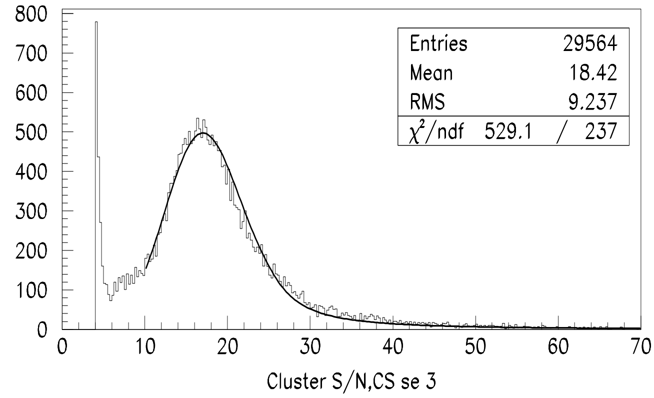

Figure 9: Histogram of data taken with a detector and a beta source, showing Landau peak at signal/noise = 18

V. RADIATION HARDNESS CHARACTERISTICS

A. NPN Bipolar device

Two critical issues determine the noise performance and radiation hardness of bipolar transistors, i.e. the base spread resistance and the degradation of β with irradiation. Radiation tests performed on individual bipolar transistors manufactured in the DMILL technology showed a similar behavior for β to that observed in other bipolar technologies [3,4], i.e. for lower current density a larger degradation of β is observed.

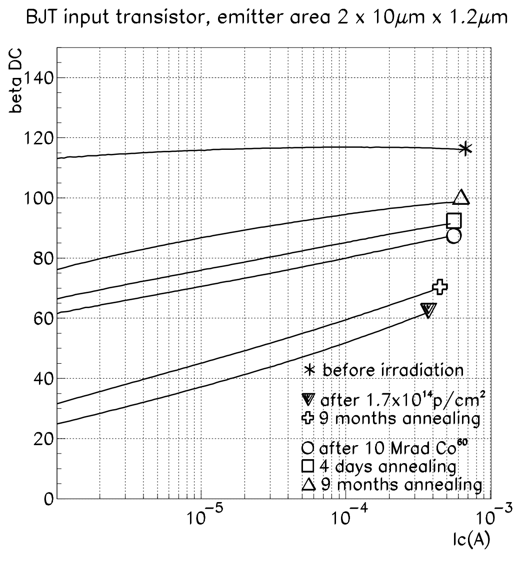

Figure 10: Degradation of the current gain factor β for the transistor geometry used for the input device.

The size of the input transistor has to be optimized taking into account the series voltage noise contribution from base spread resistance and parallel noise due to shot noise of the base current. The latter will increase after irradiation since a constant collector current should be maintained to keep the voltage noise low.

Transistors of different emitter areas from 1.2 x 1.2 μm^2 up to 2 x 1.2 x 10 μm^2 have been tested. For all types of transistors the base spread resistance has been evaluated from the noise measurements. Based on the radiation test results of individual transistors we have chosen a geometry for the input device which provides a relatively low value (of the order of 100 Ω) of the base spread resistance and reasonably high current density. The degradation of β for the transistor geometry as used in the input stage after different radiation tests is shown in fig. 10. For a nominal collector current in the input transistor of 200 μA the β is expected to be above 60 after irradiation to the maximum doses expected in the ATLAS SCT. Using the above value of current in the input stage the total power dissipation of the front-end circuit, including the output buffer, is below 1.2 mW/channel.

VI. CONCLUSIONS

A 32 channel and a 128 channel version of a radiation hard analogue front end chip intended for the readout of trackers have been succesfully demonstrated to give adequate noise performance with load capacitances expected from strip detectors in the LHC experiments. In particular, full functionality has been shown at 40 MHz both before irradiation and after 10 Mrad dose, keeping power dissipation within acceptable limits and with little degradation of the noise.

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