Digital Tests

Performed on ABCD1

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1. Introduction

The initial evaluation of the ABCD chip show a complete digital functionality according to specifications, except the following point:

1. No trailer if chip is set as “END”, if “datain” input is left open or set to one.
2. The Calibration pulse generation does not work with odd delay values and not with the proper pulse polarity.

Several modules for the SCT detector have been fabricated with 6 ABCD chips connected as proposed for the SCT module readout (one chip in MASTER mode, 4 daisy chain chips, one chip in END mode) and show generally no systematic functional failure, except the two items reported above.

The corrections for item 1 and 2 as well as design improvements are discussed in the document “Functional Improvements for ABCD2”.

To get an exact figure of the functional margins of the digital functions, some ABCD chips (first version, Batch 1 and Batch 2) have been tested with the CERN Microelectronics IMS ATS Tester. The tests are performed on a single chip mounted on a socket card attached to the tester box. The tester provides accurate time and voltages. It was possible to evaluate successively the limits of functionality for all the digital functions with respect to clock frequency and/or power supply value.

2. ATS Tests Description

The text below identifies the 8 tests sequences applied successively to the DUT.
Each test is the result of a procedure in which a stimulus description to activate the functions of the chip is associated with the resulting output patterns from the Verilog simulation. This information is dumped to the tester, which directly applies the stimuli to the DUT and compares the expected patterns (from simulation) to the real data out of the chip.

ABCD tests on the IMS Tester - description.

1. SendId mode.
   1.1. Loading configuration register with different values. Checking chip address decoding.
   Tester files: ts_a.set, ts_xa.set, ts1_a.set, ts1_xa.set.
   Test number: 1.

   1.2. BC reset tests.
   In this test the *BC Counter Reset* slow command is send followed by *L1 Trigger* comand delayed from 0 to 80 clock cycles.
   Tester files: bc_80.set.
   Test number: 2.

2. Data Taking Mode - first sequence.
   Input from Mask Register, Accumulator disabled, DCL mode = hit (00).

   2.1. No data tests.
   The Mask Register is loaded with 000... and then from 0 to 27 L1 triggers are sent.
   Tester files: ta_00a.set, ta_00xa.set.
   Test number: 3.

   2.1.1. No data readouts

   2.1.2. Overflow.

   2.1.3. Error.

   2.2. Single channel test.
   A single bit is set in the Mask Register, then from 0 to 27 consecutive L1 triggers are sent.
   Tester files: ts_01a.set, ts_01xa.set.
   Test number: 4.

   2.2.1. First channel hit.

   2.2.2. Last channel hit.

   2.2.3. Some random single channel readouts.

   2.2.4. Overflow.

   2.2.5. Error.

   2.3. Multiple channel tests.
   Test number: 5.

   2.3.1. 128 channels hit. First-last channels hits (2x1-5 channels).
   Tester files: ts_020a.set, ts_020xa.set.

   2.3.2. Random: L1 (up to 25), pattern.
   Tester files: ts_021a.set, ts_021xa.set.

   The result for the test number 5 is the worst_case(2.3.1, 2.3.2).

3. Data Taking Mode - second sequence.

3.1. Accumulator and Mask Register tests.
Masked Input Register pulse used for accumulator testing.
Tester files: ta_10a.set, ta_10xa.set.
Test number: 6.

3.1.1. No hit Accumulator test.

3.1.2. All hit Accumulator test.

3.1.3. Accumulator test - pulsing Input Register with several masks.

3.2. All DCL modes test.
Accumulator off. Pulsing Input Register with random masks. Trigger delay scanning.
Tester files: ta_11a.set, ta_11xa.set.
Test number: 7. .

3.3. Pipeline scan.
Pulsing all channels with Input Register. Trigger delay scaning from 0 to 11 clock cycles.
This test should give the worst speed results for ABCD batch 2 chips.
Tester files: pi_scan_a.set, pi_scan_xa.set.
Test number: 8.

Remark: all the tester file names are built in the same way; e.g:
ts_a - full output comparison, selected command and clock lines number 0;
ts1_a - full output comparison, selected command and clock lines number 1;
ts_xa - counters not compared, selected command and clock lines number 0;
ts1_xa - counters not compared, selected command and clock lines number 1.

3. ATS Tests Results

Table 1 shows limits of functionnality with clock frequency (4V, Ambient temperature) for several chips from the batch 1.

Table 2 shows limits of functionnality with clock frequency (4V, Ambient temperature) for several chips from different wafers from the batch 2.

Test No	Chip #2		Chip#4		Chip #11		Chip #12		Chip #14		Chip #15		Chip #16	
	A	B	A	B	A	B	A	B	A	B	A	B	A	B
1.	62.5	47.6	66.7	50.0	62.5	50.0	60.6	58.0	80.0	52.6	65.6	48.2	66.7	28.0
2.	x	47.6	x	52.6	x	50.0	x	53.0	x	52.6	x	54.1	x	NP
3.	58.8	45.4	62.5	50.0	56.7	50.0	58.8	53.0	60.6	NP	65.6	NP	60.6	x
4.	50.0	47.6	58.8	50.0	51.6	51.0	52.6	53.3	52.6	NP	55.6	x	54.8	x
5.	58.8	47.6	58.8	47.6	52.9	50.0	55.6	50.0	52.6	NP	55.6	x	54.8	x
6.	58.8	47.6	52.6	50.0	55.6	53.0	59.7	53.0	NP	NP	61.5	x	NP	x
7.	34.5	34.5	45.4	45.4	47.6	46.0	47.1	32.0	50.0	40.0	42.1	x	54.8	x

Table 1 : Speed limit tests results on digital blocks for ABCD, 1st batch. A = no test of Counters. B = incl. Counter test.

TestNo	#7-15		#7-16		#4-3		#4-4		#4-5		#4-6		#4-18	
	NoCount	Full	NoCount	Full	NoCount	Full	NoCount	Full	NoCount	Full	NoCount	Full	NoCount	Full
1	74.1	63.5	75.5	65.6	68.4	65.6	76.9	65.6	74.8	64.0	77.7	65.6	78.4	65.6
2	x	63.5	x	65.6	x	64.0	x	64.0	x	65.6	x	65.6	x	65.6
3	63.5	63.5	66.7	65.6	64.5	65.0	52.6	64.5	64.5	64.0	65.0	64.5	69.6	66.7
4	51.9	51.9	52.6	52.6	53.0	52.5	52.6	52.3	53.3	53.3	52.3	51.9	54.4	54.1
5	51.3	51.9	51.9	52.6	53.0	52.3	NP	NP	53.7	53.3	51.9	52.6	54.1	54.1
6	57.1	58.0	62.0	57.1	69.6	57.6	71.4	58.0	73.4	63.5	72.1	57.6	74.8	58.4
7	35.7	35.7	36.4	36.4	36.4	36.4	35.1	35.7	35.1	34.8	35.1	35.1	38.1	37.7
8	33.9	33.9	31.2	31.2	33.6	33.6	NP	NP	33.6	33.6	33.9	33.9	35.1	35.1

Dead: #4-9

TestNo	#6-16		#6-17		#5-11	
	NoCount	Full	NoCount	Full	NoCount	Full
1	77.7/76.9	67.2/65.6	76.2/76.2	63.5/63.0	74.1/73.4	64.0/63.5
2	x	65.6/65.6	x	63.0/63.0	x	63.5/63.5
3	66.1/65.6	66.1/65.0	67.2/66.7	63.0/63.0	NP	NP
4	53.0/52.6	53.0/52.6	53.3/53.3	53.7/53.3	NP	NP
5	52.6/52.6	53.0/52.6	53.3/53.0	53.3/53.3	NP	NP
6	72.7/72.7	58.4/58.0	73.4/73.4	58.0/58.0	NP	NP
7	35.4/35.1	35.4/35.1	36.4/36.4	36.4/36.4	35.1/34.8	35.1/34.8
8	33.6/33.3	33.6/33.3	34.8/34.5	35.1/34.5	NP	NP

Dead #5-4

Remark: first number shows the frequency when there is no error after 30 sec, second shows the same after 60 sec.
In the second table NP means that even at 200 kHz and 5 V there were errors.

Table 2 : Speed limit tests results on digital blocks for ABCD, 2nd batch. #7-15 means Wafer 7, chip number 15. NoCount = no test of Counters. Full = incl. Counter test

3. Tests Analysis

The tests on chips from Batch1 show functionality for all blocks above 40Mhz. But two limitations are visible :

- There is a visible speed margin loss when the counters values are checked (L1 and BC counts are part of the header information provided by the chip set in "MASTER" mode).
- Test number 8 show limits close to 40Mhz.

The tests on chips from Batch 2 show a slightly different behavior :

- The speed loss with counter test is less important
- Tests number 7 and 8 show limitations which concern the pipeline data transfer.

Corrections are proposed for solving these two limitations for the new version of ABCD.

The document "ROC FIFO CORRECTION" describes the correction done for the counters speed limitation.

The document "THE PIPELINE" describes the correction done for the pipeline speed limitation.

The other ATS test results show quasi uniform speed limits across different functions.

3. Irradiation

Two chips from the 2nd batch have been irradiated with a X-ray source up to the equivalent of 10Mrads (env. 200rads/sec). Table 3 show the speed limits of the digital functional blocks after 5Mrads and 10Mrads.

Before irradiations :

CHIP #6-16

TestNo	Max speed @ 4V NoCount	Full	Min VDD @ 40MHZ NoCount	Full
1	77.7/76.9	67.2/65.6	3.30	3.30
2	x	65.6/65.6	x	3.30
3	66.1/65.6	66.1/65.0	3.30	3.30
4	53.0/52.6	53.0/52.6	3.30	3.30
5	52.6/52.6	53.0/52.6	3.30	3.30
6	72.7/72.7	58.4/58.0	3.30	3.30
7	35.4/35.1	35.4/35.1	4.25	4.25
8	33.6/33.3	33.6/33.3	4.425	4.425

CHIP #6-17

TestNo	Max speed @ 4V NoCount	Full	Min VDD @ 40MHZ NoCount	Full
1	76.2/76.2	63.5/63.0	3.325	3.325
2	x	63.0/63.0	x	3.325
3	67.2/66.7	63.0/63.0	3.325	3.325
4	53.3/53.3	53.7/53.3	3.325	3.325
5	53.3/53.0	53.3/53.3	3.325	3.325
6	73.4/73.4	58.0/58.0	3.325	3.325
7	36.4/36.4	36.4/36.4	4.20	4.20
8	34.8/34.5	35.1/34.5	4.325	4.325

AFTER IRRADIATIONS 5Mrads (Xray):

CHIP #6-16

TestNo	Max speed @ 4V NoCount	Full	Min VDD @ 40MHZ NoCount	Full
1	55.6	55.6	3.40	3.40
2	x	55.6	x	3.40
3	55.6	55.6	3.40	3.40
4	49.4	49.4	3.45	3.45
5	49.4	49.4	3.45	3.45
6	54.8	54.8	3.45	3.45
7	35.7	35.7	4.20	4.20
8	34.5	34.5	4.40	4.40

CHIP #6-17

TestNo	Max speed @ 4V NoCount	Full	Min VDD @ 40MHZ NoCount	Full
1	53,3	53.3	3.475	3.475
2	x	53.3	x	3.450
3	-	53.3	-	3.425
4	47.6	47.6	3.50	3.50
5	-	48.2	-	3.50
6	-	53.3	-	3.45
7	-	36.4	-	4.275
8	-	34.8	-	4.40

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10Mrads (Xray):

CHIP #6-16
TestNo  Max speed @ 4V              Min VDD @ 40MHZ

      NoCount     Full        NoCount     Full

1     48.8        48.8        3.50        3.50
2     x           48.8        x           3.50
3     48.8        48.8        3.50        3.50
4     -           45.5        -           3.65
5     -           45.5        -           3.65
6     -           48.8        -           3.50
7     -           32.3        -           4.62
8     -           30.8        -           4.75

CHIP #6-17
TestNo  Max speed @ 4V          Min VDD @ 40MHZ
      NoCount     Full        NoCount     Full

1     48.2        48.2        3.55        3.55
2     x           48.2        x           3.55
3     -           48.2        -           3.55
4     46.0        46.0        3.60        3.60
5     -           46.0        -           3.60
6     48.2        48.2        3.52        3.52
7     -           34.2        -           4.35
8     -           33.1        -           4.50


x = not relevant
- = not measured
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Table 3 : ATS tests results for two ABCD chips, 2nd batch, before irradiation, after 5 Mrads and 10 Mrads.

The irradiation tests show a speed limit degradation in the range of 11% at 5Mrads and 14 % at 10Mrads.