# ROC Fifo Correction

# Implemented in ABCD2T/NT (SCT Readout chip)

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# 1. Problem on version 1

The digital tests on the first version of the ABCD chips has shown a rapid loss of the L1 and BC counters information above 40 MHz. Some chips (2nd run) always fail on the tests of the counts, all of them fail the test at any frequency after 10Mrads irradiation. The detected failure is : the count values are zero for both L1 and BC counts.

# 2. Analysis of the problem

Eldo simulation of the logic circuit made of the counters, the FIFO memory which holds the counters data and the Readout Controller (ROC) was performed. Analysis shows that the most probable cause of failure is the loss of data when it is readout from the FIFO and latched into a parallel-to-serial register (PSC) within the ROC.
The ROC provides a sequence in which at one clock edge, a 25ns long READ signal is applied to the FIFO, at the next one a 25ns long PSC_LOAD signal allows the latching of the data in the PSC register.
The simulations outputs show that the delay for getting the data out of the FIFO can be longer than the delay between the READ signal and the clock edge used to latch the data into the PSC. The conditions in which the FIFO data latching is missed in simulations is VDD=3.5V, TEMP = 27 deg.C, slow-slow parameters, 25 ns clock period.
Before the data are established, the FIFO is in precharge mode, with outputs forced to zero. Thus when it fails, the PSC latches count 0 instead of the FIFO value. This corresponds to the failure observed with tests on the chip.
A description of the time sequence is given in figure 1.

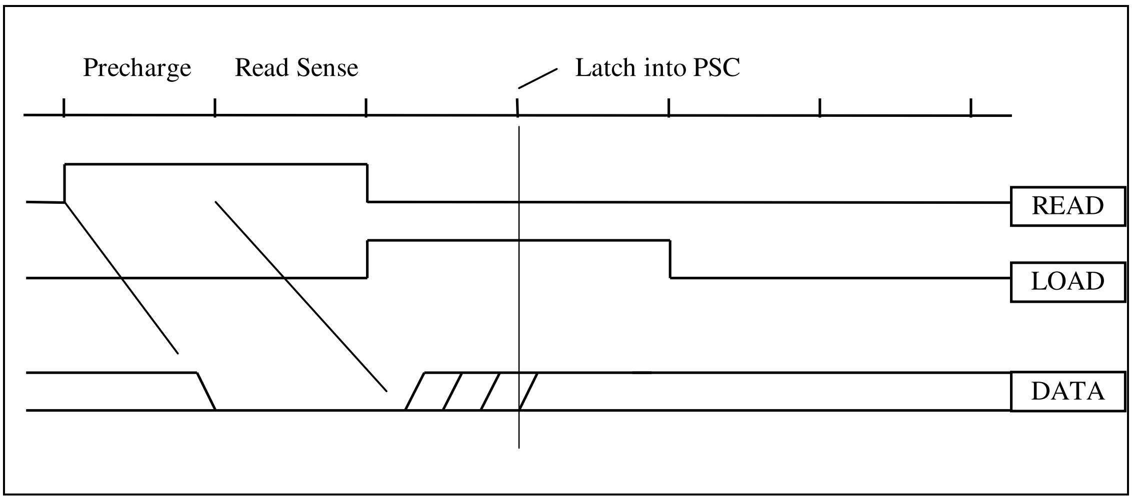


Fig. 1

## 3. Correction of the problem

The solution proposed is to adopt a new FIFO schema, in which the delay from READ signal to valid output is by construction shorter. With this option, the READ to PSC LOAD time interval does not need to be changed. The ROC controller can be kept the same as on the first ABCD version. Making a new sequence and rerouting of the ROC function was seen as having too much risk for this block which builds-up the output serial data stream. The new FIFO cell is a larger cell with an internal buffer transistor, thus allowing for a simple readout sense circuit. The cost in area of larger memory cells is fully compensated by the reduced complexity of the surrounding logic system. Furthermore, there is no clock needed and the data is directly available from the rising edge of the READ signal. There is almost one clock period less in the delay from READ edge to valid data.
The simulation performed with the new schema shows a full functionality of the circuit (counters, FIFO, ROC) in the following conditions:
VDD=3.7V, TEMP = 40 deg.C, irradiated slow-slow parameters, 17 ns clock period.

The new timing description is sketched in Figure 2.

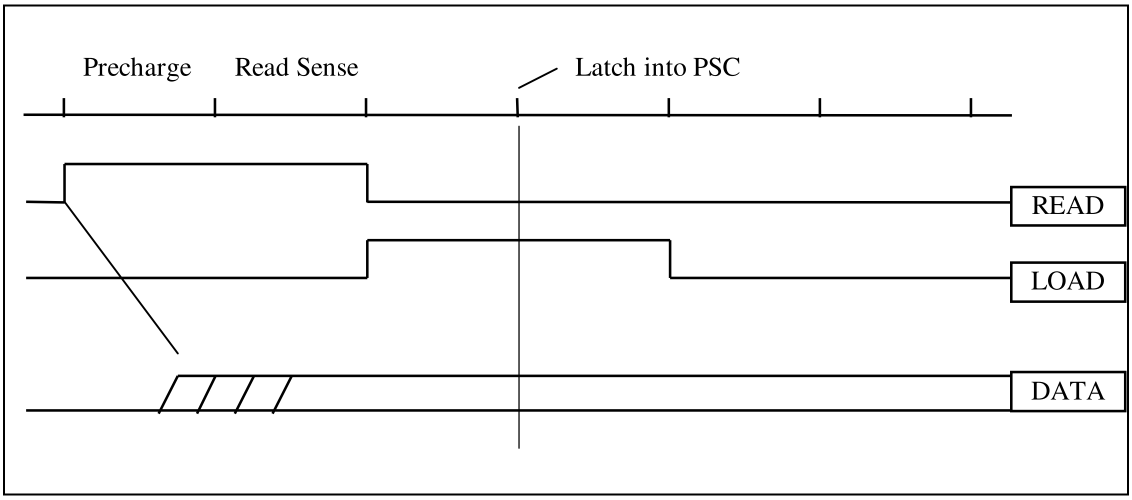


Fig. 2

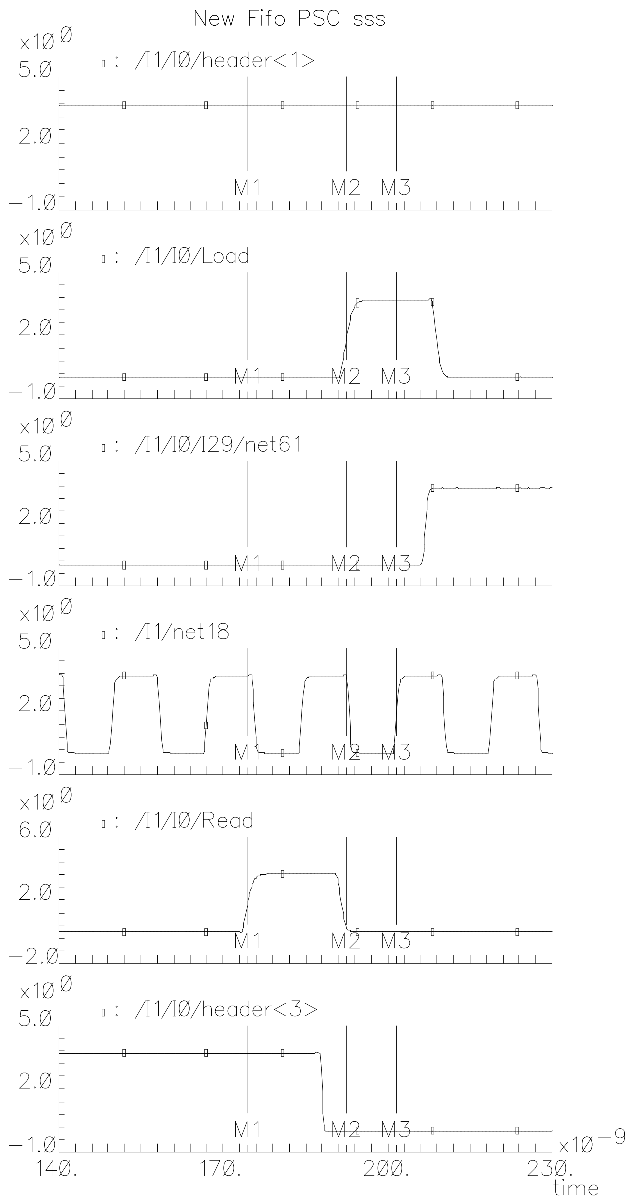


Fig. 2 : Traces out of the Counter/ROC system. From top, traces 2 and 5 show the respective positions of READ and LOAD (PSC) signals. Last trace is the output from the Fifo. It is settled 12 ns before the clock latches the data into the PSC register (M3 marker). Eldo simulation output, “iss” parameters, 40 deg.C, 3.7V, 17ns clock cycle.