Functional Improvement

for ABCD2T/NT
(SCT Readout chip)

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1. Description

Two functional errors are corrected for ABCD2 chip. They are :

1. No trailer if chip is set as “END”, if “datain” input is left open or set to one.
2. The Calibration pulse generation does not work with odd delay values and not with the proper pulse polarity.

Three items are changed :

1. “Select” input is changed from pull up to pull down drive
2. A L1 command issued after a BCReset command or a SoftReset command should produce the same BC count.
3. The Command Decoder instruction set is modified for ABCD2T (Trim DAC loading)

Apart of the front-end and DAC corrections, there are two digital functions improved for clock speed margins:

1. Pipeline data transfer. The document “THE PIPELINE” describes the correction done for the pipeline speed limitation.
2. Counter FIFO speed issue. The document “ROC FIFO CORRECTION” describes the correction done for the counters speed limitation.

2. Functional corrections

2.1. Missing Trailer

When the ABCD chip is set as “END” and has no connexion to its “datain” inputs, the unknown state on “datain” can corrupt the internal sequencing and the Trailer pattern is not sent out. The fix is to add a gate after the “datain” receivers to switch off “datain” logical value when the “END” bit from the configuration register is set.
The correction has been validated with Verilog simulation.

2.2. Calibration Pulse

The functional description of this block was wrong and led to an improper operation of the test pulse delay register. The result is that the delay register did not recognized the odd delay numbers, and, when set with even delay numbers, the pulse polarity was wrong (it was possible anyway to use the test pulse for calibration by using the pulse trailing edge instead of the leading edge). This has been fixed and verified with analog simulation.

3. Functional changes

3.1. Select Input

The “select” input has a pull down instead of a pull up in the ABCD2 version. This makes the defaults inputs for clock and command signals to be clk0/clk0B and com0/com0B.

3.2. BCReset stretch

It has been observed that a L1 command sent adjacent to a SoftReset command or to a BCReset command was producing two different BC counts (resp. 5 and3). This has been corrected by producing internal SoftReset and BCReset pulses of the same width (BCReset stretch to 3 clock periods). This change has been fully validated with Verilog simulation (BC count is 3 if L1 is issued adjacent to SofReset or BCReset).

3.3. Command Decoder for TRIM DAC

The command decoder has been modified (ABCD2T version only) to adopt a new instruction to load the TRIM DAC of the front-end channels. See the Specification for a description of the new command. This additional feature has been validated with Verilog. The full operations of the other commands have been checked as well. Still to be done is the verification with Eldo simulator and corner parameters of the technology.

4. Modifications Resume for ABCD2T/NT

Item	ABCD2T	ABCD2NT	Remarks
Front-end (b) update	yes		With TRIM DAC
Front-end (c) update		yes	No TRIM DAC
Trim DAC added	yes	no	
DAC update	yes	yes	Radhard version
Calibration Pulse update	yes	yes	Correct polarity
Input Register	yes	yes	Pipeline speed improvement
Pipeline	yes	yes	
Readout Buffer	yes	yes	
Command Decoder update	yes	no	ABCD2T : New instruction for TRIMDAC
ROC (Readout Controller) update	yes	yes	Counter&Fifo speed improvement BCReset stretch
ROL (Readout logic)	no update	no update	
Front Pad Ring update	yes	yes	Front Pad pitch at 48um
Back Pad Ring update	yes	yes	Missing Trailer correction Pull down on "select" input Passive components updated for DMILL4.3 cap & res parameters LVDS Receiver updated for DMILL4.3 corner parameters