LVDS Receiver

Implemented in ABCD2T/NT (SCT Readout chip)

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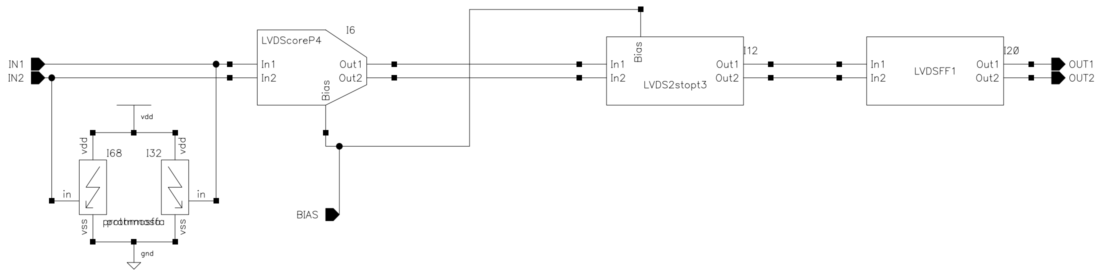
1. Specification

A "LVDS" type of input receiver has been developed for the Clock and Command input lines. The three main features of these inputs are:
. Differential, voltage sensing inputs, 100mV minimum swing, with very large Input Common Mode range, from 50mV to 2.35V (@ 4V VDD).
. 40MHz typical clock rate (Clock Inputs) or 25ns burst pulse regime (Command Inputs).

2. Description



Pin name	Function
IN1	LVDS negative input
IN2	LVDS positive input
OUT1	Output signal. This signal goes to the core of the chip.
OUT2	Output with inverted polarity.

The input stage (LVDScoreP) with a limited DC gain of 2~3, has outputs with DC levels almost insensitive to the Input Common Mode range.
The second stage (LVDS2stopt) provides sufficient gain to get full swing differential outputs.
The last stage (LVDSFF) creates sharp edges on the signal shape.

All these blocks have their bandwidth limitation near 200 MHz to provide sufficient speed margin. This avoids having DC operating points drifts when the inputs receive bursts of data (Command Inputs).

Figure 2 shows one of the two outputs after the three stages. The output is clearly seen almost independent of the VCM Input Common mode value.

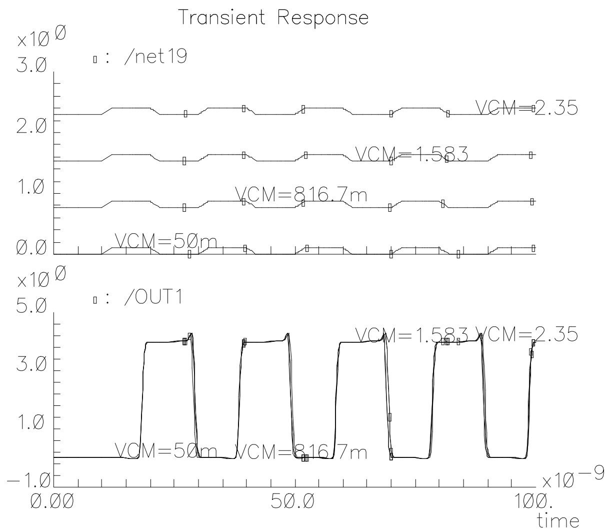


Fig. 2

3. Simulation outputs

A table of characteristics is shown below, from simulations using the DMILL 4.3 release corners parameters. "ff" corresponds to fast-fast process parameters, "tt" to typical parameters , "ss" to slow-slow parameters , "iss" to irradiated slow-slow parameters.

	Min.	Max.	Remarks
Differential Voltage (Vdm)	100mV	450mV	Full parametric range
Common Mode Input (Vcm)	Vdm/2	2.4V - Vdm/2	"ff" to "ss" parametric range, 0 to 40 C, 3.7-4.3V supply "iss" parameters, 0 to 40C, 3.8-4.3V
Power Supply	3.2 V		Vdm = 100mV, Vcm =1.5 V T = 27oC, tt
Differential Skew		+/-6ns	Vdm = 100mV, Vcm =1.5 V VDD = 4 T = 27oC, tt
Delay time (input to output)	5.50 ns (ff, 4.5V, VCM =2.35V)	14.60 ns (iss, 3.5V, VCM = 0.05V)	Vdm = 100mV