The Data Compression Logic

Implemented in ABCD2T/NT (SCT Readout chip)

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1. Specification

The Data Compression Logic reads three 128-bit words (time slices) from the Output Buffer. Then all the channels are scanned for data that compromise given compression criteria. The selected channels' addresses and hit data are sent to the output of the block on the request form Control Logic.

2. Description

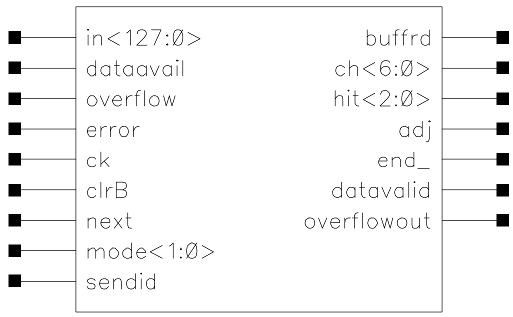

Figure. 1. The Data Compression Logic block symbol.

Pin name	Function
in<127:0>	Data input from Output Buffer
dataavail	Data available flag (*emptyB* in the Output Buffer)
overflow	Overflow flag (from the Output Buffer)
error	Error flag (from the Output Buffer)
ck	Clock signal input
clrB	Reset signal input
next	Next data request input (from the Readout Logic)
mode<1:0>	Data compression criterion (look into specification for details)
sendid	SendId mode flag (from the Configuration Register)
buffrd	Read signal for the Output Buffer
ch<6:0>	Channel address (for the Readout Logic)
hit<2:0>	Channel data (for the Readout Logic)
adj	Adjacent channel flag (for the Readout Logic)
end_	End flag (for the Readout Logic)
datavalid	Data valid flag (for the Readout Logic)
overflowout	Overflow flag (for the Readout Logic)

After receiving the data on L1 trigger command, the Output Buffer sets the *datavalid* input signal of the DCL active. The DCL, if it is not processing previous data, reads three 128-bit words from the Output Buffer and stores them into the internal register. Then, for each channel that compromises given compression criteria a flag is set. First four of the selected channels are loaded into the output buffer of the DCL. The data for the first channel arrives at the DCL output, and the *datavalid* signal is set active. If the next channel is the consecutive one (has an address by one higher from the current), the *adj* flag is set. For the last channel data the *end_* flag is set. For special conditions e.g. overflow or error information gained from the Output Buffer, the *overflowout* flag is set. When the chip is in the SendId mode no data is processed. However, the three words are read from the Output Buffer.

3. Modifications

No modification has been made in comparison to the previous ABCD design.

3. Simulation status

The following actions are planed:
- simulation of the DCL with Verilog, gate-level with old Verilog models (developed for the previous version of the DMILL design kit – MHS_v3.0).
- analogue simulation of the basic sub-blocks with Eldo and the current models;
- creating new Verilog models (with corner parameters);
- simulation of the DCL with the new Verilog models;