The Input Register

Implemented in ABCD2T/NT (SCT Readout chip)

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1. Specification

The Input Register reads the data from the Front-End. The data is synchronized with the clock, masked, and sent to the Pipeline. If the edge mode is enabled, the edge detection is preformed and for each hit only a single data bit is generated. In the test mode the contents of internal Mask Register is sent to the Pipeline instead of the Front-End data. For the testing purposes it is possible to set all the outputs high with the *Pulse* signal.

2. Description

Figure. 1. The Input Register symbol.

Pin name	Function
clk	Clock input.
mode	Test mode on/off.
sin	Serial input for the Mask Register.
load	Load signal for the Mask Register.
Pulse	Sets all the outputs high.
edgemode	Edge mode on/off.
i<127:0>	Inputs from the Front-End.
o<127:0>	Outputs for the Pipeline.
MASK<0>	Test output.

The Input Register contains the following sub-blocks:

- The Latch. The outputs from the Front-End are latched with the *clk* signal. When the edge mode is enabled, the zero suppression is performed.

- The Mask Register. This is the 128-bit register serially loaded.

- The Masking Logic. The output data for the Pipeline is chosen depending on the state of the *mode* signal. If the state of the *mode* signal is low the data from the Front-End is masked with the contents of the Mask Register and sent to the Pipeline. If the state is high, the content of the Mask Register is applied to the input of the Pipeline. In both cases all the outputs of the Input Register can be set high with the *Pulse* signal.

3. Modifications

The following modification have been made in comparison to the previous ABCD design:
- input clock for the latch clock has been inverted (following the solution of the "DCL" problem);
- a dflip-flop was added to synchronize the *pulse* input signal with the pipeline)

3. Simulation status

The following actions are planed:
- simulation of the Input Register with Verilog, gate-level with old Verilog models (developed for the previous version of the DMILL design kit – MHS_v3.0).
- analogue simulation of the basic sub-blocks with Eldo and the current models;
- creating new Verilog models (with corner parameters);
- simulation of the Input Register with the new Verilog models;
- analogue simulation of the Input Register to the Pipeline interface.