The Pipeline

Implemented in ABCD2T/NT (SCT Readout chip)

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1. Specification

The Pipeline is the 132 cell long dynamic delay buffer. It should store the data from the Input Register until the L1 is generated. The content of the Pipeline is not reset with the *clrb* signal.

2. Description

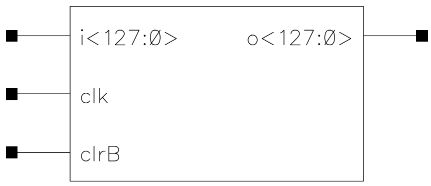

Figure 1. The Pipeline symbol.

Pin name	Function
clk	Clock input.
i<127:0>	Inputs from the Input Register
o<127:0>	Outputs for the Output Buffer
clrb	Reset signal for the clock generator.

The Pipeline consists of a Clock Generator and 128 channels. The Clock Generator outputs 12 non-overlapping clock signals. The basic pipeline cell is shown in figure 2.

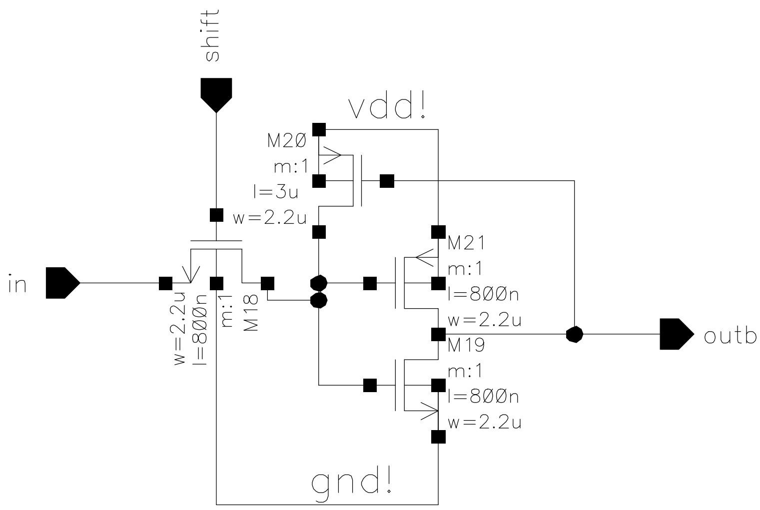

Figure 2. The basic Pipeline cell.

The memory cell is semi-dynamic: for “1” input data it is static (as the feedback transistor pulls the storing capacitance to Vdd, while “0” is kept with no refreshing.

Each Pipeline channels consist of twelve multiplexed sub-channels. The schematic of the single Pipeline channel is shown in figure 3.

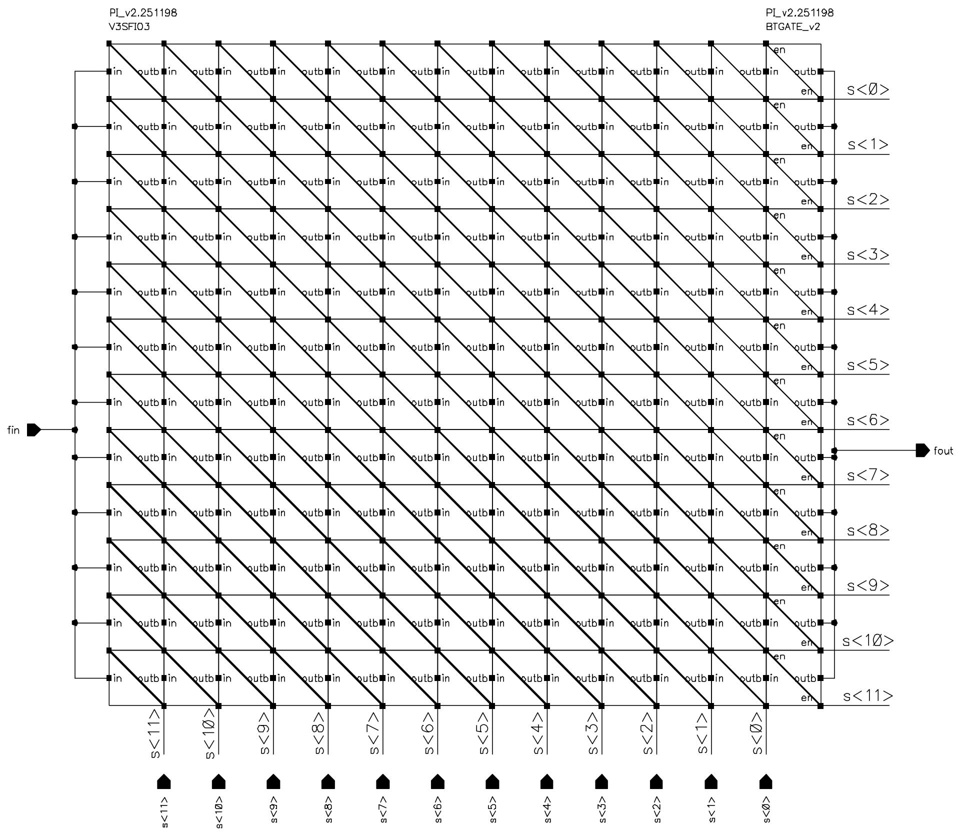

Figure 3. The single Pipeline channel schematic.

Each clock cycle first cell in the one of the twelve sub-channels is loaded. Then, each eleven clock cycles the data is shifted by one memory cell. As the memory cell inverts the data, each bit is refreshed every twenty two clock cycles. Last cell in the channel consists of the inverter and the nmos switch. The schematic of the cell is shown in figure 4.

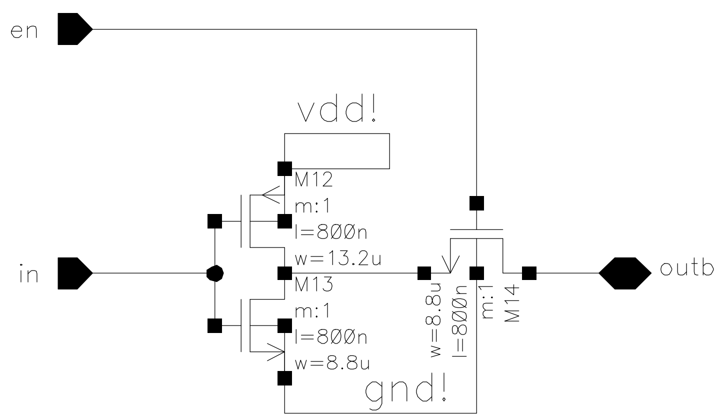

Figure 4. The output cell of the Pipeline.

3. Modifications

The following modification have been made in comparison to the previous ABCD design:
- input clock signal has been inverted (following the solution of the "DCL" problem);
- sizes of the output cell transistors were increased (following the solution of the "DCL" problem);
- a dflip-flop was added to synchronize the *clrb* reset signal with the clock.

4. Simulation status

The following simulations have been done:
- Pipeline cell analogue simulation (Eldo, all the corners);
- Pipeline to Output Buffer interface simulation (Eldo, all the corners).

The following actions are planed:
- analogue simulation of a single channel (Eldo, all the corners)
- creating new Verilog models (with corner parameters);
- analogue simulation of a few channels + interfaces from Input Register and to the Output Buffer.

5. ABCD1 Speed Problem Description

During the ABCD1 tests on the ATS VLSI test a serious speed limitation of the ABCD chip was discovered. It was first known as the "DCL Problem", because the limitation was observed for the test patterns, which were developed to test the Data Compression Logic. During the test the *pulse input register* command was sent to the ABCD followed by the *L1* command switching through all the DCL modes.

After more detailed tests the speed limitation was found in the interface between the Pipeline and the Output Buffer. The analogue simulation with the new models confirmed that the problem is well understood.

The following changes have been made to avoid the speed limitation:
- the Pipeline output cell transistors have been resized;
- the Output Buffer input cell transistors have been optimized;
- the clock phase in the Pipeline has been inverted.

The modified Pipeline – Output Buffer interface has been simulated for all the corners with Eldo.