Top Level Simulation.

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1. Introduction.

The top-level simulation is one of the critical issues of the chip design. The way it is run can result in good or faulty behavior of the whole chip. For the digital part of the ABCD1 chip the major discovered problems were a result of improper inter-block timing adjustment. Now the complete set of the models (including pre- and post-rad) is available for DMILL technology and the top-level timing can be estimated much more precisely.

2. General approach.

There are three groups of the simulations to be distinguished:
- Analogue simulations. The goal for these simulations is to check the critical nets and devices in the chip e.g. pipeline – output buffer interface or clock three simulation.
- Analogue simulations supporting Verilog simulations. These include characterization of the standard cells and the simulations run to provide the timing data for behavioral Verilog models (e.g. for the Pipeline or the LVDS receiver).
- Verilog simulation of the whole chip with and without backannotation.

3. Simulation status.

Done:
- Characterization of the standard cells (Eldo).
- Pipeline – Output Buffer interface simulation (Eldo).
- Skill procedure for backannotating the parasitics from the extracted view to Verilog.
- Verilog simulation of the whole chip with old Verilog models.

To be done:
- Simulation of the clock three.
- Simulation of the data passing through: Input Register -> Pipeline -> Output Buffer for 4 channels (Eldo).
- Simulation of the DCL; first – last channel hit (Eldo).
- Verilog simulation of the whole chip with backannotation.
- Verilog simulation of a few chips together.