Original proposal made to SCT Colaboration to implement the trim DAC option in the ABCD chip.

I. Motivation.

The measured threshold spread in the ABCD prototype chip is substantially bigger compared to the design values. The measurements indicate that the effective matching of device parameters is worse by a factor of about 5 compared to the values specified by the technology vendor. The source of this discrepancy is not fully understood yet.

In addition a possible worsening of the matching of the device parameters after irradiation should be anticipated. No results on the DMILL technology with respect to that problem are available at the moment but a significant effect was observed in the MAXIM process used for the CAFE-M chip.

Taking all these results into account we are concerned about the possibility of reaching the SCT specification with the circuit configuration implemented presently in the ABCD front-end. Although some improvement of the technology parameters is expected we believe that "tuning" the present configuration will not provide us sufficient headroom to cover possible degradation of threshold uniformity after irradiation. A possible "tuning" of the present configuration would result in increasing the gain in single-ended stages of the front-end circuit which is not desirable from the point of view of system aspects.

The analysis of present results and of possible solutions lead us to a proposal of implementing an individual trim DAC per channel which will allow us to correct the threshold non-uniformity. The functionality of the threshold DAC for a common threshold control for all the channels in the chip will remain as it is in the present prototype. The feasibility study of such a solution has been performed and the conceptual design is already worked out.

II. Specification concerning the trim DAC

1. Gain of the front-end circuit	60 mV/fC
2. Range of the trim DAC	60 mv
3. Resolution of the trim DAC	4 bit (4 mV/step)
4. Expected threshold spread after correction	4 mV p-p

III. Impacts of the proposal

1. Die area and power consumption.

The die area will be increased by about 5 mm^2, i.e. by 10% compared to the present ABCD prototype. The increase is partially due to the trim DACs (6%) and partially due to the fact that a new type of resistor has to be used (4%). The new rad-hard resistors have to be implemented in the next prototype independent of the trim DACs.The additional power consumption for the trim DACs will be less then 100 micro-Watt per channel.

2. Operation.

It is foreseen that the correction of the threshold offsets will be done once during the building of a data base for each chip. The correction of the threshold offsets will be performed and the values of the trim DACs settings will be stored in the data base. Then after each initialization of the chip, the correction values of the trim DACs need to be loaded. For setting the nominal threshold as well as for threshold scanning for calibration purpose only the common threshold DAC will be used like in the present chip.

3. Risk.

The risk associated with the addition of trim DACs is considered to be very small. The trim DAC will be based on the same structure as the other DACs implemented in the ABCD chip. However, implementation of the trim DACs will require a new design of the command decoder and a new layout of the front-end. We propose that the next submission to the DMILL process will include two versions of the ABCD chip; one with the trim DACs and one in which some "tuning" of the front-end circuit will be implemented. The second one is expected to meet SCT specification concerning the threshold uniformity providing we obtain device parameters matching as specified by the vendor. It should be stressed that due to changes in the resistor technology the "tuning" of the front-end without trim DACs will result in a substantial redesign of this part of the ABCD and is not risk free either.

We believe that in the present critical situation with the front-end electronics this is the most efficient way we can proceed, at least as far as the DMILL technology is concerned.

4. Schedule

According to the present estimate a full engineering of the proposed modification will require about 3 months of work of a few key designers involved in the project. This work can be done mostly in parallel with other work on the front-end without trim DACs and on the back-end of the ABCD. Given the present situation with the available designers the same persons will be working on both versions. We estimate that this will results in an additional 1-2 months delay in submission of the two versions compared to submission of the ABCD without trim the DACs only.