Corner and sensitivity analysis of the ABCD front-end

The basic set of simulation was performed for all combinations of:

- 3 sets of corner parameters for resistors (as listed below)
- 9 sets of corner and postradiation parameters for MOS transistors (as listed below)
- 3 sets of parameters for BIPOLARs (tt, ll, post_rad)
- temperatures 0 and 40 deg C
- VCC supply voltage 3.3, 3.5 and 3.7 V

In addition some critical combinations of VCC (analog) and VDD (digital) supply voltages were tested.

Corner and post-radiation parameters

Resistors

RSET=0	typical		
RSET=-1	lower value	RLV-24%	RBXB-24%
RSET=+1	higher value	RLV+24%	RBXB+24%

MOSFETs

PSET<=0	typical-typical	VtPMOS = -0.80	VtNMOS = 0.87
PSET=1	slow-slow	VtPMOS = -0.92	VtNMOS = 0.95
PSET=2	slow-fast	VtPMOS = -0.91	VtNMOS = 0.79
PSET=3	fast-slow	VtPMOS = -0.70	VtNMOS = 0.95
PSET=4	fast-fast	VtPMOS = -0.69	VtNMOS = 0.79
PSET=5	slow-slow-irradiation	VtPMOS = -1.13	VtNMOS = 1.05
PSET=6	slow-fast-irradiation	VtPMOS = -1.11	VtNMOS = 0.69
PSET=7	fast-slow-irradiation	VtPMOS = -0.91	VtNMOS = 1.05
PSET=8	fast-fast-irradiation	VtPMOS = -0.87	VtNMOS = 0.69

NPNs

BIPOLAR	tt	beta = 250
BIPOLAR	hh	beta = 130
BIPOLAR	ll	beta = 370
BIPOLAR	post_rad	beta = 45-60

From each analysis the following critical circuit parameters are extracted:

Threshold (Thrs) - threshold voltage (VT1 - VT2) generated by the threshold DAC
Effective threshold (eThrs) - voltage difference directly at the discriminator inputs
DC bias at the preamplifier output (DC1)
DC bias at the second stage output (DC2)
Peaking time at the shaper output (PkTim)
Gain at the diff pair output (Gain)
Delay of the discriminator response with respect to start of the signal at the diff pair output (Delay)
Width of the discriminator response (Width)
Level of calibration signal generated by the calibration DAC (Icharge).

The results are presented separately for each BIPOLAR corner (ll, tt, posti).
Each plot contains results for:
(3 resistor corners) x (9 MOS corners) x (2 temperatures) x (3 supply voltages).