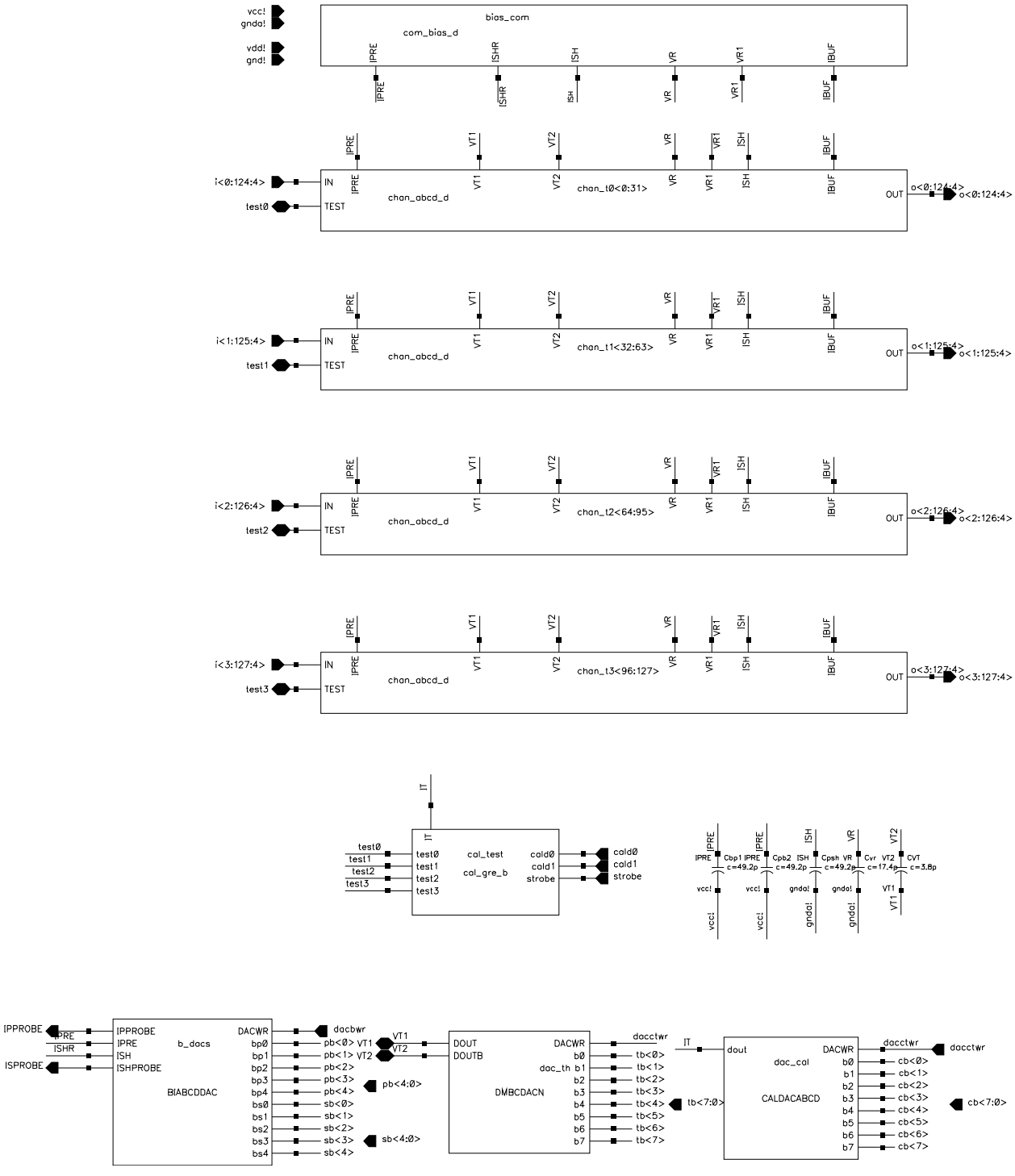
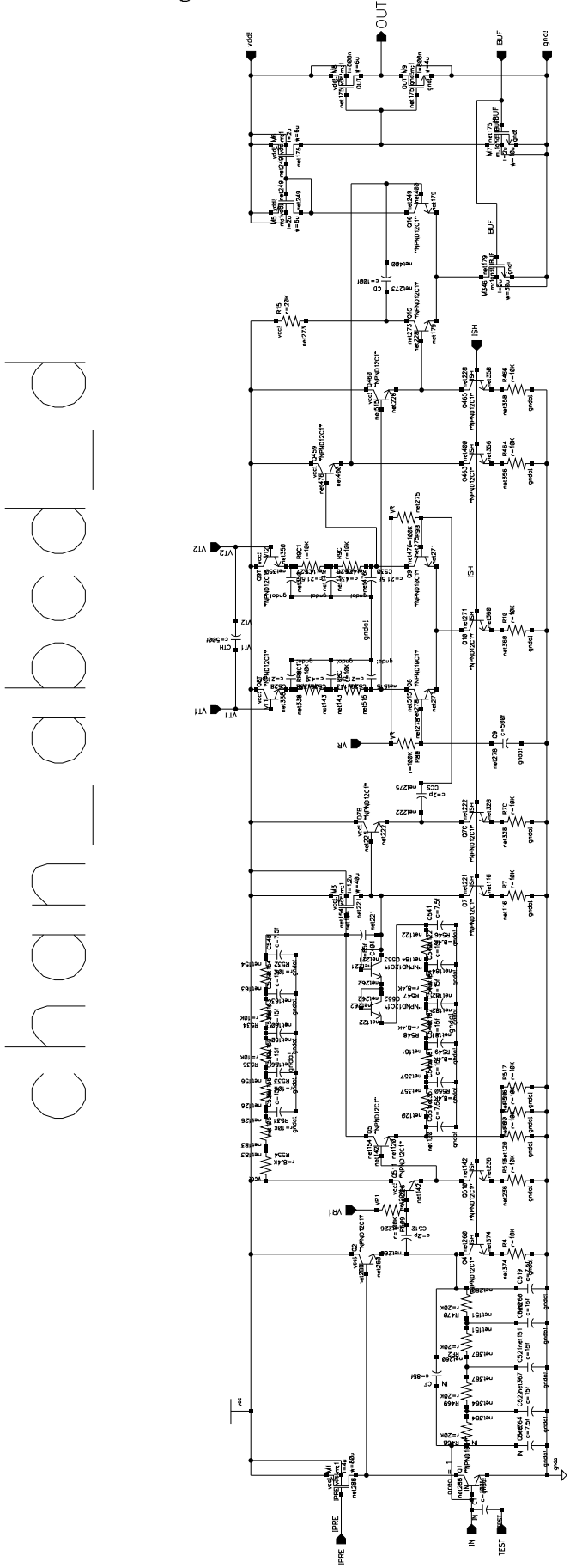
ABCD front-end without TrimDAC

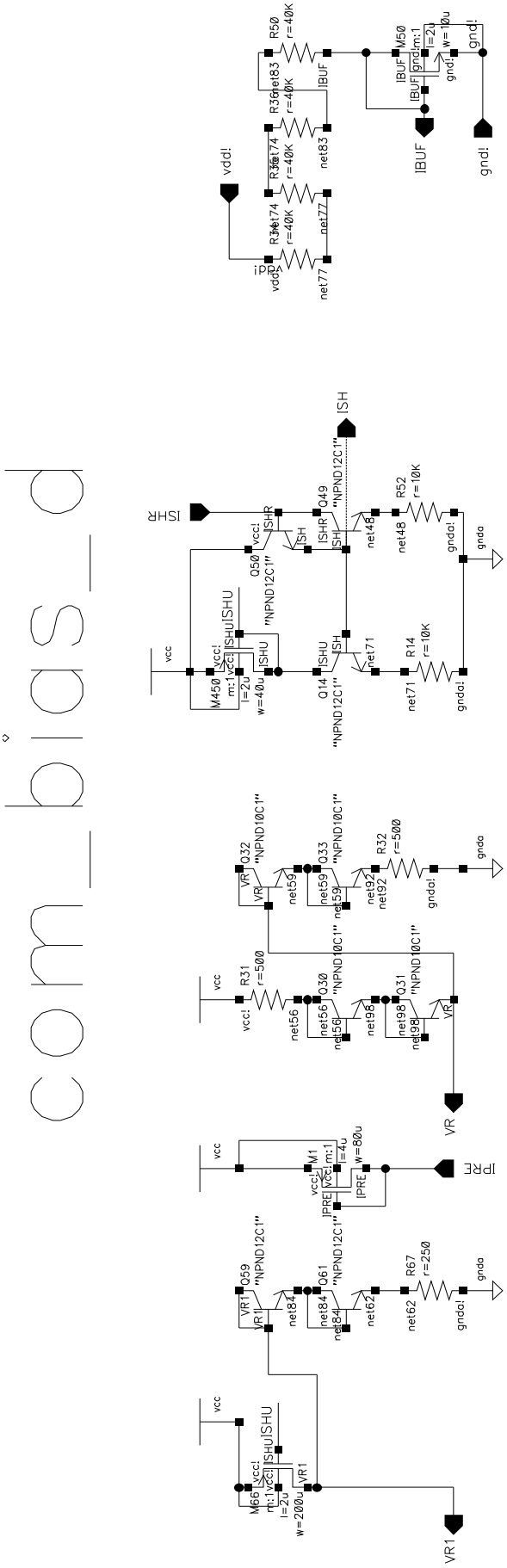
Top level schematic

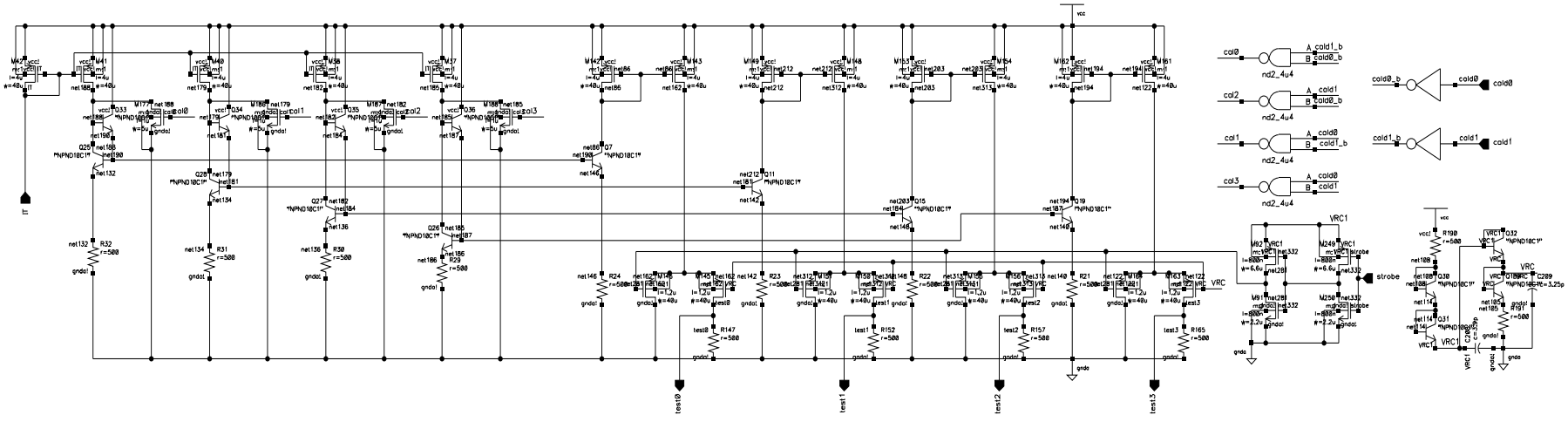


Single channel schematic



Common bias schematic

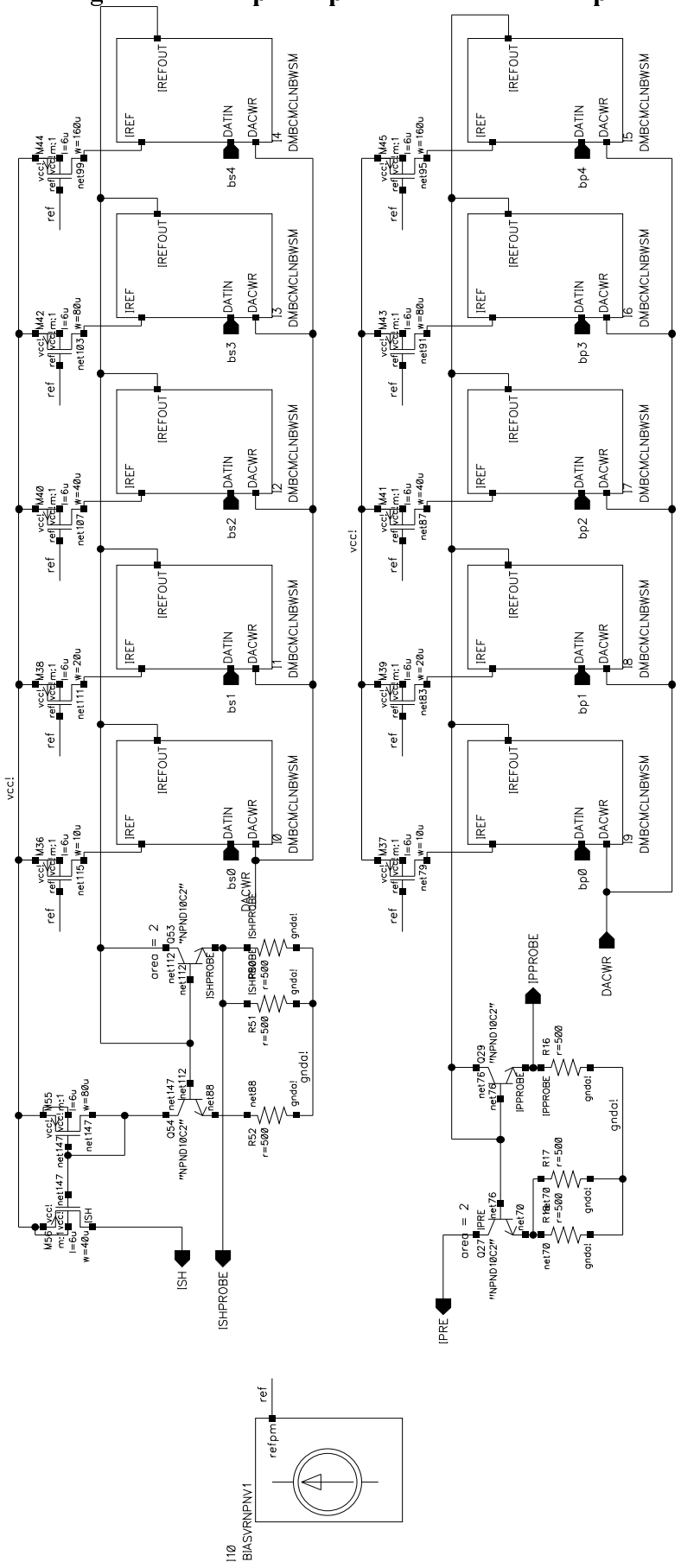




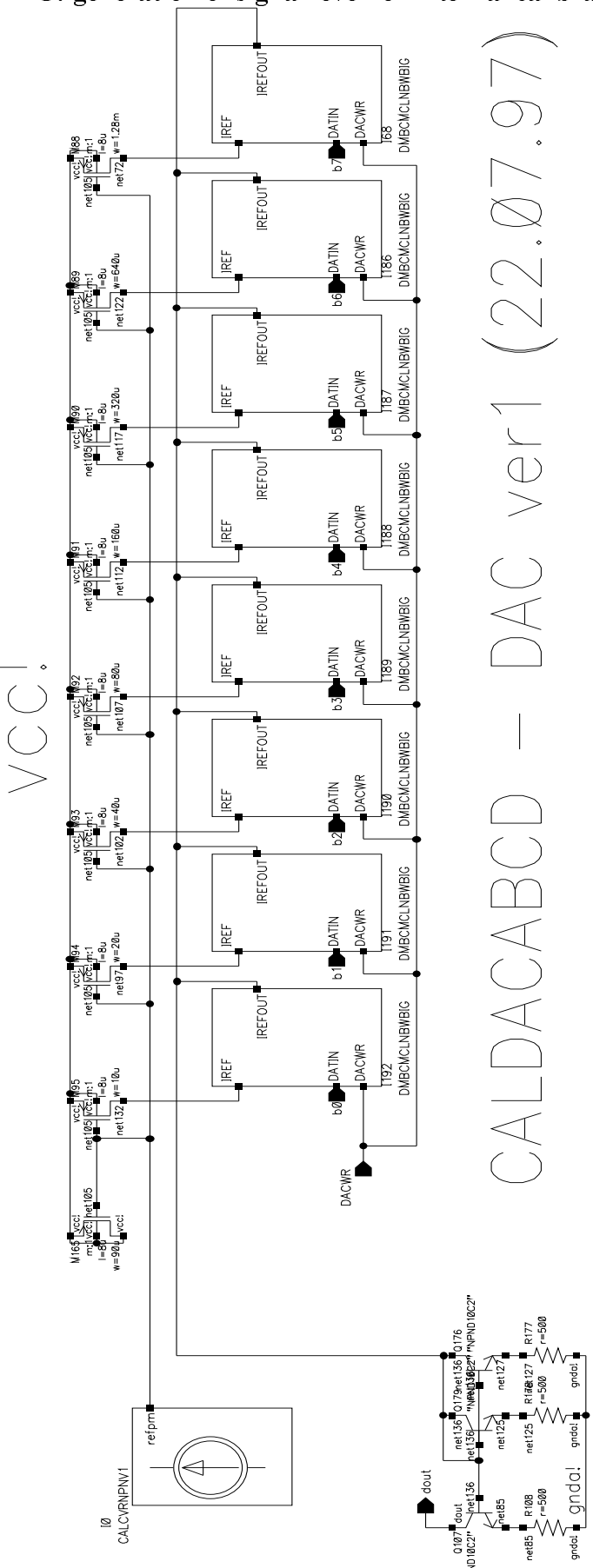
Calibration circuit

calibration circuit for p-side readout
output referenced to gnd, 24.04.97

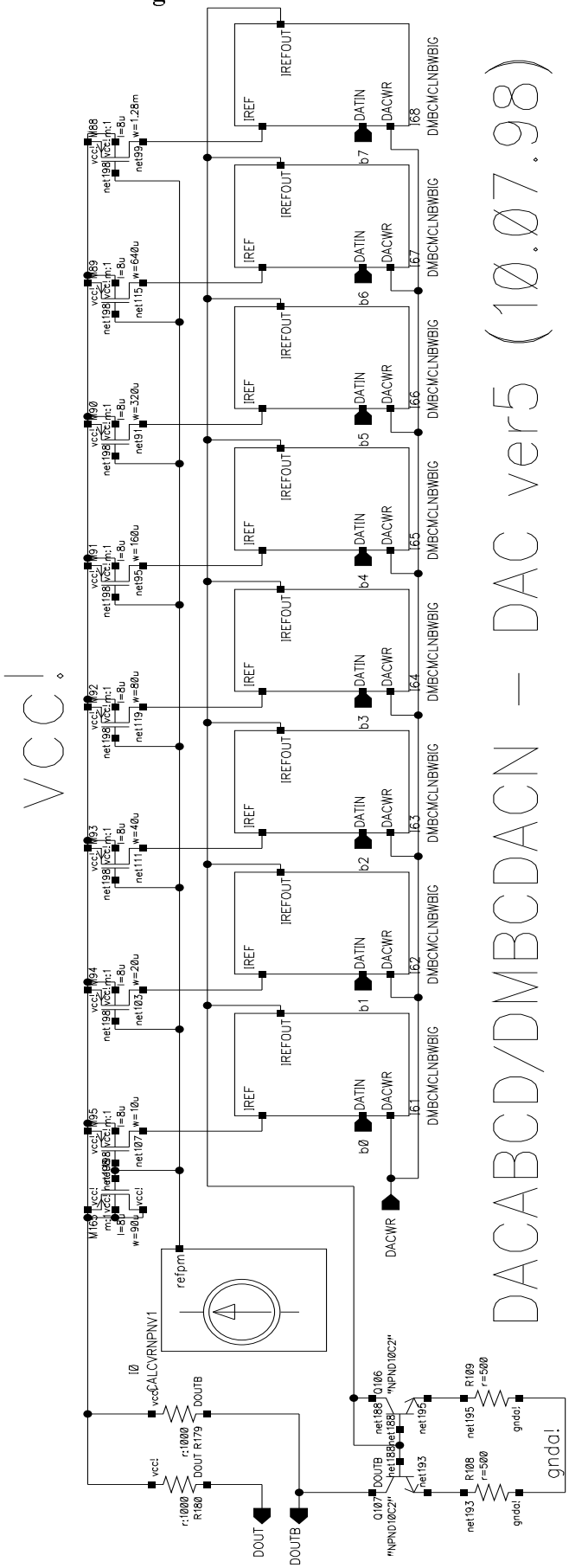
Bias DAC: generation of preamplifier current and shaper current



Calibration DAC: generation of signal level for internal calibration circuit



Threshold DAC: generation of differential threshold level



List of simulation results

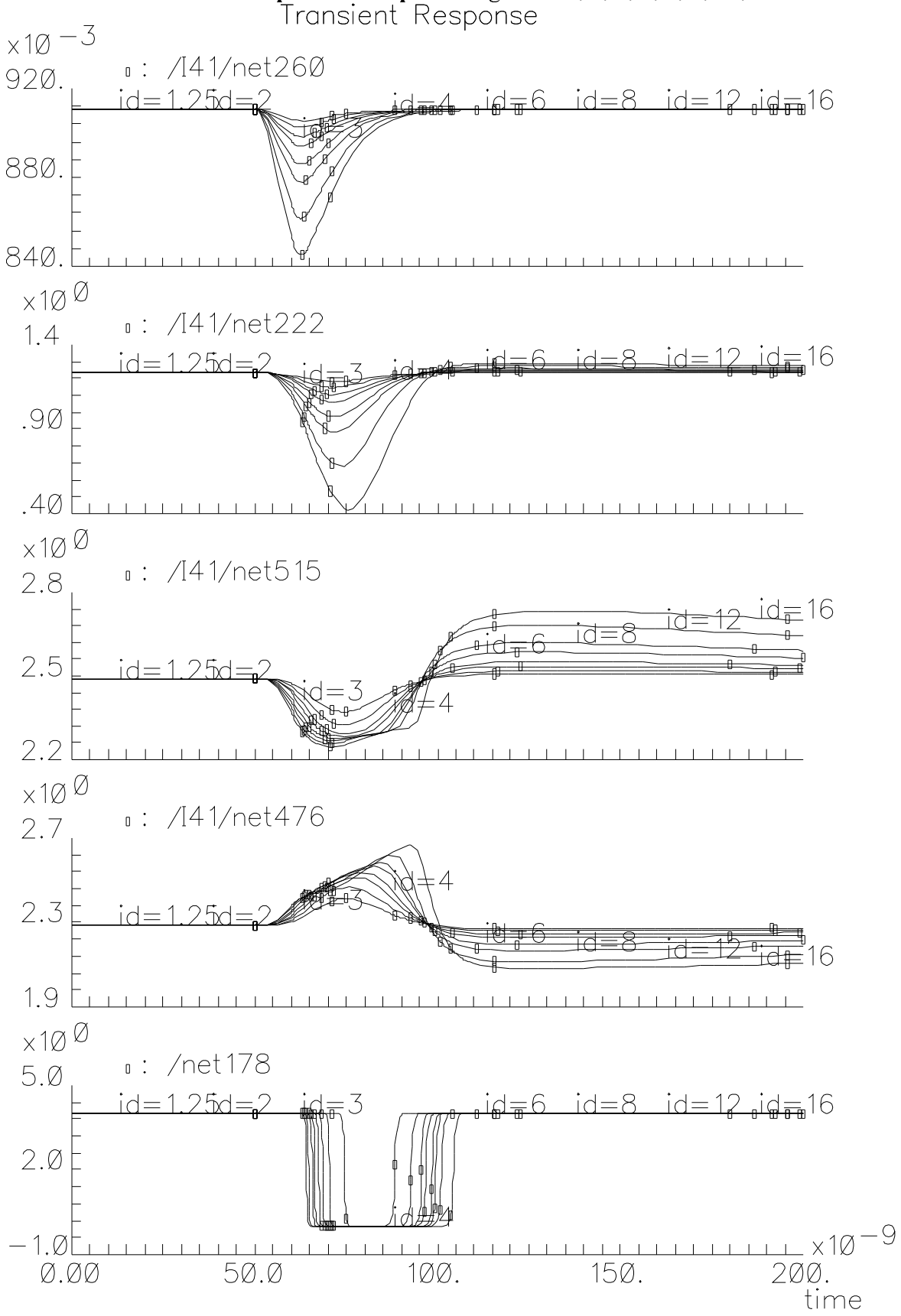
A. Single channel + common bias + calibration circuit + all DACs;
Input capacitance = 20 pF, threshold = 1 fC, typical parameters, TEMP = 0 deg C
net260: preamplifier output
net222: second stage output
net515, net476: output of the differential pair
net178: output of the CMOS inverter

1. Transient response for input charges: 1.25, 2, 3, 4, 6, 8, 12, 16 fC.
2. Differential signal on the diff pair output for input charges: 1.25, 2, 3, 4, 6, 8, 12, 16 fC.
3. Walk time evaluation; CMOS inverter output for input charges: 1.25, 2, 3, 4, 6, 8, 12, 16 fC.
4. Double pulse resolution; two 3.5 fC signals spaced by 50 ns.
5. Double pulse resolution for input charges: 1.25, 2, 3, 4, 6, 8, 12, 16 fC spaced by 50 ns.
6. Details of the CMOS inverter output for (5).
7. Response to overload; 80 fC signal followed by 3.5 fC one, 1us later.
8. Input impedance (magnitude and phase) vs frequency.
9. Open loop gain (magnitude and phase) of the preamplifier vs frequency.
10. Power supply rejection ratio; AC analysis.
11. Power supply rejection ratio; TRAN analysis, 40 MHz, 20 mV pp signal on VCC
12. Power supply rejection ratio; TRAN analysis, 100 kHz, 200 mV pp signal on VCC.

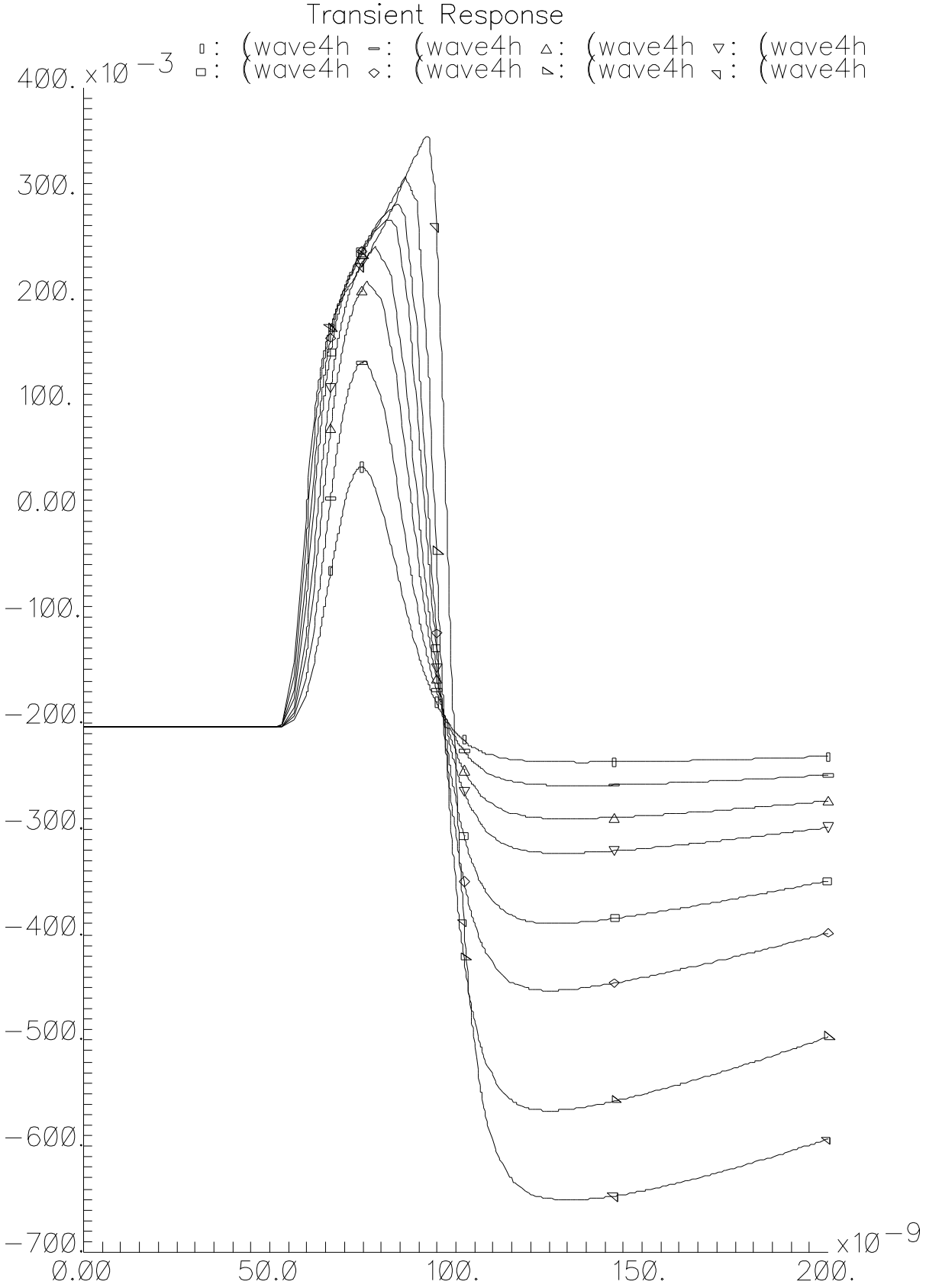
B: All circuitry as on the top level schematic;
equivalent circuit of the strip detector included,
interstrip capacitance: 8 pF to each neighbour

1. Transient response of one stimulated channel while 32 channels stimulated simultaneously with 4 fC signal form the internal calibration circuit.
2. Transient response of a channel neighbouring to the stimulated one.

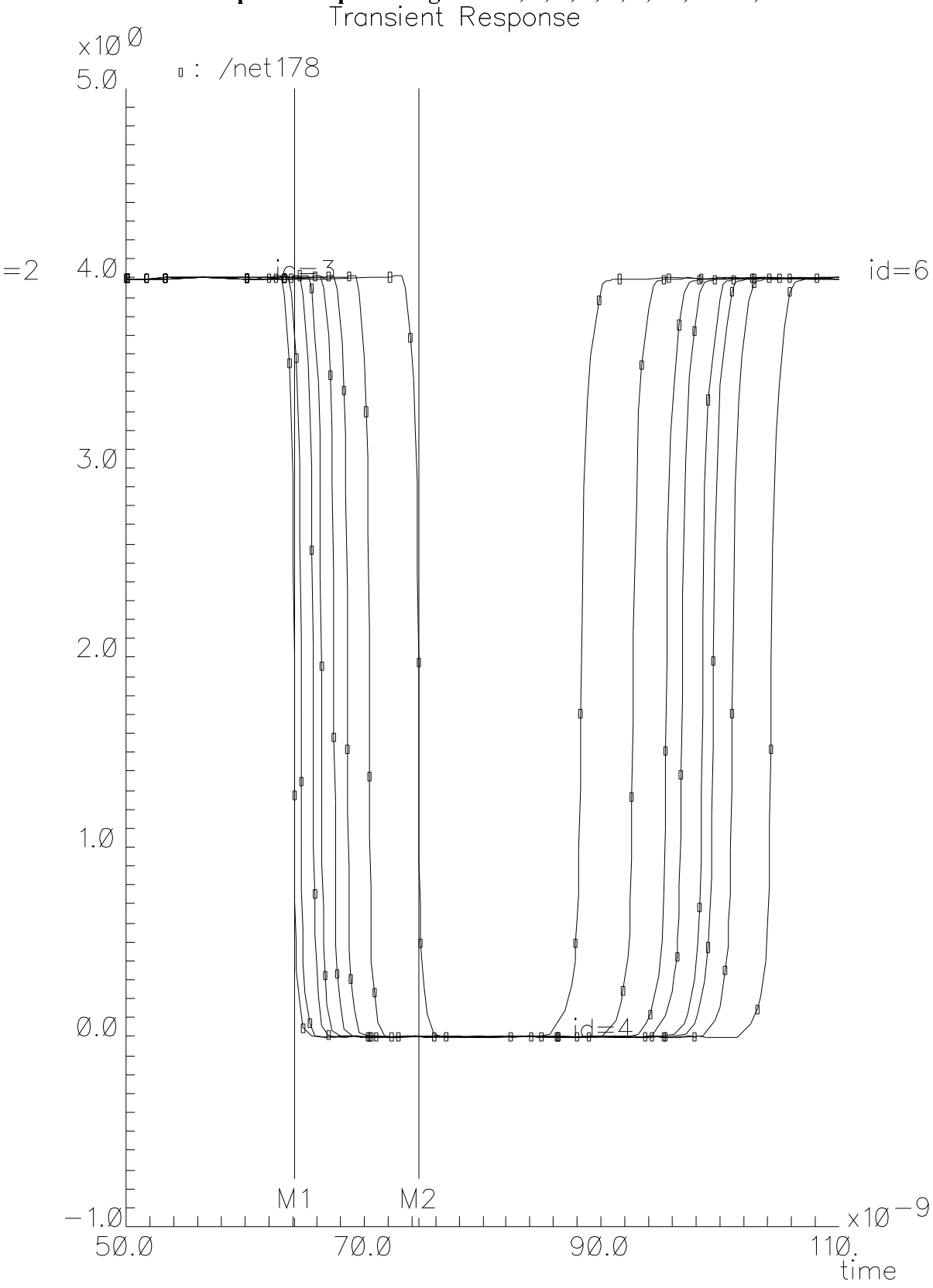
A1: Transient response for input charges: 1.25, 2, 3, 4, 6, 8, 12, 16 fC



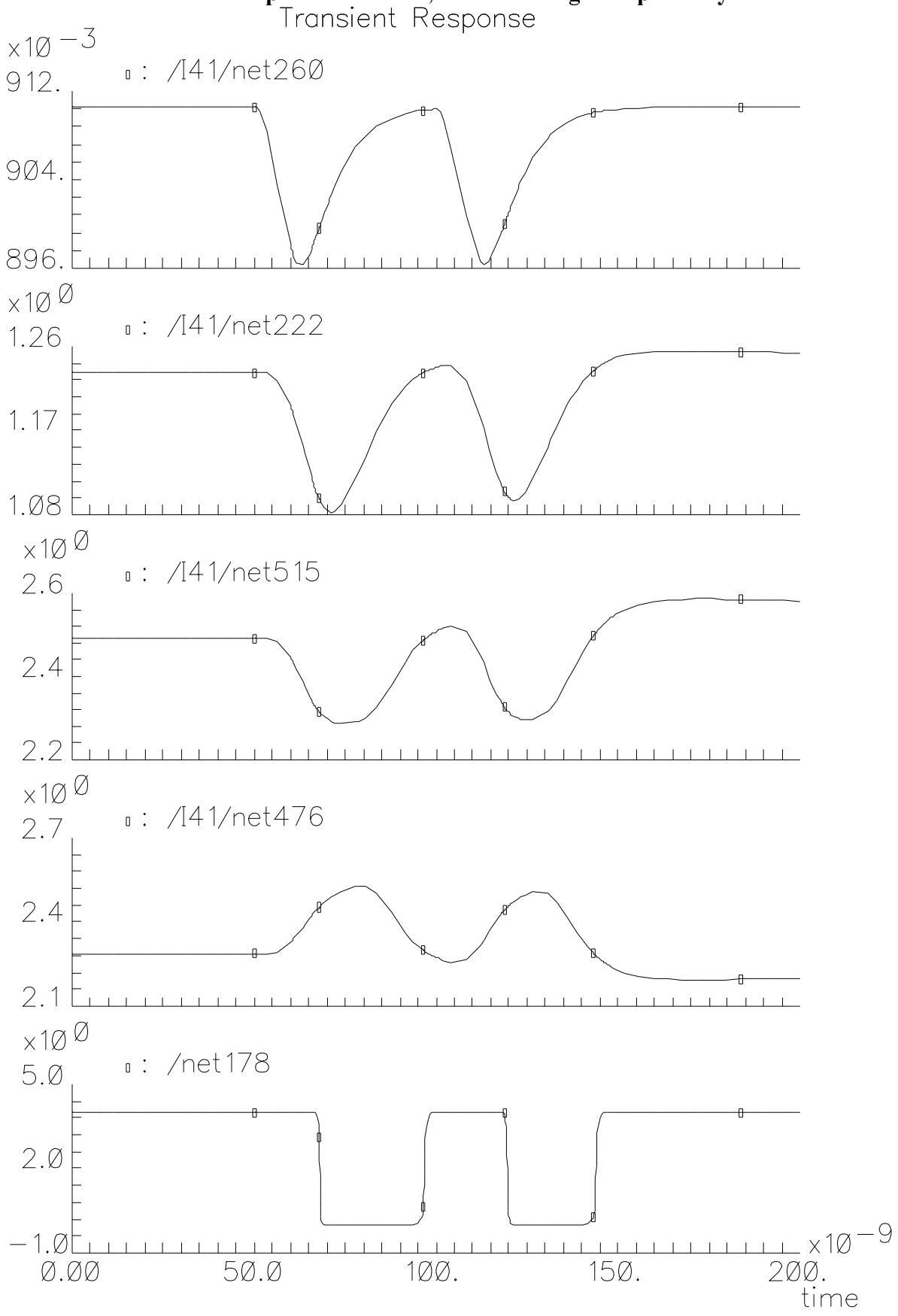
A2: Differential signal on the diff pair output for input charges: 1.25, 2, 3, 4, 6, 8, 12, 16 fC.



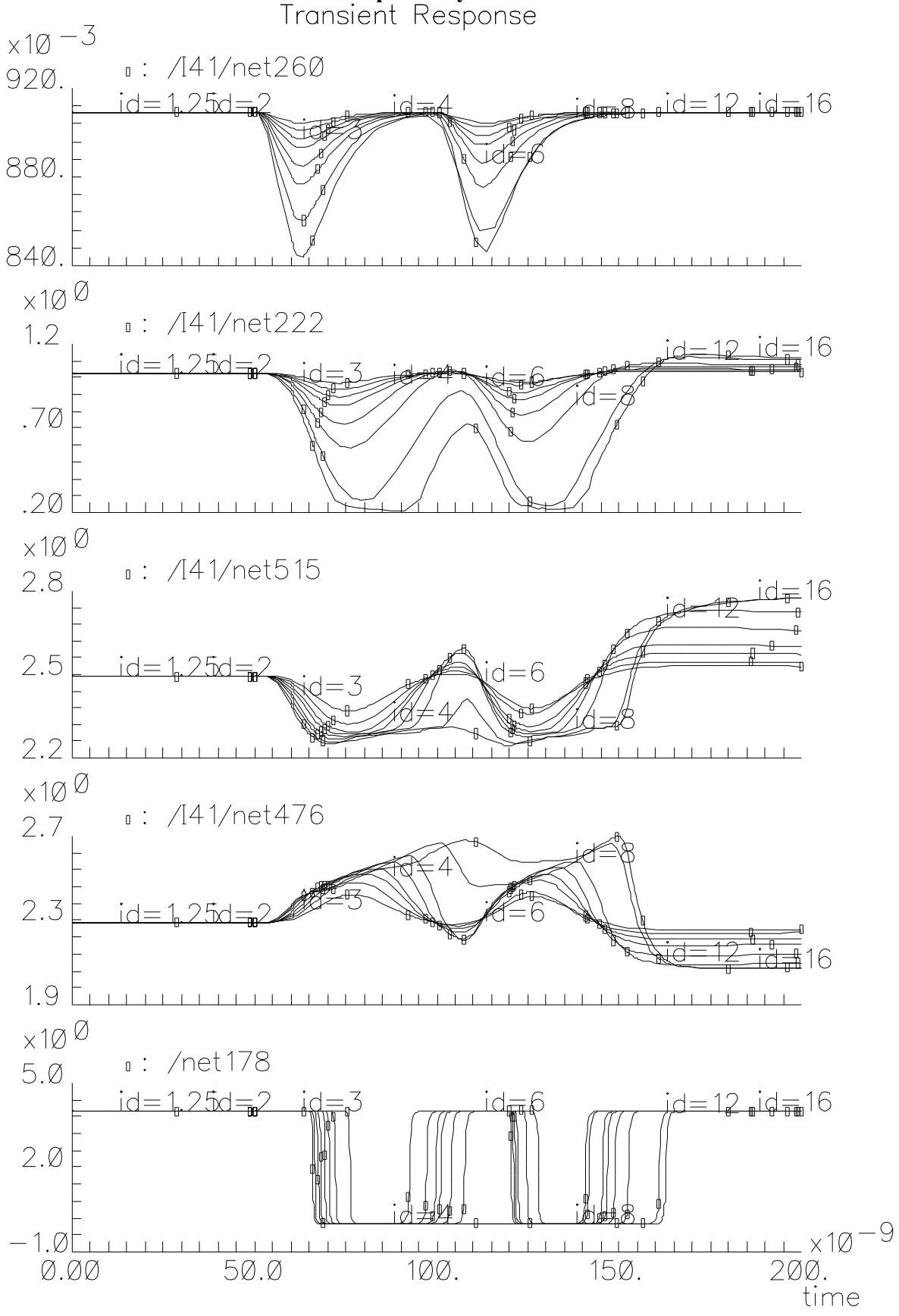
A3: Walk time evaluation;
CMOS inverter output for input charges: 1.25, 2, 3, 4, 6, 8, 12, 16 fC, Walk < 12 ns



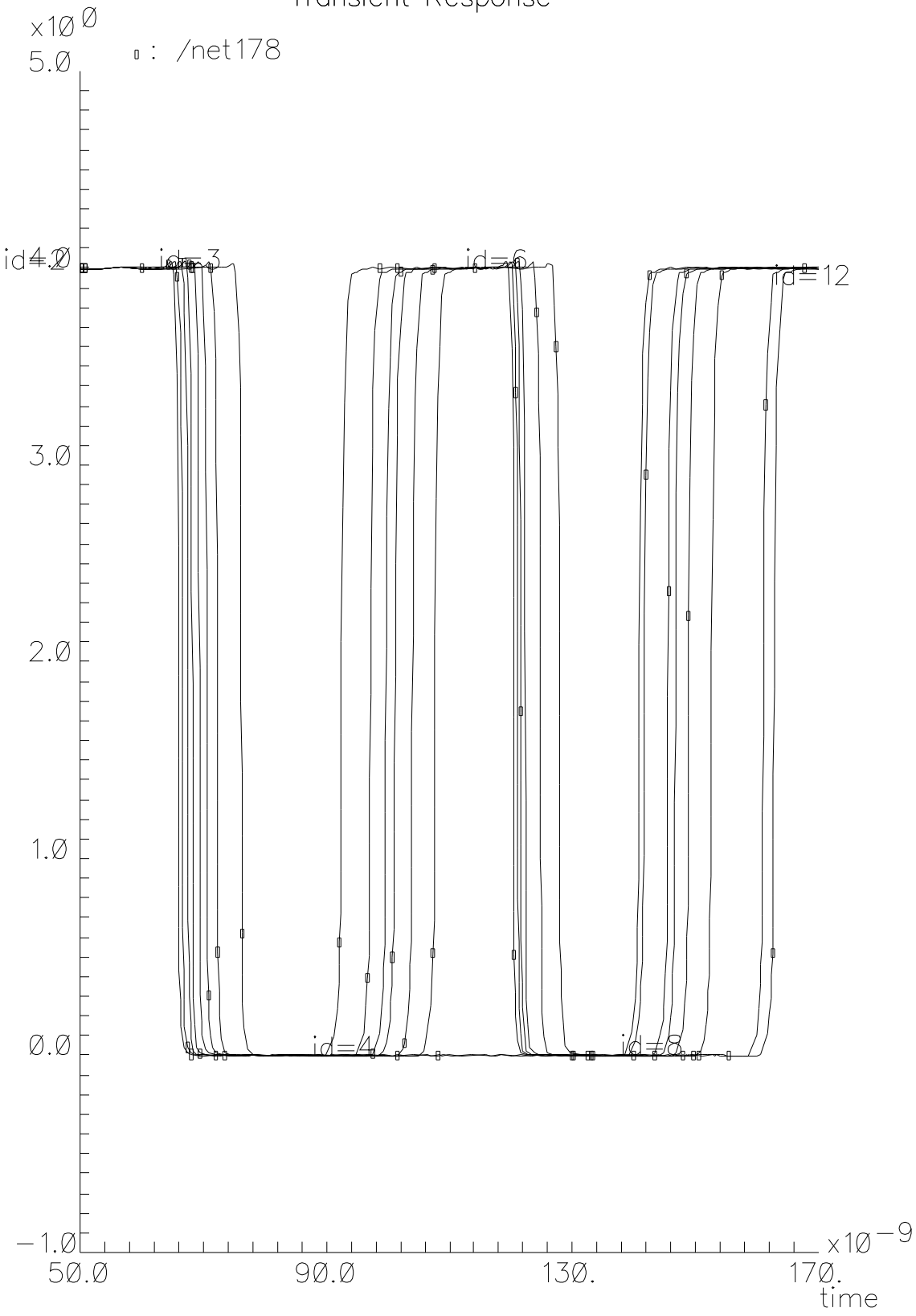
A4: Double pulse resolution; two 3.5 fC signals spaced by 50 ns.



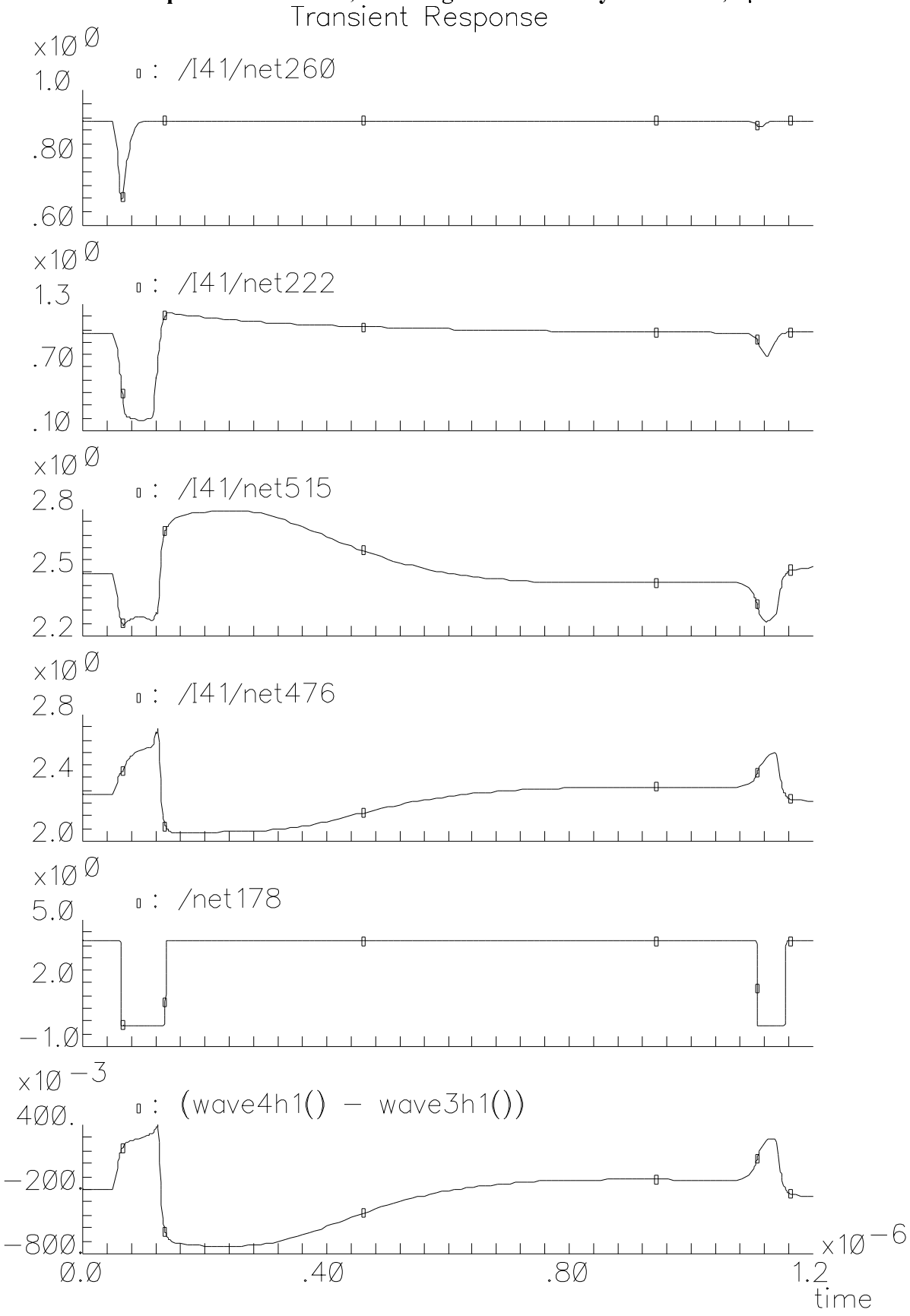
A5: Double pulse resolution for input charges: 1.25, 2, 3, 4, 6, 8, 12, 16 fC spaced by 50 ns.



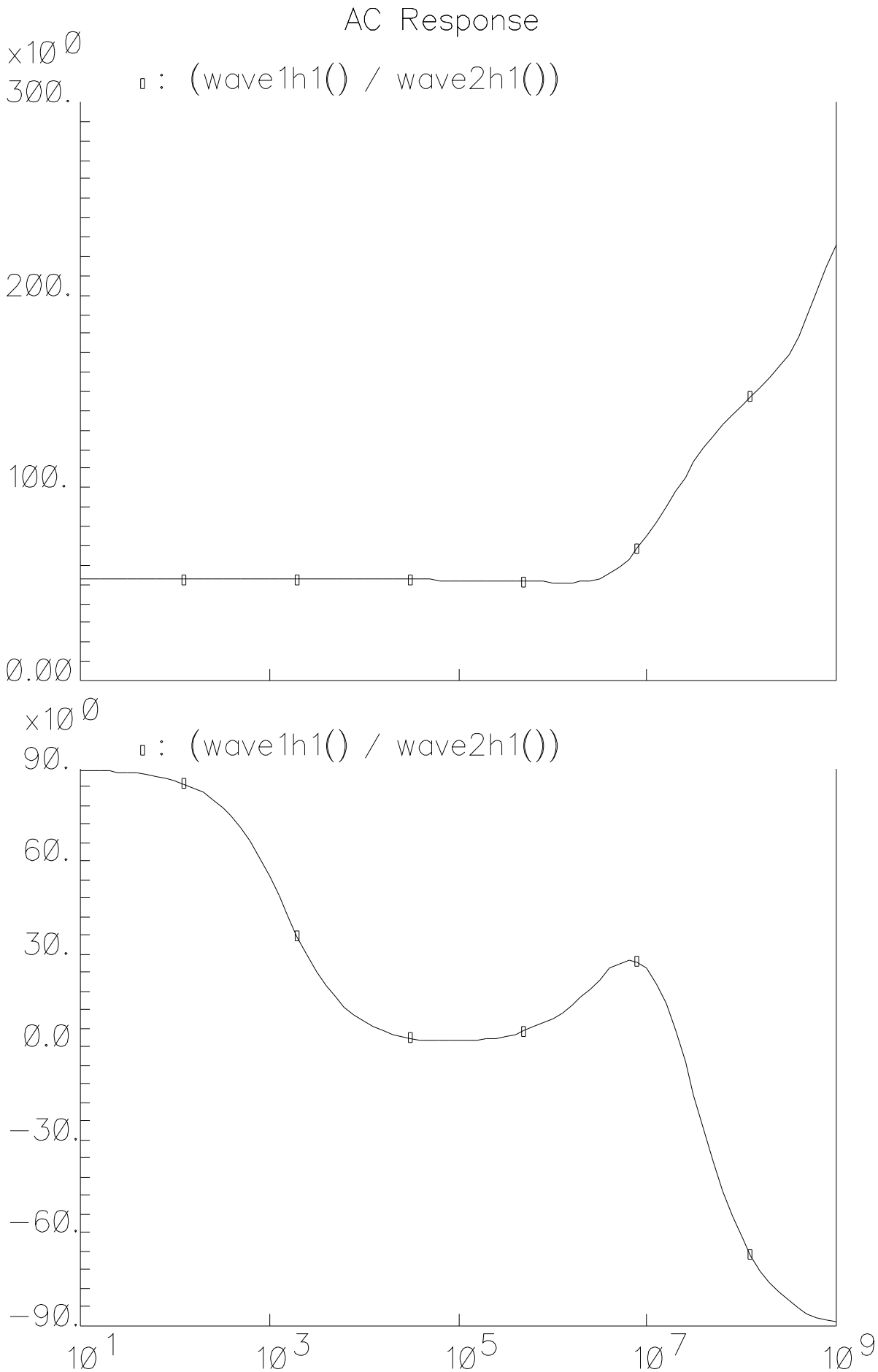
A6: Details of the CMOS inverter output for (A5)
double pulse resolution of 50 ns over input signal range 1.25 - 8 fC



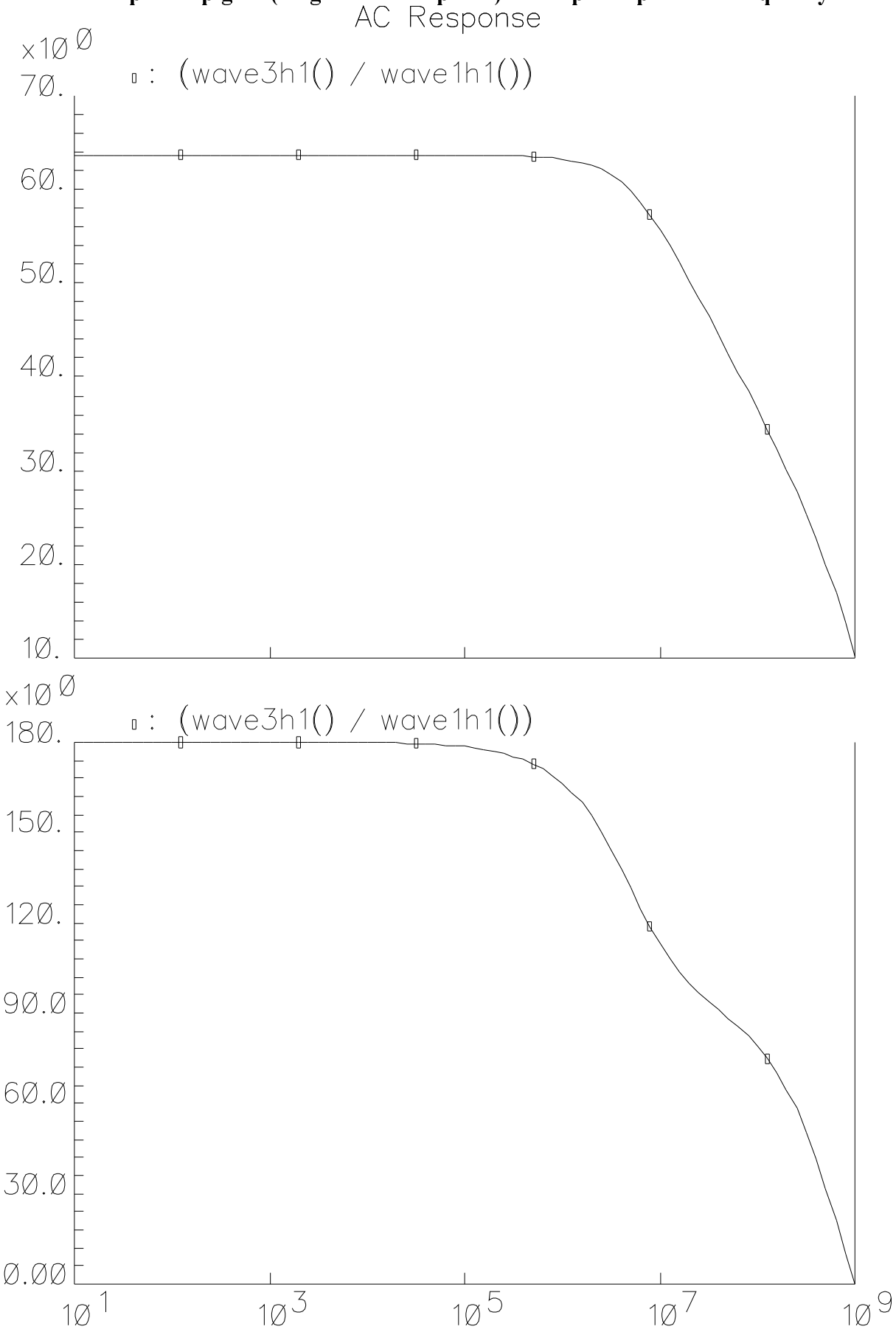
A7: Response to overload; 80 fC signal followed by 3.5 fC one, 1μs later



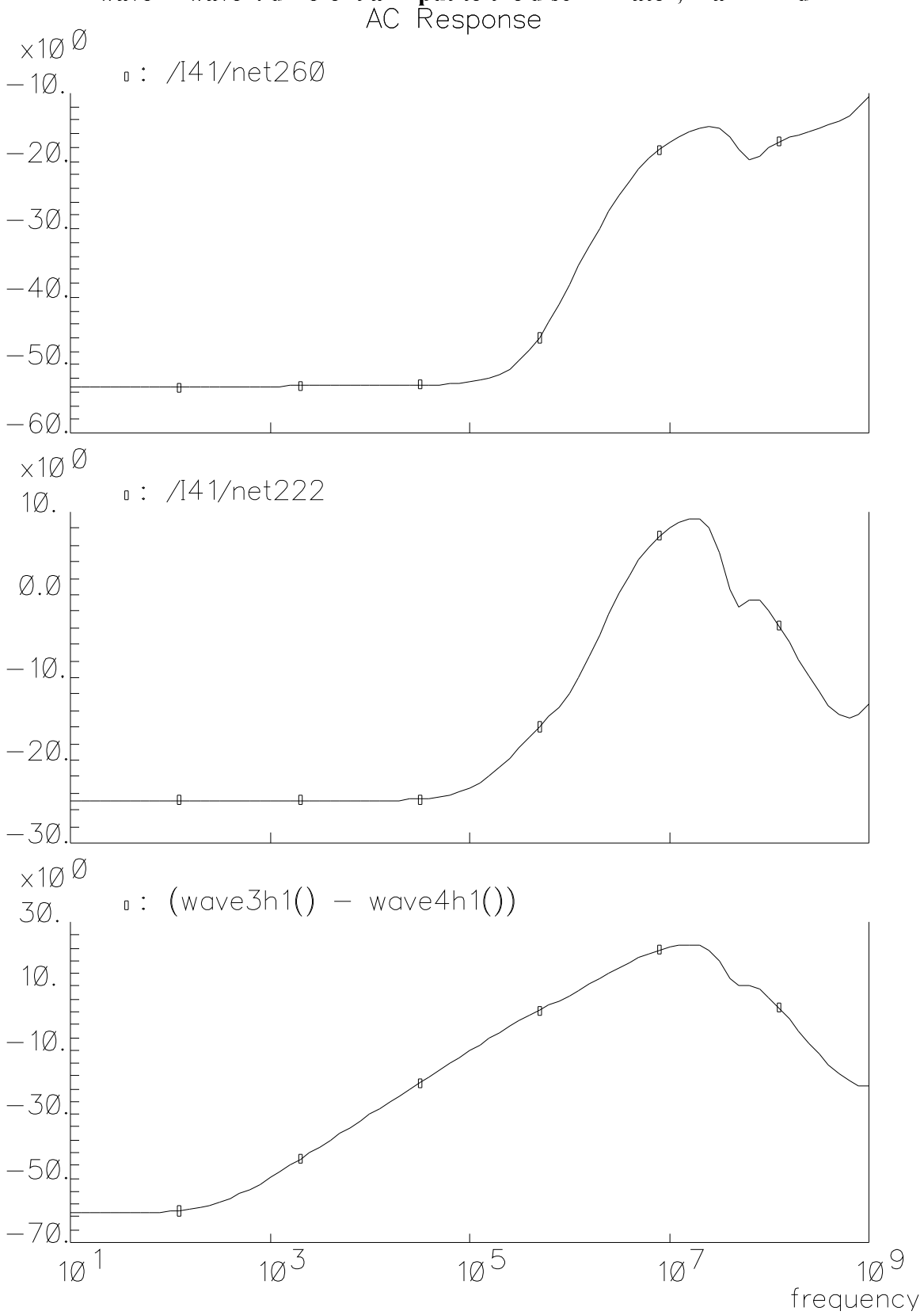
A8: Input impedance (magnitude and phase) vs frequency


AC Response
x10 0
300.
: (wave1h1() / wave2h1())
200.
100.
0.00
x10 0
90.
: (wave1h1() / wave2h1())
60.
30.
0.0
−30.
−60.
−90.
10 1
10 3
10 5
10 7
10 9

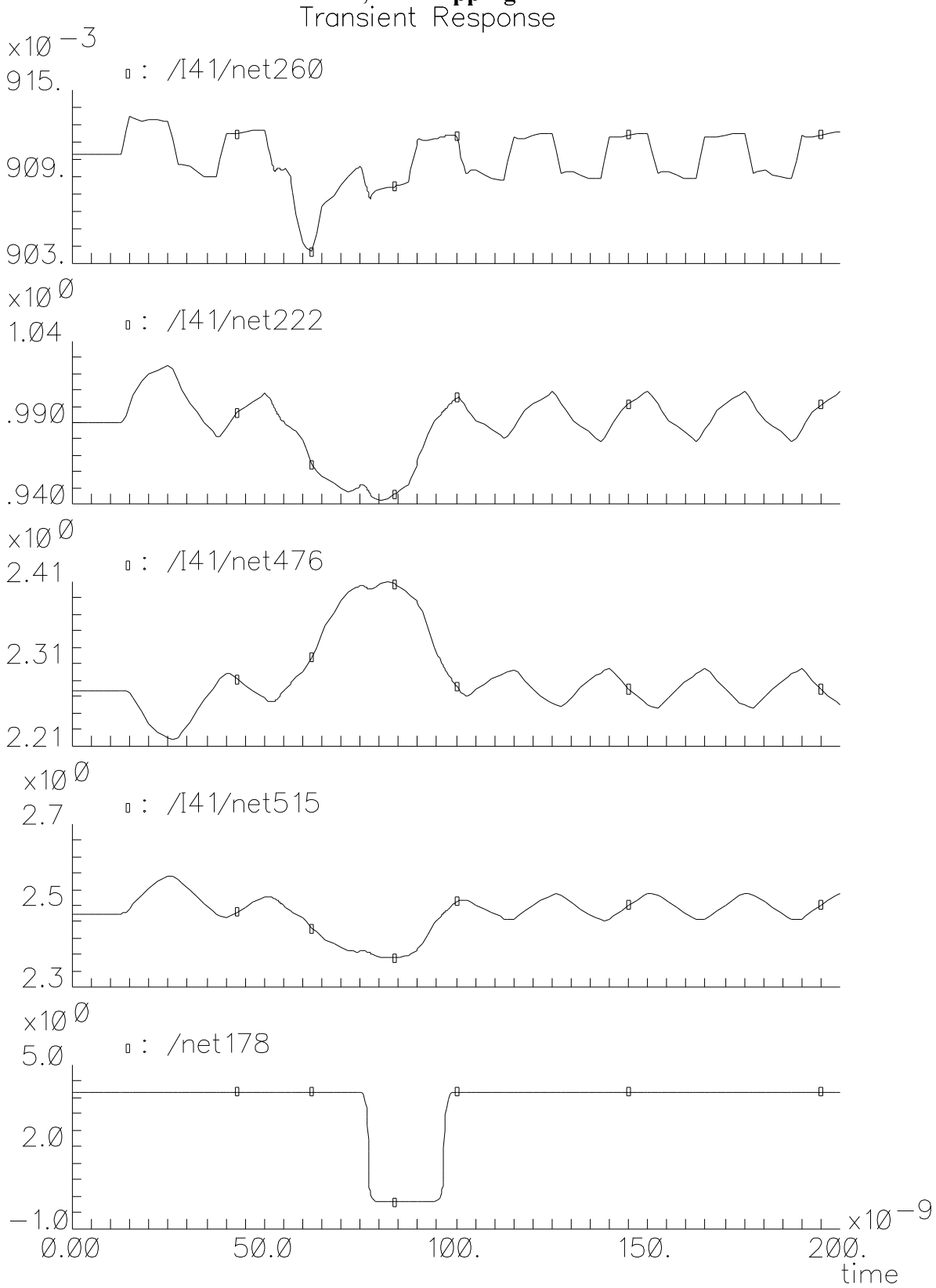
A9: Open loop gain (magnitude and phase) of the preamplifier vs frequency



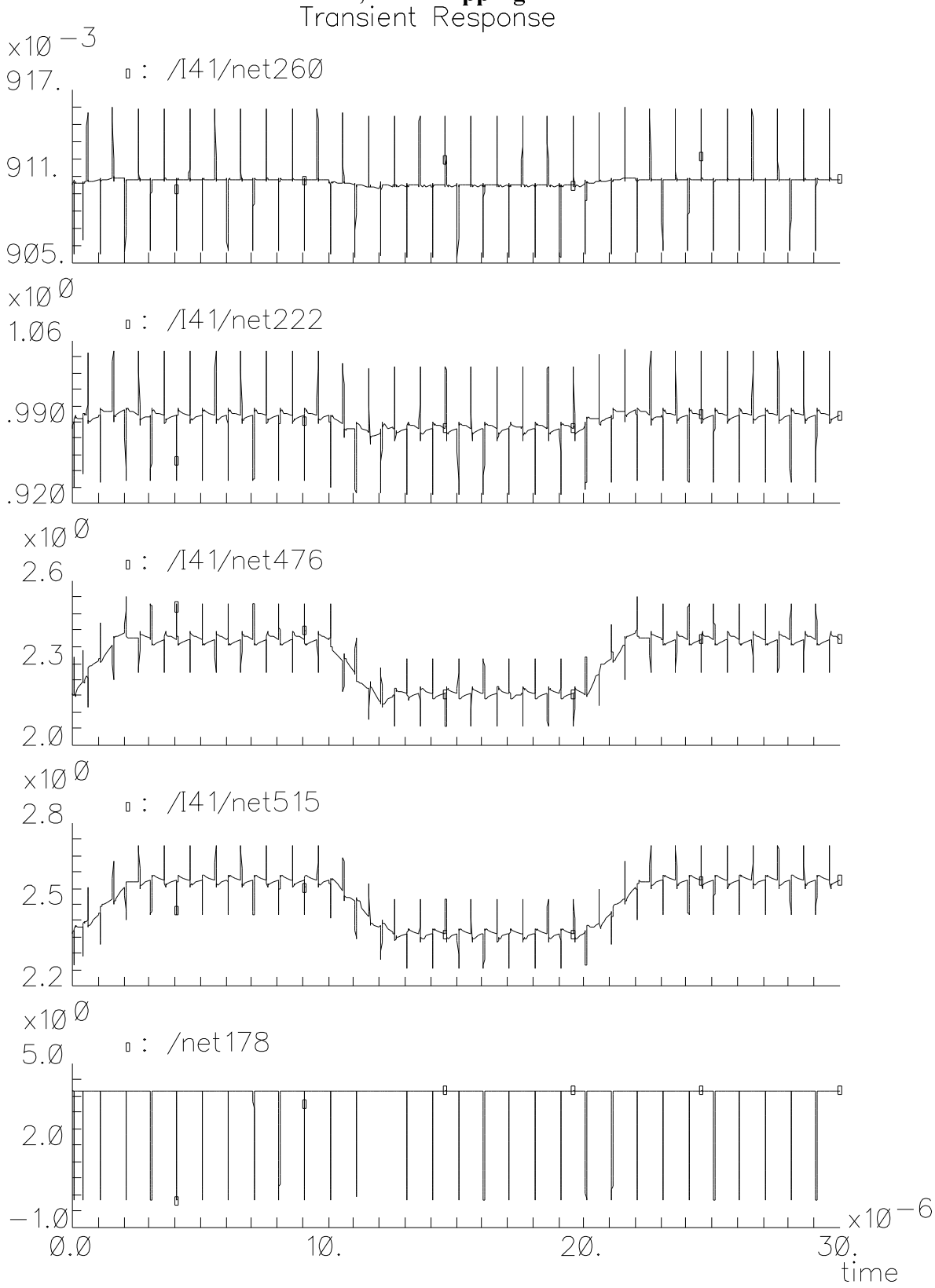
A10: Power supply rejection ratio; AC analysis
wave3 - wave4: differential input to the discriminator; max = 26 dB



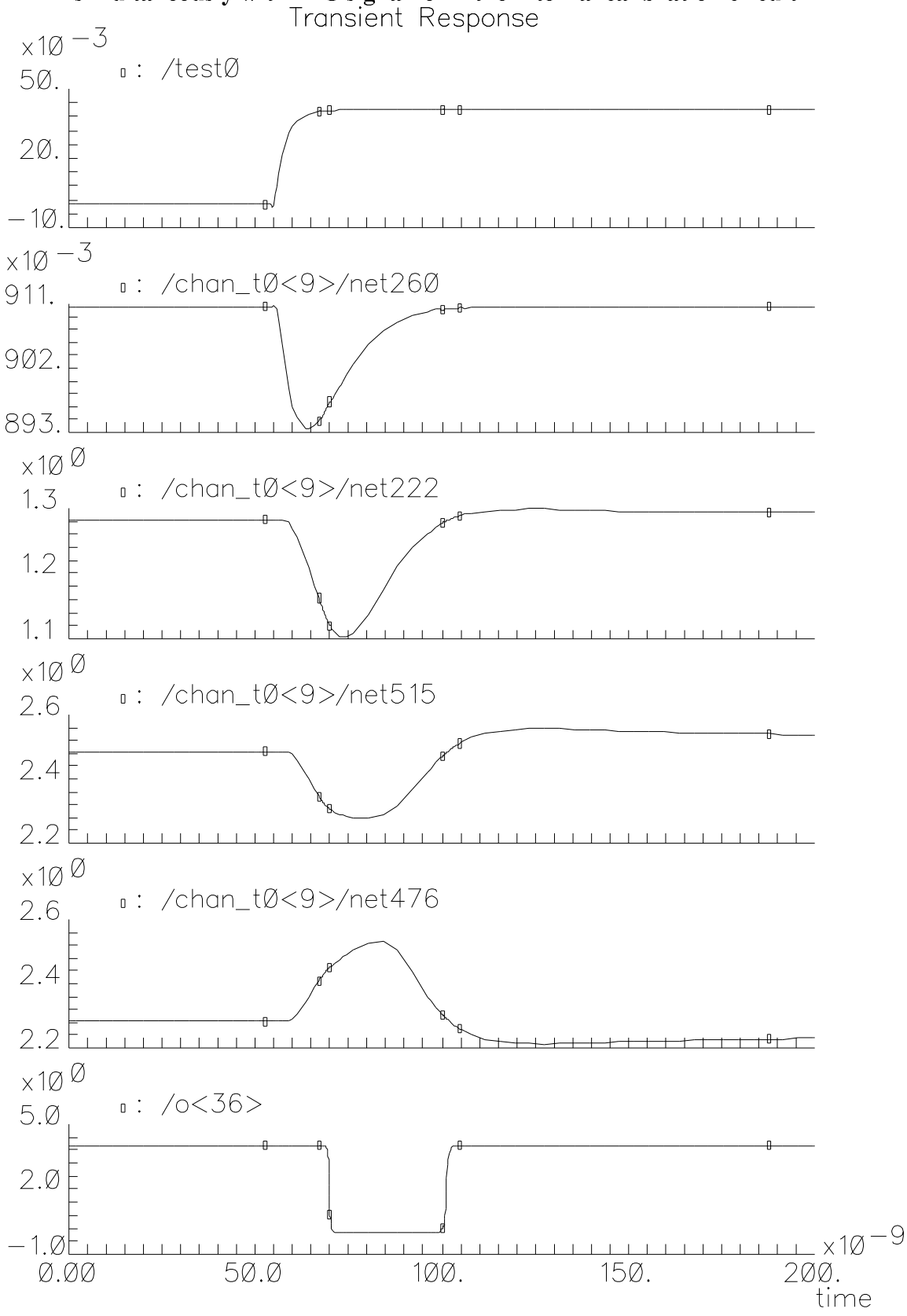
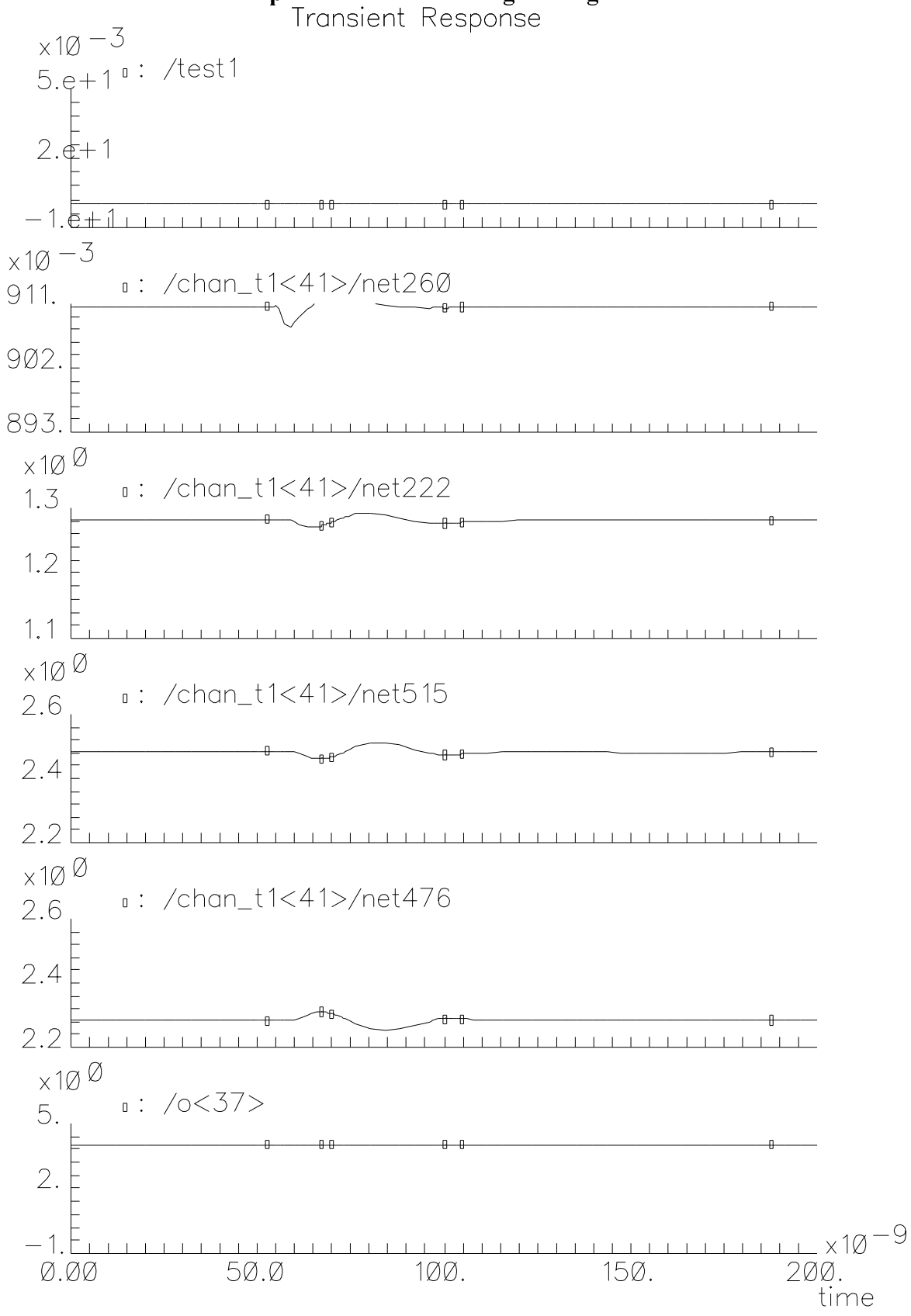
A11: Power supply rejection ratio; TRAN analysis,
40 MHz, 20 mV pp signal on VCC



A12: Power supply rejection ratio; TRAN analysis,
100 kHz, 200 mV pp signal on VCC



B1: Transient response of one stimulated channel while 32 channels stimulated simultaneously with 4 fC signal form the internal calibration circuit



B2: Transient response of a channel neigbouring to the stimulated one