# ABCD2T/NT DAC architecture (3.12.98)

The ABCD2T/NT chip incorporates a new implementation of the Digital to Analogue Converters. Figure 1 shows the schematic diagram of the voltage reference used in the Bias DAC. Figure 2 to 4 show the architecture and the electrical diagrams of the Threshold, Calibration and Bias DAC's. The schematic diagram of the DAC memory cells is shown in Figure 5.

The reference current obtained in the voltage reference is scaled using PMOS current mirrors and switched in between the output reference current line or to the gnd depending on actual DAC setting.

It is an important difference with respect to the architecture applied in the old design where we had switched "on" or "off" the PMOS transistors in the current mirrors which results in different bias condition under irradiation of those transistors. The differences between Vt shifts of the irradiated PMOS transistors were in the range of 50mV after 1 MRad (depending on whether the transistor was "on" or "off") which basically killed the functionality of the old DAC's after the irradiation.

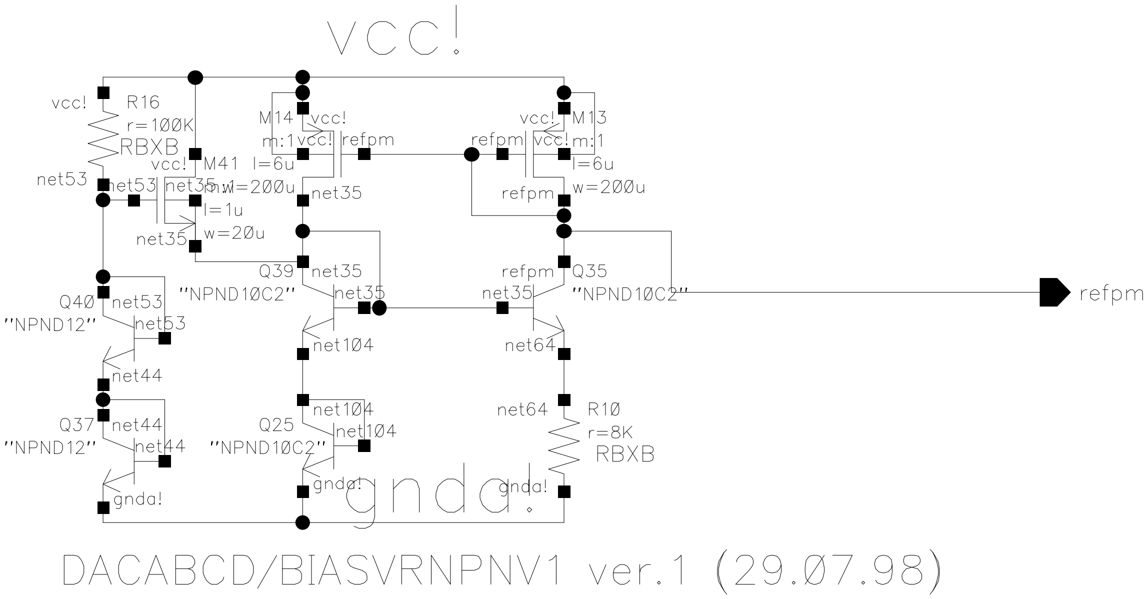


Fig.1 Schematic diagram of the voltage reference.

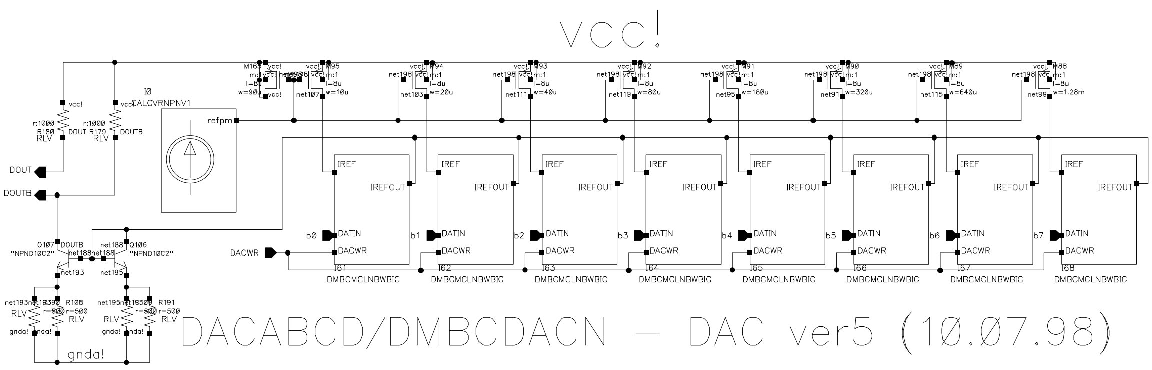


Fig.2 Schematic diagram of the threshold DAC.

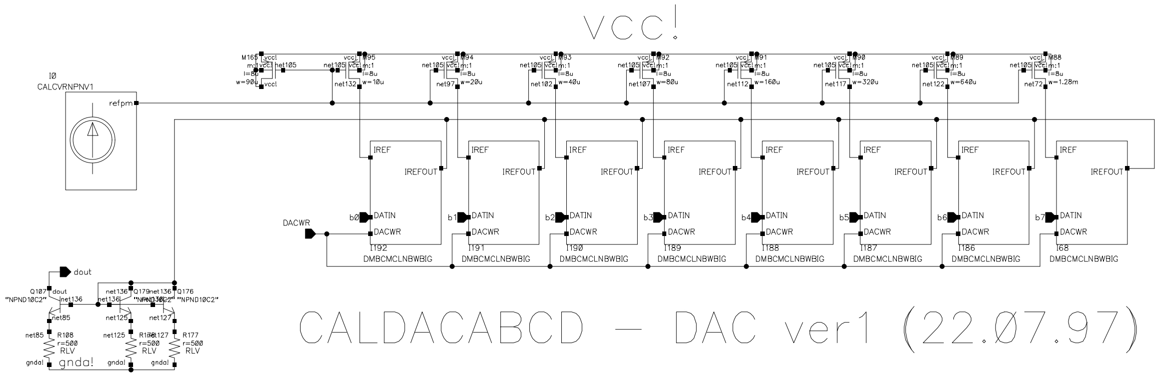


Fig.3 Schematic diagram of the Calibration DAC.

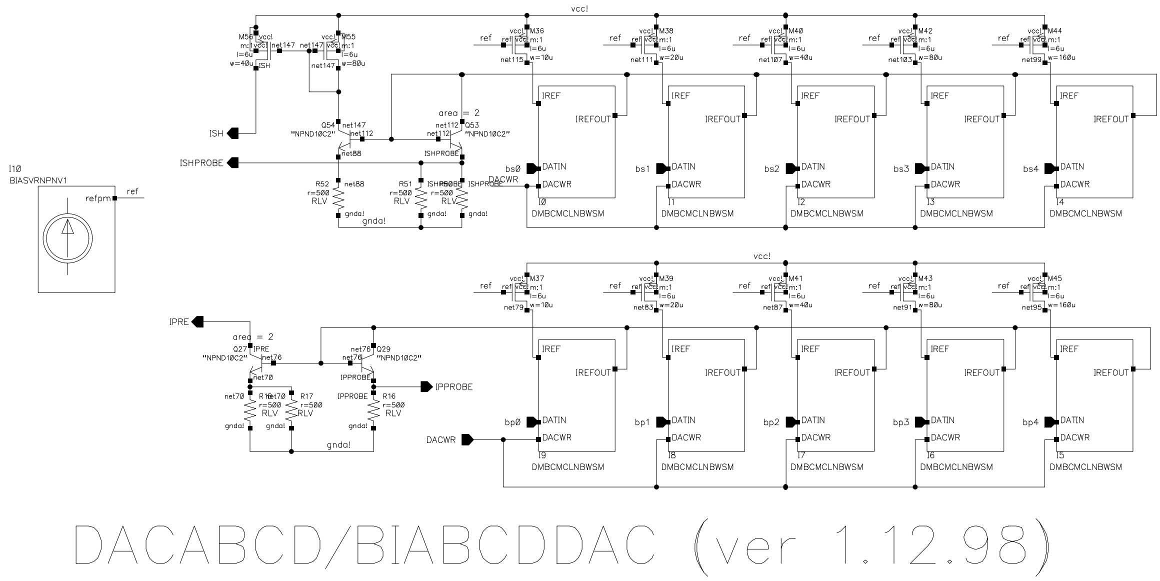


Fig.4 Schematic diagram of the Bias DAC.

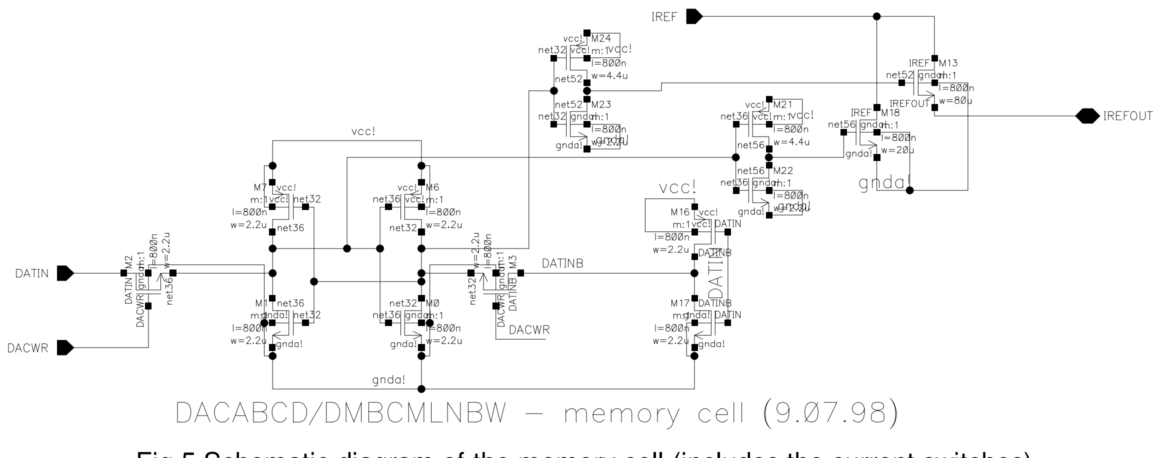


Fig.5 Schematic diagram of the memory cell (includes the current switches)

The new DAC architecture has been prototyped in the SCTA128HC/LC chip (analogue version of the read-out chip in DMILL technology) and tested up to 5MRad. Figures 6 to 7 show the

transfer characteristic and the linearity error of the preamplifier bias DAC before and after irradiation.
The DAC range and the nonlinearity error remain the same after 5MRad of X-Ray irradiation.

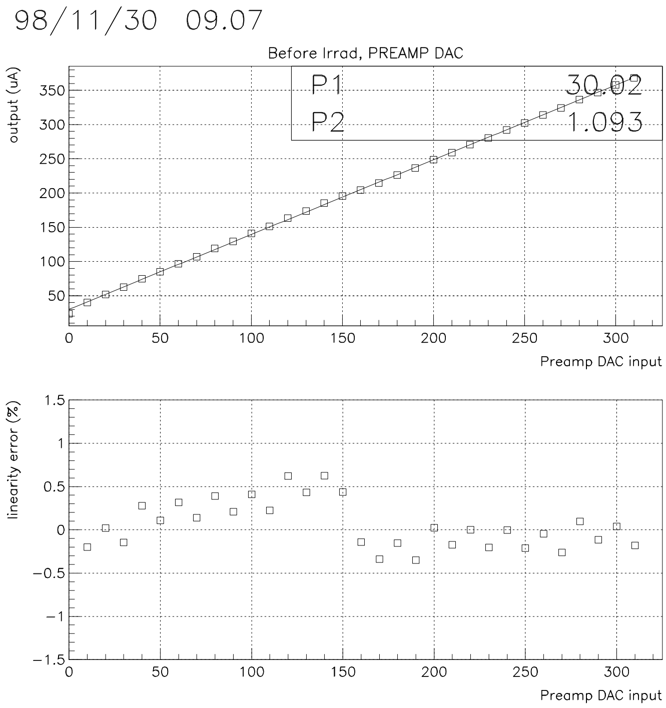


Fig.6 Preamplifier Bias DAC performance before irradiation.

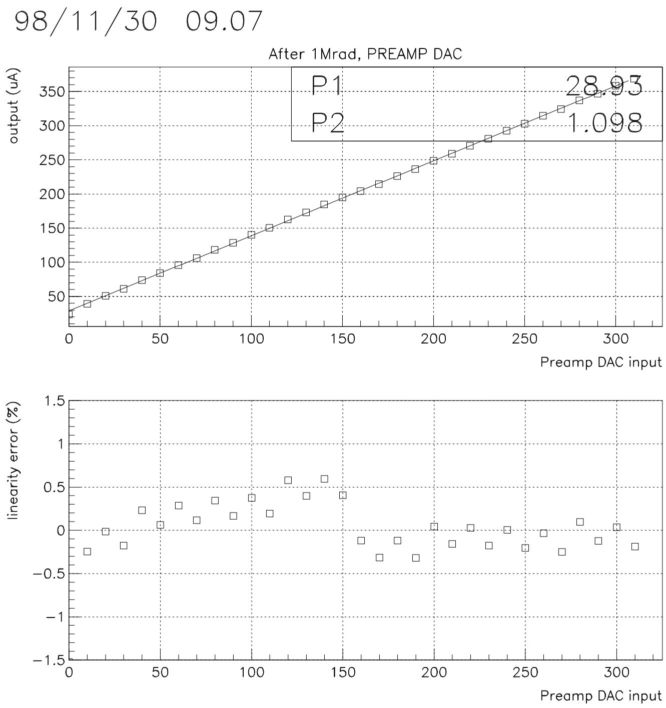


Fig.7 Preamplifier Bias DAC performance after 1Mrad.

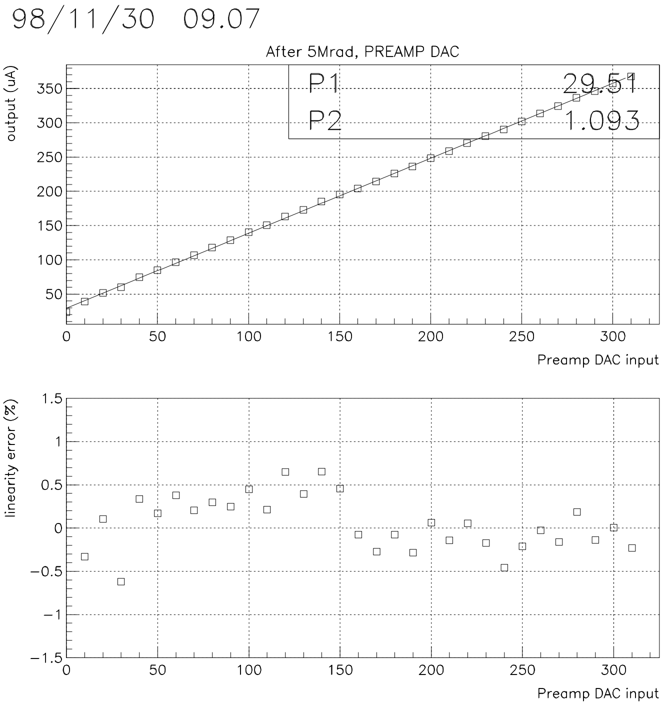


Fig.8 Preamplifier Bias DAC performance after 5Mrad.

Switching the currents instead of the voltages in the present design could have important consequences in the performance of the DACs for low voltage power supply (linearity).
In order to obtain a good linearity for wide range of the power supply voltages (starting from 3V) and corner parameters (temperature 0 & 40C, resistors ±25%, corner CMOS model parameters) it was necessary to optimise the size of the NMOS transistor used as a current switch.
Figure 9 shows the result of DC simulation of the Threshold DAC loaded with the maximum value (maximum current flowing in the switch) performed for three different temperatures.
A good linearity has been achieved starting from 3V power supply, worst case CMOS model parameters (PSET=5 means slow NMOS & slow PMOS after irradiation) and post radiation bipolar transistor model.

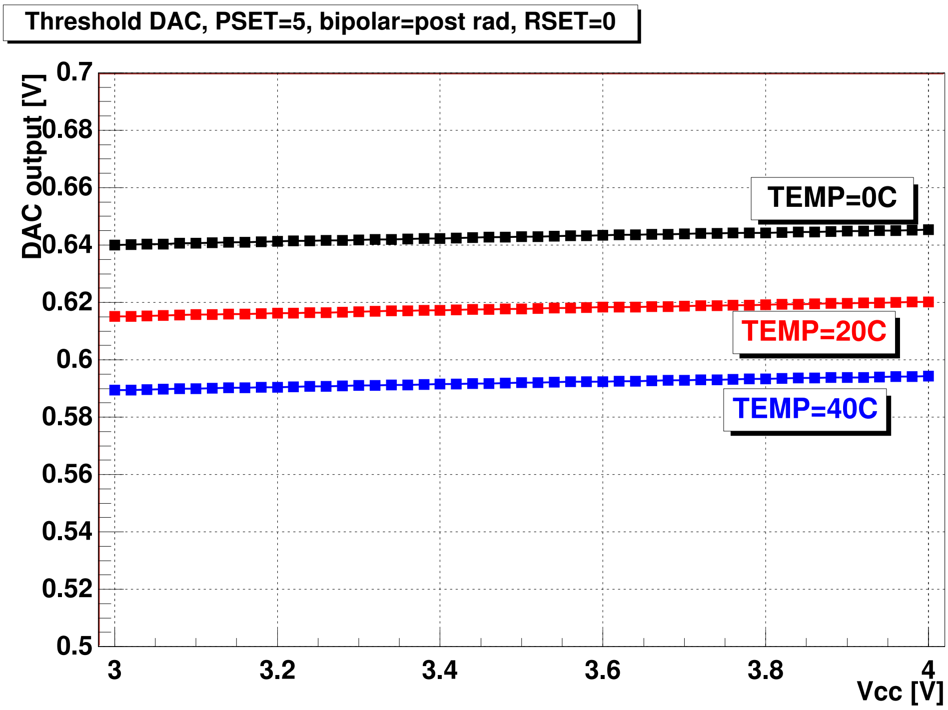


Fig.9 Result of DC simulation of the Threshold DAC loaded with maximum value.

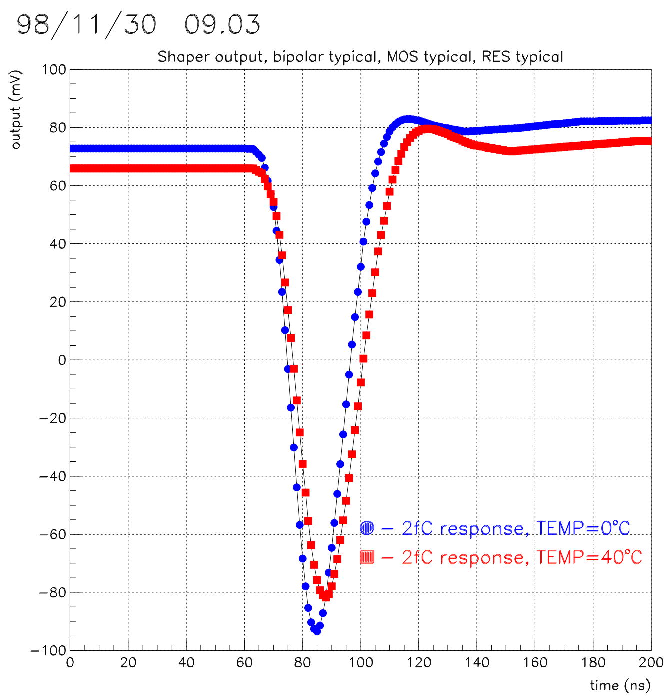


Fig.10 Thermal drift of the FE amplifier gain

The PSRR extracted from the presented figure is in the range of 40dB. One can notice the temperature dependence of the DAC value which is due to the implemented architecture of the voltage reference. The thermal drift of the threshold DAC is in the range of 2%/-10C.

Figure 10 shows the simulated response of the FE amplifier for an injected 2fC pulse and for two different values of the temperature. One can see that the thermal drift of the amplifier gain is partially compensated by the drift of the threshold DAC (baseline shift).

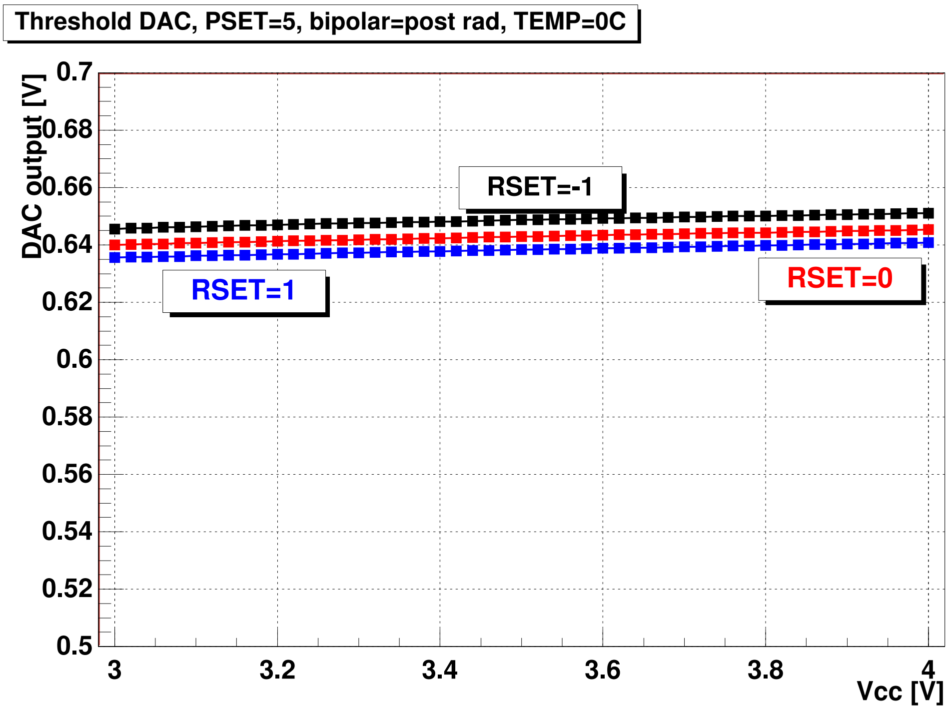


Fig.11 Result of DC simulation of the Threshold DAC loaded with maximum value.

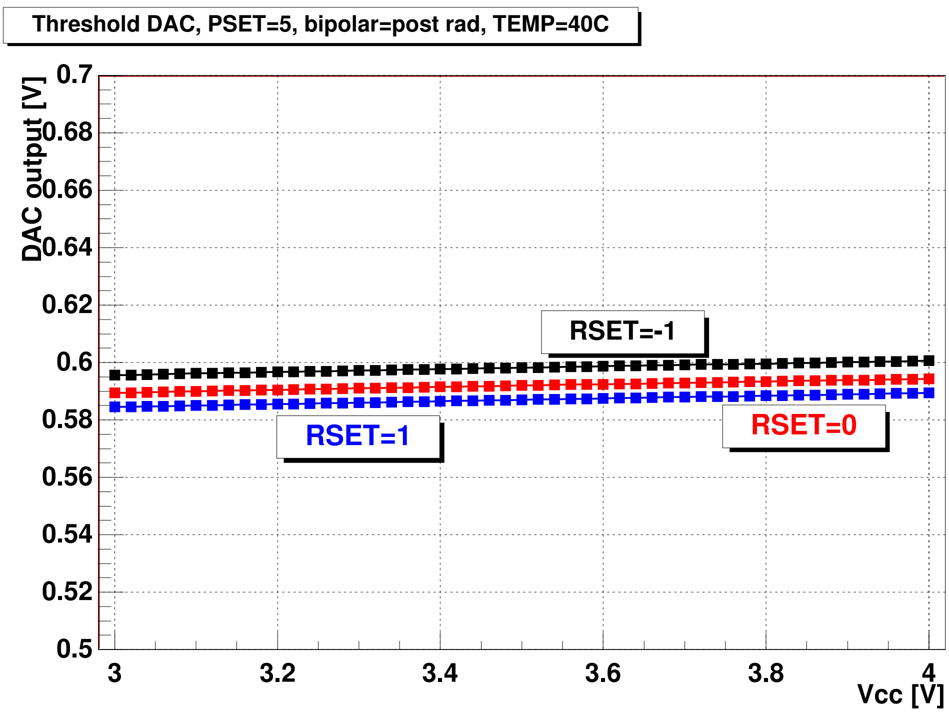


Fig.12 Result of DC simulation of the Threshold DAC loaded with maximum value.

Figure 11 and 12 shows the results of the DC simulation done for different temperatures and different corner values of the resistors (RSET parameter).
One can extract the sensitivity of the threshold due to the RSET parameter as a ±0.8% maximum.

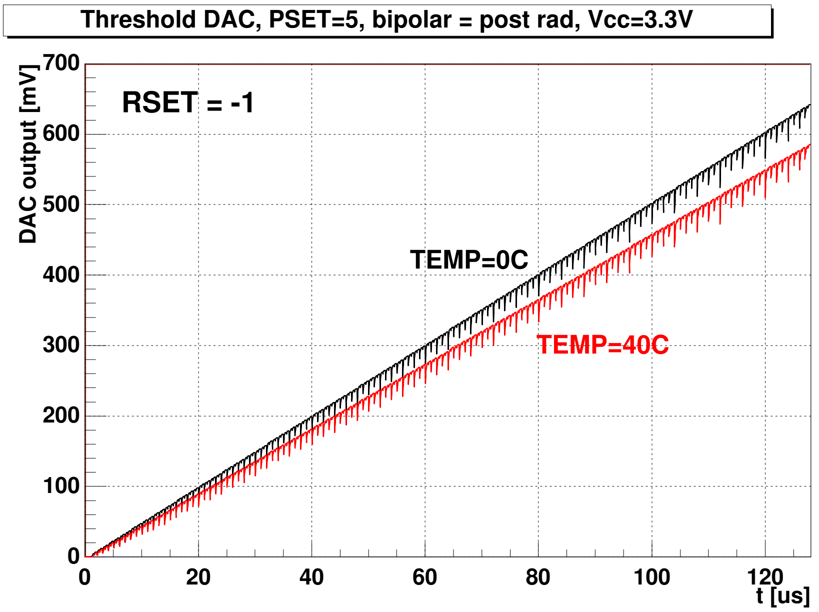


Fig.13 Result of transient simulation of the Threshold DAC. The DAC value is incremented across the whole range.

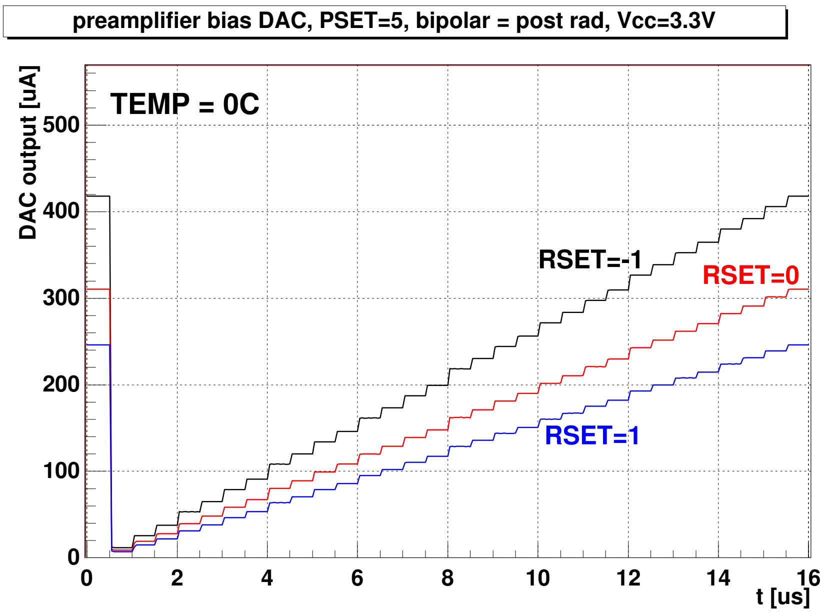


Fig.14(a) Results of transient simulation of the preamplifier Bias DAC. The DAC value is incremented across the whole range.

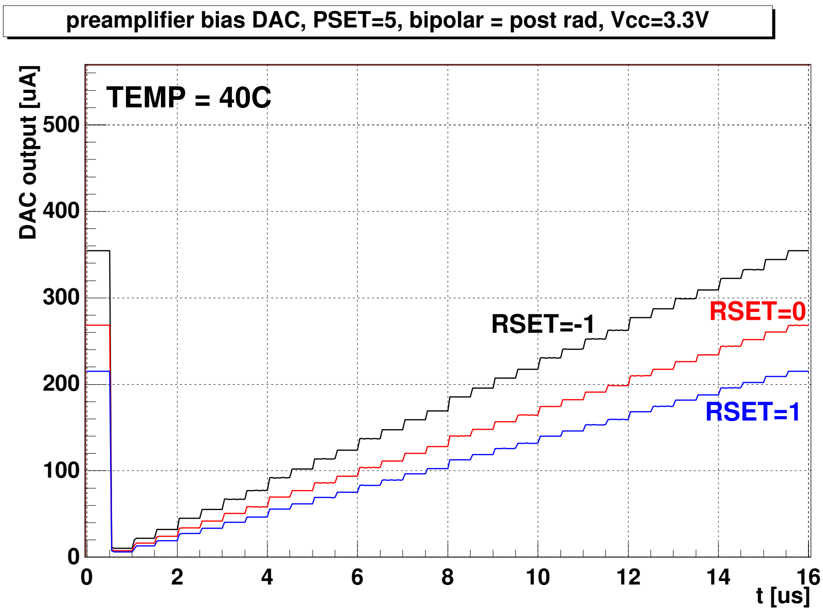


Fig.14(b) Results of transient simulation of the preamplifier Bias DAC. The DAC value is incremented across the whole range.

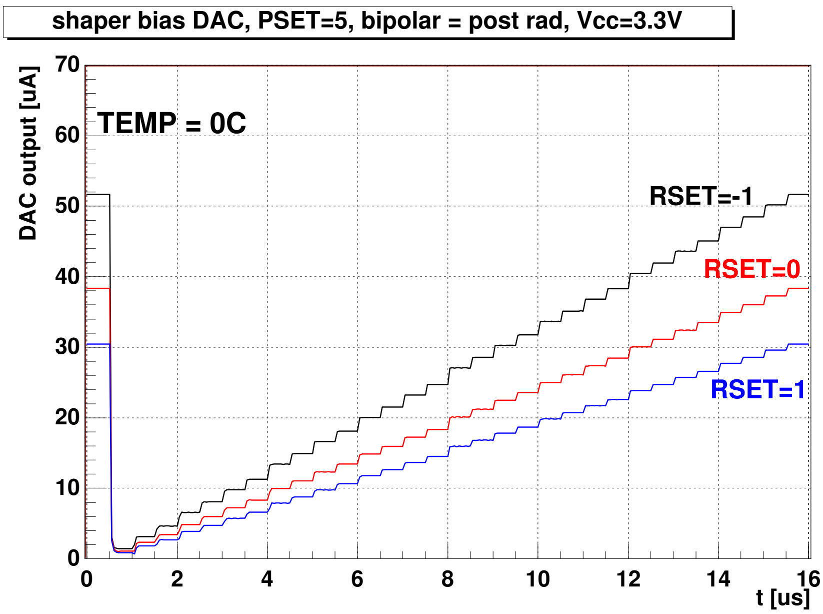


Fig.15(a) Results of transient simulation of the shaper Bias DAC. The DAC value is incremented across the whole range

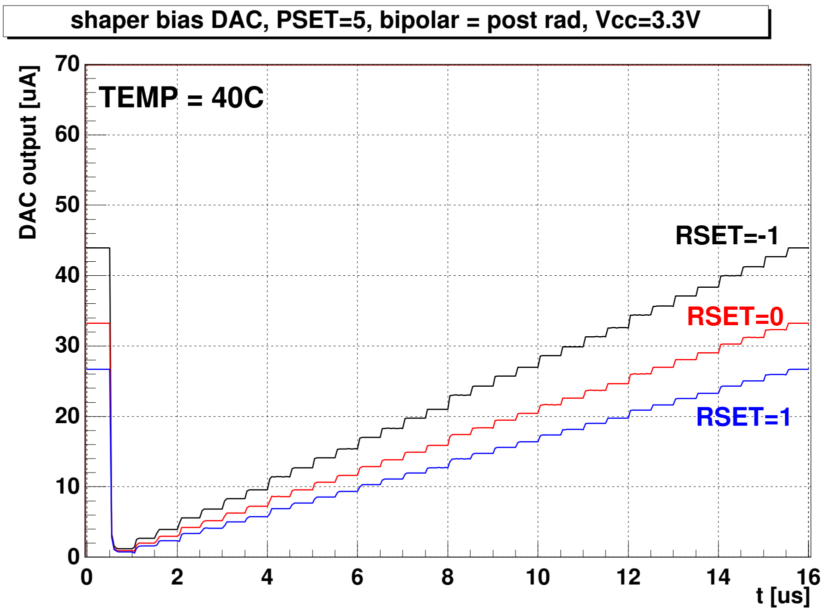


Fig.15(b) Results of transient simulation of the shaper Bias DAC. The DAC value is incremented across the whole range

Figures 13-15 show the result of transient simulation done for the worst corner of resistor, CMOS and bipolar parameters. The DAC value was incremented every 0.5us starting from 0 to the maximum value. The width of the WRITE pulse was 5ns (nominal 25ns) and the power supply was set for 3.3V.