Project Specification
Project Name: CAFE-M
Version: V3.01

1. Scope:

Establish the requirements and the target design specifications for the Front-end Bipolar Amplifier/Discriminator Integrated Circuit to be used as part of the Binary Readout of the ATLAS Semi-Conductor Tracker (SCT). This design is based upon previous work, in particular TekZ IC used in the DESY ZEUS experiment, the FABRIC IC used in the CERN NA50 experiment and the LBIC and CAFE prototype ICs.

2. Reference Documents:

1) Specification for the Atlas Binary Chip (ABC), 1996.
2) I. Kipnis, "CAFE: A complementary Bipolar Analog Front End Integrated Circuit for the ATLAS SCT", 1995.
3) E. Spencer, et al., "A Fast Shaping Low Power Amplifier-Comparator Integrated for Silicon Strip Detectors", IEEE Nuclear Science Symposium, 1994, (SCIPP 94/32)
4) W. Dabrowski, et al., "Fast Bipolar Front-end for Binary Readout of Silicon Strip Detectors", Nuclear Instruments and Methods A 350 (1994), 548
5) I. Kipnis, et al., "An Analog Front-end Bipolar-transistor Integrated Circuit for the SDC Silicon Tracker," IEEE Transactions on Nuclear Science, vol. 41, no. 4, (1994), 1095-1103.
6) E. Barberis, et al., "A Fast Shaping Amplifier-Comparator Integrated Circuit for Silicon Strip Detectors", IEEE Nuclear Science Symposium, 1992, (SCIPP 92/40)
7) "Silicon Tracker Conceptual Design Report", SCIPP 92/04.
8) H. Spieler, "Electronics Baseline Specification - Recap and Postscript", Minutes of SDC Silicon Tracker Meeting at LBL, 16-Dec-92.
9) J. Leslie, A. Seiden, Y. Unno, "Signal Simulations for Double-sided Silicon Strip Detectors", SCIPP 92/20.
10) H. Spieler, "Rate of Noise Hits in Threshold Discriminator Systems", unpublished note.
11) H. Spieler, "Some Comments on Specifications for Front-End Electronics in the SDC Silicon Tracker", unpublished note.

3. Technical Aspects:

3.1 Requirements

3.1.1 An Integrated Circuit (IC) to process signals from 128 n-type strips of a Silicon Micro-strip Detector. An outline schematic of the IC is shown in Figure 1.

3.1.2 Signal Processing (See block diagram in Figure 2):

The IC must contain the following functions:

Charge integration
Pulse shaping
Threshold/timing discrimination

The result of the discrimination function, indicating a "hit" or "no hit" for each strip, is output from this IC to another circuit for further digital processing. This IC will have one independent channel to process signals from each silicon strip of the detector. Signals from each detector strip will be received at single-ended Sensor

Input pads IN0..INn and results appear at single-ended Output pads OUT0..OUTn. Two reference current outputs OUTRH and OUTRL are provided as well as a ground return DRET for the output current.

A control input (VISET) is provided to set the operating current of the input transistor.

The threshold value is provided either as a differential voltage from an external source (VTHP, VTHN) or as a programmable current from the adjoining digital processing IC (ITH) as selected by the pad VTSEL. See 3.2.3.7 for more details.

3.1.3 Compatibility:

The design of this IC and that of the digital processing IC, ABC, must be compatible so that they can work together as a chip set. This compatibility of design includes the interface circuits (128 data signals with references, the calibration and threshold controls and the DAC reference) and the corresponding bonding pad locations.

3.1.4 Calibration Circuitry (See block diagram in Figure 3):

Each channel will have an internal Calibration Capacitor connected to its input for purposes of simulating a "hit" strip. The Calibration Capacitors will be charged by a chopper circuit which is triggered by an independent differential input Calibration Strobe (CALSP, CALSN). Every fourth channel can be tested simultaneously with group selection determined by two binary coded Calibration Address inputs (CALD0, CALD1). These strobe and selection signals are expected to originate in the accompanying digital processing IC which is acting on commands from the experiments control system. The voltage applied to the Calibration Capacitors by the chopper is determined by a single differential DC Calibration Level input voltage (CALVP, CALVN) or as a single programmable current from the adjoining digital processing IC (CALI). See 3.2.3.9 for more details. The four calibration bus lines, each of which connects the calibration capacitors of every fourth channel, are also brought out to pads on each side of the IC (CBUS0, CBUS1, CBUS2, CBUS3) which can be directly driven with an AC coupled voltage step. This is intended for use during IC testing.

3.1.5 DAC Reference Circuit (See block diagram in Figure 4):

The adjoining digital processing IC will contain digital-to-analogue converters (DACs) to supply programming currents for the Comparator Threshold and the Calibration Level. It is assumed that these DACs will scale down a reference current supplied by this bipolar IC according to values programmed via commands from off-detector. One reference current will be generated via a band-gap reference circuit. The derived reference current and the voltages derived from the returned currents programmed by the DACs will depend upon resistors on this bipolar chip in order to maintain process independent scaling.

3.2. Specification of Deliverables:

3.2.1 Physical Requirements:

Number of amp/comparator channels per IC: 128

Physical Layout: See Figure 5.

Pad Layout:

Sensor Inputs on front edge.
Comparator Outputs on back edge
Service (power, ground, references) on side edge (reflected on both sides)
Threshold Inputs on back edge (current mode, including reference current)
and also on side edge (differential voltage mode, reflected on both sides)
Calibration Strobe & Address Inputs on back edge near corners
Calibration Amplitude Inputs on back edge (current mode)
and also on side edge (differential voltage mode, reflected on both sides)
Output logic high and low reference current on back edge

Sensor Input Pad Pitch: = 48 μm, 2 rows @ 96 μm pitch each offset at 48 μm to each other

Output Pad Pitch: = 44 μm, 2 rows @ 88 μm pitch each offset at 44 μm
Note that an alternative output pad arrangement is under consideration in order to allow the ABC chip to be kept to its minimum width. This arrangement would use 3 rows of pads @ roughly 96 μm pitch each.

Pad Size (nominal):

Sensor Inputs:	140 x 60 μm
Outputs:	140 x 60 μm
Service: (Vcc, GND)	190 x 92 μm
(Other Service on side edge)	92 x 92 μm
Service on front and back edge:	140 x 60 μm

Total Chip Width: $\geq$ 6.4 mm, $\leq$ 6.6 mm after sawing and including all bond pads.

Total Chip Length: $\geq$ 3.8 mm, $\leq$ 4.5 after sawing and including all bond pads. (Minimize total area to improve cost.)

Channels must be laid out in parallel to meet electrical requirements.

Services like power, ground and voltage references must be bussed across chip with pads on both sides to allow bonding on either side. The SSGND pads must be bonded on both sides of the IC to equalize voltage drop across the IC. It would ease the IC layout if the services were required to be bonded on both sides rather than on either side. This should be studied further with the hybrid designers.

Critical service pads (e.g. Vcc, GND) are made double width to allow double wire bond for improved reliability.

3.2.2 Assumed Detector Electrical Characteristics at Input to this IC from n-type 12 cm long strips:

	Unirradiated	Irradiated
Coupling type to amplifier	AC	AC
Coupling capacitance to amp Total for 12 cm strips	20 pF/cm 240 pF	20 pF/cm 240 pF
Capacitance of strip to all neighbor strips	1.22 pF/cm	0.92 pF/cm
Capacitance of strip to backplane	0.28 pF/cm	0.28 pF/cm
Metal strip resistance	20 Ω/cm	20 Ω/cm
Bias Resistor	0.75 MΩ	0.75 MΩ
Max leakage current per strip for shot noise {estimated}	2.0 nA	2.0 μA

AC characteristics for the detector signal are shown in Figure 6 and Table 3 for an irradiated n-strip detector. For an unirradiated detector, the pulse shape will be slightly narrower.

3.2.3 Electrical Requirements:

Note that notation convention for currents used in the entire specification is "+" for current going into (sunk by) the chip and "-" for current going out of (sourced from) the chip.

3.2.3.1 Sensor Input Characteristics:

Input Signal Polarity: Negative signals from n strips.

Crosstalk: < 5% (with detector)

Input Protection: Must sustain voltage step of 300 V of either polarity with a cumulative charge of 5 nC in 15 ns.

Open Inputs: Any signal input can be open without affecting performance of other channels.

Max Parasitic Leakage Current: 100 nA DC per channel with < 10 % change in gain at 1 fC input charge.

3.2.3.2 Calibration Input Characteristics:

The digital signal processing IC, ABC, must provide the following inputs for the Calibration Circuit. See 3.2.3.9 for functional specifications of the Calibration Circuit.

Two single ended logic inputs CALD1, CALD0 to select one of four groups of channels to test.

	Min	Nominal	Max
"1" State Level	2.9 V	4 V	4.2 V
"0" State Level	0 V	0 V	0.5 V
Current			100 µA
Rise Time			10 ns
Duration		DC	

One pair of Calibration Strobe inputs CALSP, CALSN which form one signal to activate the Calibration circuitry. The CALSP input is normally in the "Off" state and the CALSN input is normally in the "On" state when the Calibration Strobe is idle. During an active Calibration Strobe, CALSP goes to the "On" state and CALSN goes to the "Off" state. It is expected that these inputs are driven by a complementary driver:

	Min	Nominal	Max
"On" State Current at 0.7 V Nom (each input)	- 180 µA	- 240 µA	- 300 µA
"Off" State Current	- 15 µA		- 30 µA
Voltage Range (either state)	Vcc-0.9V		Vcc-0.6V
Rise Time			2 ns
Duration	125 ns		
Delay after transition of CALD1,CALD0	250 ns		
Off interval between consecutive pulses	250 ns		

Calibration Level: See DC Supply and Control Characteristics

3.2.3.3 DC Supply and Control Characteristics:

The following DC inputs are required for 128 channels with voltage specifications listed on this page and current specifications on the following page. Differential pairs are grouped together.

		Operational Values			Absolute
	Pad Name	Min	Nominal	Max	Max
Circuit Supply	Vcc	3.325 V	3.5 V	3.675 V	0 to 6 V
Preamp Current Control	VISET	0 V	1 V	2 V (off)	Vcc
Small Signal Ground	SSGND		0 V		
Circuit Ground	GND		0 V		
Digital Ground Return	DRET	-100 mV	0 V	100 mV	-500 mV
Comparator (voltage) Threshold	VTHP	3.1 V	Vcc	Vcc+.3V	Vcc+.5V
	VTHN		VTHP-.2V		Vcc+.5V
(Vthp - Vthn)			0.2 V	0.9 V	0 to 2 V
Comparator (current) Threshold	ITH	Vcc - 1.2 V			Vcc
Threshold Select (for voltage mode)	VTSEL	Vcc - 0.5 V		Vcc	Vcc
Calibration (voltage) Level (diff. pair)	CALVP	1.2 V		2.8 V	Vcc
	CALVN	1.2 V		2.8 V	Vcc
(CALVP - CALVN)		50 mV		1 V	2.0 V
(Equiv. Charge)		(.5 fC)		(10 fC)	
Calibration (current) Level	CALI	1.0 V		2.4 V	Vcc
DAC Reference Current	IDAR	1.8 V			Vcc

Special Requirements
(Not design targets but simulation results of the completed circuit):

Gain Sensitivity to Vcc for 1 fC signal — See Figure 7

Power Supply Rejection Ratio at:

10 Hz - 100 Hz	50 dB
100 kHz - 300 kHz	-3 dB
10 MHz - 60 MHz	-24 dB

The current draw at each DC input is as follows. Maximums assume -20 % resistor production skew.

		Min	Nominal	Max
Circuit Supply	Vcc			
For I(Vi1)=150 µA			45 mA	51 mA
For I(Vi1)=300 µA			67 mA	73 mA
Preamp Current Control	VISET		.15 to .3 mA	.5 mA
Small Signal Ground	SSGND			
For I(Vi1)=150 µA			23 mA	23 mA
For I(Vi1)=300 µA			45 mA	45 mA
Circuit Ground	GND		22 mA	27 mA
Digital Ground Return	DRET		1 mA	
Comparator (voltage) Threshold	VTHP		12 µA	15 µA
	VTHN		12 µA	15 µA
Current Balance	|I of VTHP - I of VTHN|			
Comparator (current) Threshold	ITH	- 3 µA		- IDAR
Threshold Select	VTSEL		50 µA	60 µA
Calibration (voltage) Level	CALVP			1 µA
	CALVN			1 µA
Current Balance	|I of CALVP - I of CALVN|			10 %
Calibration (current) Level	CALI	+ 15 µA		IDAR
(Equiv. Charge)		(.5 fC)		(10 fC)
DAC Reference Current	IDAR		+ 324 µA	+ 363 µA

3.2.3.4 Signal Output Characteristics:

Assumed type of logic of receiving stage: edge triggered

Output configuration: open collector output of npn transistor as a current source.

	Min	Nominal	Max
"Off" State Current	0 μA		10 μA
"On" State Current	130 μA	200 μA	300 μA
Pulse Duration			
for 1.25 fC	8 ns		
for 3.50 fC			44 ns

Open Outputs: Any signal output can be open without affecting performance of other channels.

Output Reference pad named OUTRH: DC current equal to that of "On" state of normal outputs.

Output Reference pad named OUTRL: DC current equal to that of "Off" state of normal outputs.

3.2.3.5 Power Dissipation:

Power use will be minimized for this design.

Average Power: <= 1.8 mW for one bipolar channel, for VISET at 300 μA and nominal fabrication processing parameters.

Total Average Power: <= 275 mW for VISET at 300 μA and -20 % resistor production skew. {This is an over estimate which will be adjusted later.}

3.2.3.6 Noise:

Maximum rms. noise for nominal components including contributions from:
a) All detector parameters listed in 3.2.2
b) Two neighboring channels (one on each side): 3 channel simulation will be: <= 1400 electrons for unirradiated module
<= 1500 electrons for irradiated module

Noise analysis predicated on worst case n-strip signal (WNS) as shown from simulation of depleted detector n-strip signal in Figure 6 and Table 3 assuming the front-end ICs are wire bonded at the center of the 12 cm detector strips.

3.2.3.7 Comparator Stage:

A threshold is applied as a voltage offset to the comparator stage.

Threshold setting range: 0.5 fC to 5 fC, nominal 1 fC

This threshold voltage is applied externally either as a differential voltage or as a current. The unused inputs must be left floating. A pad VTSEL on the side of the chip must be bonded to Vcc to use the voltage mode or left floating to use the current mode.

For voltage mode, typical externally applied differential threshold voltage to establish nominal threshold of 1 fC: ~ 190 mV (150 mV/fC + offset)

For current mode, a reference current (IDAR) is sunk as output expecting a programmable scaled current supplied as a threshold input (ITH). It is expected that the reference current will be scaled into 256 programmable linear steps to provide the necessary precision. Resulting step size near 1 fC threshold should correspond to ~0.025 fC of input charge. Typical externally supplied current to establish nominal threshold of 1 fC: ~ 60 μA.

Threshold variation at 1 fC:
4% (1 sigma) channel to channel matching within one chip
20% (1 sigma) including all process variations

3.2.3.8 Timing Requirements:

Timewalk: <= 16 ns. This specification depends on the precision of the digital acquisition latch edge. Good alignment, 1 or 2 ns over a common clocked array of channels implies a longer timewalk assignment to the rising edge of the shaped signal.

Timewalk defined: The maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 to 10 fC, with the comparator threshold set to 1 fC according to 3.2.3.7.

Double Pulse Resolution: <= 50 ns for a 3.5 fC signal followed by a 3.5 fC signal, including a 6 ns off state of Output between pulses.

Max recovery time for a 3.5 fC signal following a 80 fC signal: 1 μs

3.2.3.9 Calibration Circuit Characteristics:

Calibration Capacitors: 100 fF +- 20% (3 sigma) over full production skew
+- 2% (3 sigma) within one chip

Absolute accuracy of voltage step applied to capacitors: 5% (full process skew)

Relative accuracy of voltage step: < 2 %
(for known values of calibration capacitors, amplitude range 0.8 to 4 fC, across one chip, including non-linearity of differential receiver, switching pickup, etc.)

Relative accuracy of voltage step: < 10 %
(for known values of calibration capacitors, amplitude range 0.8 to 8 fC, across one chip, including non-linearity of differential receiver, switching pickup, etc.)

Calibration circuit must be laid out such that Calibration Strobe signal pickup at comparator will be less than 0.3 fC equivalent sensor input.

The calibration amplitude is established externally either as a differential voltage or as a current. The unused inputs can be left floating or grounded

For voltage mode, typical externally applied differential voltage will correspond linearly to roughly 100 mV/fC of equivalent input charge up to 1 V

For current mode, the same reference current (IDAR) used for threshold control will be available expecting a programmable scaled current supplied as a calibration level input (CALI). It is expected that the reference current will be scaled into 256 programmable linear steps to provide the necessary precision. Typical externally supplied current will correspond linearly to roughly 30 μA/fC of equivalent input charge up to 300 μA. Linearity will be < 1 % in the range 0.5 fC to 2 fC and < 4 % in the range 2 fC to 10 fC.

For test purposes, a voltage step can be applied directly to any one of the four groups of calibration capacitor via the input pads (CBUS0, CBUS1, CBUS2, CBUS3). Such an external voltage step must be AC coupled. When not used, these four pads must be left floating.

4. Quality Assurance:

4.1 Specification Review:

This specification and all revisions will be approved by the selected Review Committee for appropriateness to meet the goals of the detector and integratability with the rest of the subsystem.

4.2 Circuit Simulations:

The design will be simulated to test fulfillment of these requirements before submission to fabrication.

Transient analyses will be performed in which all DC supplies are cycled in random order to verify that no latch up occurs in the circuit.

Behavior will be simulated for variations in supply voltages 25 mV beyond that specified in section 3.2.3.3. Simulations will be done at temperatures of -10 and 25 degrees centigrade.

DC and AC analysis will be performed for 25% of the channels activated using actual metal busses and expected on-chip and off-chip bus impedances.

Sensitivity analysis will be done for all relative process parameters over 3 standard deviations of the expected fabrication distributions to the satisfaction of the review committee listed in 4.3. Circuit parameters will also be varied to simulate circuit

performance at initial commissioning and after irradiation of $10^{14}/cm^2$ particles including the respective sets of unirradiated and irradiated detector parameters given in section 3.2.2.

In the sensitivity analysis, < 1% of all channels may deviate from the specification.

4.3 Preliminary Design Review:

The design will be checked and simulations reviewed in detail by at least one engineer other than the circuit designer.

A Data Sheet specific to each prototype design must be submitted and include typical operating values, operating limits and absolute maximum values of supply voltages and currents.

The specific data sheet and simulation results will be reviewed by the Selected Review Committee of this specification before submission to fabrication.

4.4 Intermediate Design Review:

Results of prototype circuits including test data will be reviewed by the Review Committee to verify compliance with these requirements.

4.5 Final Design Review:

Before this circuit is submitted for Production Fabrication, a Final Design Review will be held by the Review Committee. The following data will be reviewed including comparisons between different vendors:

Electrical component tests

Electrical tests in assembled modules

Comparisons of tests vs. simulations

Expected yield and performance over process variations from each potential vendor

Reliability data

Irradiation effects

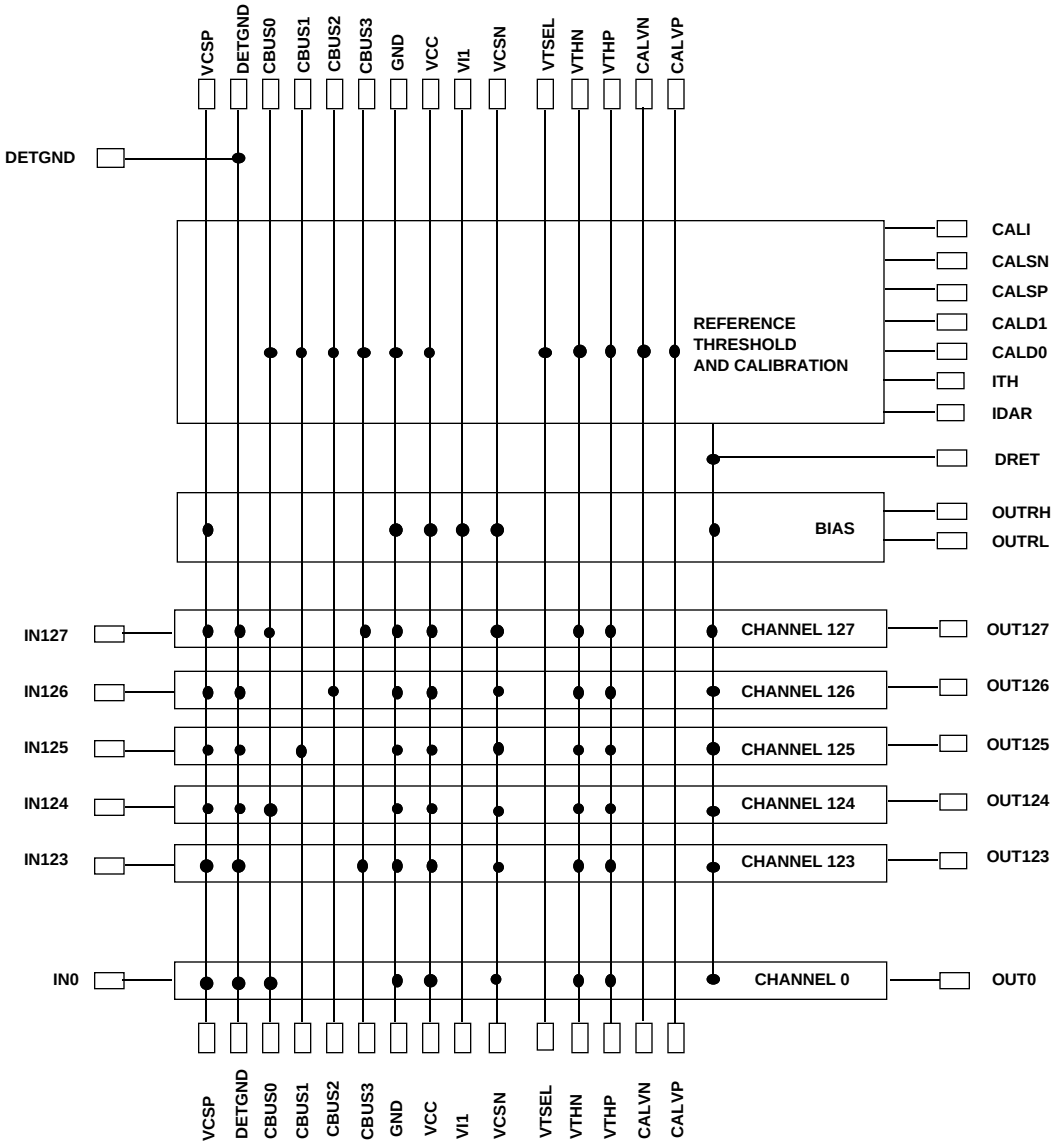

Figure 1: Chip Outline Schematic
Note: This figure shows relationships of input/output signals to circuit blocks and not relative pad positions of the chip layout.

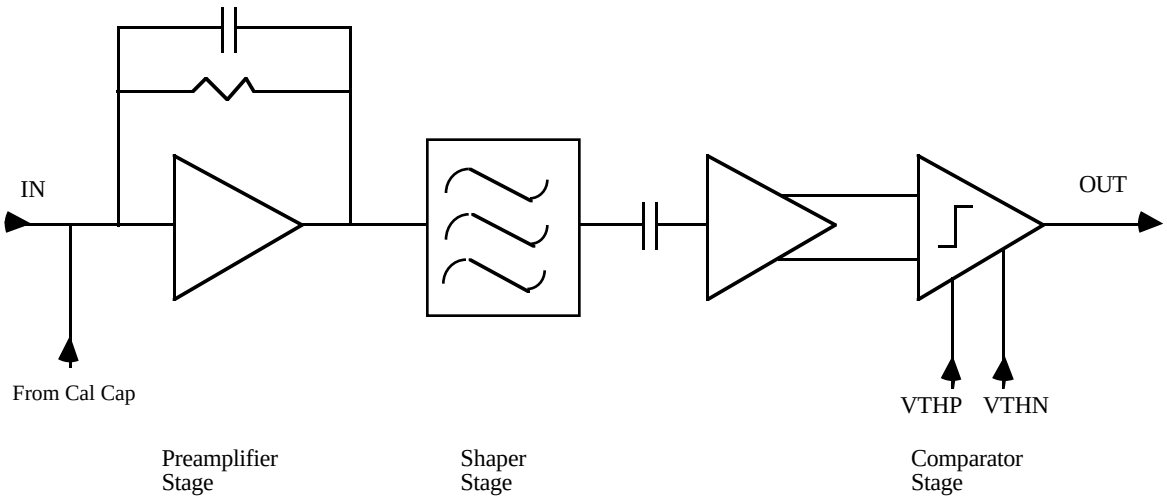

Figure 2: Block Diagram of One Signal Processing Channel

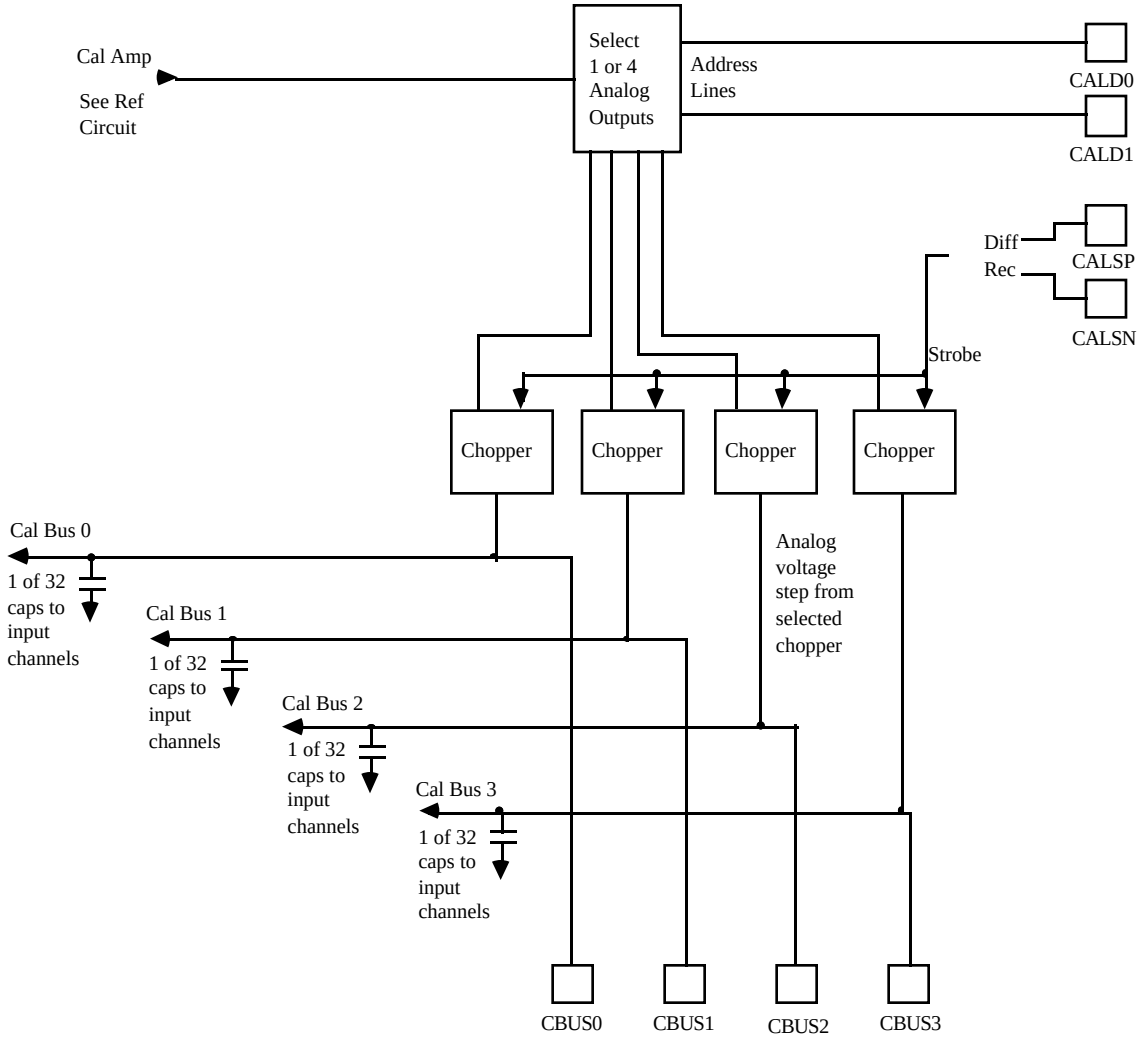

Figure 3: Block Diagram of Calibration Circuitry

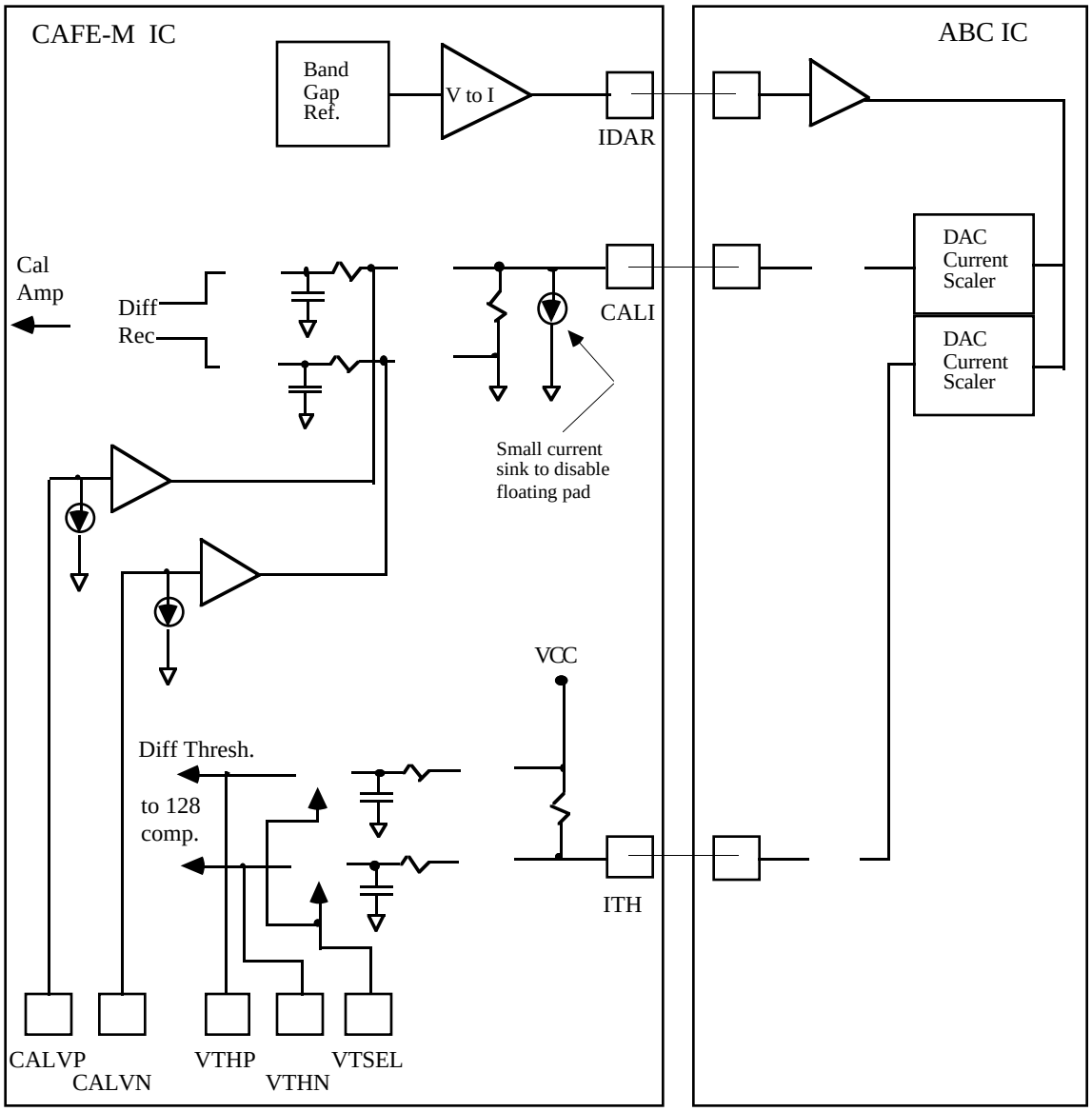

Figure 4: Block Diagram of DAC Reference Circuit

Table 1: Pad List

IN0 .. IN127	128 input data channels
SSGND	Ground of Strip Detector
OUT0 .. OUT127	128 output data channels
OUTRL	Low output reference current
OUTRH	High output reference current
DRET	Ground return to digital processing IC
Vcc	Chip power
GND	Chip ground
VISET	Bias for front-end transistor
VCSP	Internal bias bus for diagnositcs
VCSN	Internal bias bus for diagnostics
IDAR	Reference current for DACs on digital processing IC
ITH	Current mode threshold control
VTHP	High side of differential voltage threshold control
VTHN	Low side of differential voltage threshold control
VTSEL	Threshold control mode selection
CALI	Current mode calibration amplitude control
CALVP	High side of differential voltage calibration amplitude control
CALVN	Low side of differential voltage calibration amplitude control
CALD0	Address 0 for calibration channels
CALD1	Address 1 for calibration channels
CALSP	High side of calibration strobe
CALSN	Low side of calbiration strobe
CBUS0	Calibration Bus #0 for channels 0, 4, .. 124
CBUS1	Calibration Bus #1 for channels 1, 5, .. 125
CBUS2	Calibration Bus #2 for channels 2, 6, .. 126
CBUS3	Calibration Bus #3 for channels 3, 7, .. 127

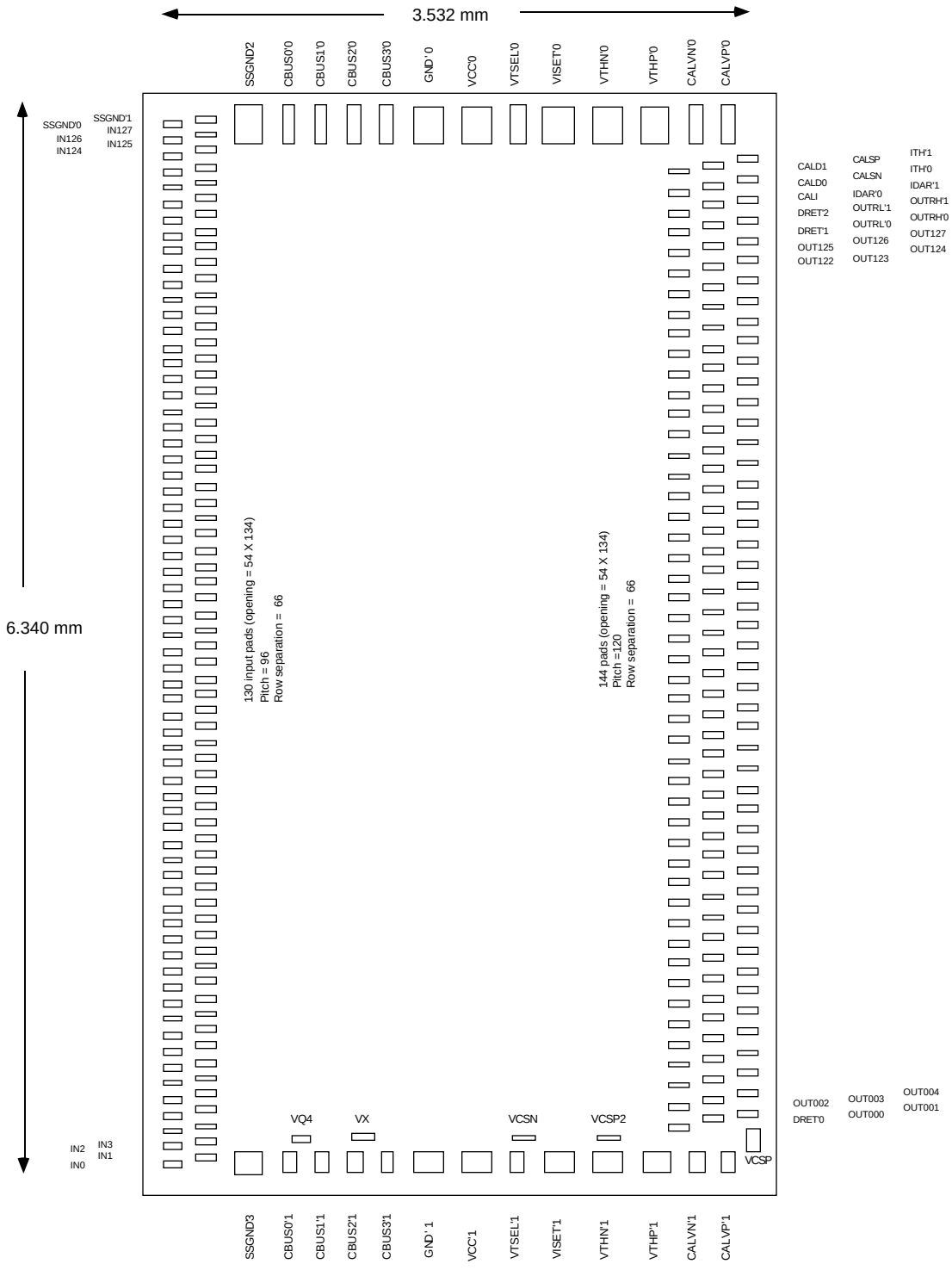

Figure 5: Pad Layout
Overall chip size is extent of digitized area (not including scribe area).
Openings for diagnostic probe points are not all shown.

Table 2: Pad Coordinates and Sizes

X, Y Coordinates refer to layout of Figure 5 with X measuring to the right and Y measuring up. The orgin is at lower left corner edge of digitized area.
Pad sizes are for openings in over glass.

Pad #	Name	X-Center	Y-Center	X-Size	Y-Size
1	IN0	72	64	134	54
2	IN1	272	108	134	54
3	IN2	72	160	134	54
4	IN3	272	204	134	54
5	IN4	72	256	134	54
6	IN5	272	300	134	54
7	IN6	72	352	134	54
8	IN7	272	396	134	54
9	IN8	72	448	134	54
10	IN9	272	492	134	54
11	IN10	72	544	134	54
12	IN11	272	588	134	54
13	IN12	72	640	134	54
14	IN13	272	684	134	54
15	IN14	72	736	134	54
16	IN15	272	780	134	54
17	IN16	72	832	134	54
18	IN17	272	876	134	54
19	IN18	72	928	134	54
20	IN19	272	972	134	54
21	IN20	72	1024	134	54
22	IN21	272	1068	134	54
23	IN22	72	1120	134	54
24	IN23	272	1164	134	54
25	IN24	72	1216	134	54
26	IN25	272	1260	134	54
27	IN26	72	1312	134	54
28	IN27	272	1356	134	54
29	IN28	72	1408	134	54
30	IN29	272	1452	134	54
31	IN30	72	1504	134	54
32	IN31	272	1548	134	54
33	IN32	72	1600	134	54
34	IN33	272	1644	134	54
35	IN34	72	1696	134	54
36	IN35	272	1740	134	54
37	IN36	72	1792	134	54
38	IN37	272	1836	134	54
39	IN38	72	1888	134	54
40	IN39	272	1932	134	54
41	IN40	72	1984	134	54
42	IN41	272	2028	134	54
43	IN42	72	2080	134	54
44	IN43	272	2124	134	54
45	IN44	72	2176	134	54
46	IN45	272	2220	134	54
47	IN46	72	2272	134	54
48	IN47	272	2316	134	54
49	IN48	72	2368	134	54
50	IN49	272	2412	134	54
51	IN50	72	2464	134	54
52	IN51	272	2508	134	54
53	IN52	72	2560	134	54
54	IN53	272	2604	134	54
55	IN54	72	2656	134	54
56	IN55	272	2700	134	54
57	IN56	72	2752	134	54
58	IN57	272	2796	134	54
59	IN58	72	2848	134	54
60	IN59	272	2892	134	54
61	IN60	72	2944	134	54
62	IN61	272	2988	134	54
63	IN62	72	3040	134	54
64	IN63	272	3084	134	54
65	IN64	72	3136	134	54
66	IN65	272	3180	134	54
67	IN66	72	3232	134	54
68	IN67	272	3276	134	54
69	IN68	72	3328	134	54
70	IN69	272	3372	134	54
71	IN70	72	3424	134	54
72	IN71	272	3468	134	54
73	IN72	72	3520	134	54
74	IN73	272	3564	134	54
75	IN74	72	3616	134	54
76	IN75	272	3660	134	54
77	IN76	72	3712	134	54
78	IN77	272	3756	134	54
79	IN78	72	3808	134	54
80	IN79	272	3852	134	54
81	IN80	72	3904	134	54
82	IN81	272	3948	134	54
83	IN82	72	4000	134	54
84	IN83	272	4044	134	54
85	IN84	72	4096	134	54
86	IN85	272	4140	134	54
87	IN86	72	4192	134	54
88	IN87	272	4236	134	54
89	IN88	72	4288	134	54
90	IN89	272	4332	134	54
91	IN90	72	4384	134	54

92	IN91	272	4428	134	54	146	CALD1	3060	5924	134	54
93	IN92	72	4480	134	54	147	ITH'0	3460	5884	134	54
94	IN93	272	4524	134	54	148	CALSN	3260	5844	134	54
95	IN94	72	4576	134	54	149	CALD0	3060	5804	134	54
96	IN95	272	4620	134	54	150	IDAR'1	3460	5764	134	54
97	IN96	72	4672	134	54	151	IDAR'0	3260	5724	134	54
98	IN97	272	4716	134	54	152	CALI	3060	5684	134	54
99	IN98	72	4768	134	54	153	OUTRH'1	3460	5644	134	54
100	IN99	272	4812	134	54	154	OUTRL'1	3260	5604	134	54
101	IN100	72	4864	134	54	155	DRET'2	3060	5564	134	54
102	IN101	272	4908	134	54	156	OUTRH'0	3460	5524	134	54
103	IN102	72	4960	134	54	157	OUTRL'0	3260	5484	134	54
104	IN103	272	5004	134	54	158	DRET'1	3060	5444	134	54
105	IN104	72	5056	134	54	159	OUT127	3460	5404	134	54
106	IN105	272	5100	134	54	160	OUT126	3260	5364	134	54
107	IN106	72	5152	134	54	161	OUT125	3060	5324	134	54
108	IN107	272	5196	134	54	162	OUT124	3460	5284	134	54
109	IN108	72	5248	134	54	163	OUT123	3260	5244	134	54
110	IN109	272	5292	134	54	164	OUT122	3060	5204	134	54
111	IN110	72	5344	134	54	165	OUT121	3460	5164	134	54
112	IN111	272	5388	134	54	166	OUT120	3260	5124	134	54
113	IN112	72	5440	134	54	167	OUT119	3060	5084	134	54
114	IN113	272	5484	134	54	168	OUT118	3460	5044	134	54
115	IN114	72	5536	134	54	169	OUT117	3260	5004	134	54
116	IN115	272	5580	134	54	170	OUT116	3060	4964	134	54
117	IN116	72	5632	134	54	171	OUT115	3460	4924	134	54
118	IN117	272	5676	134	54	172	OUT114	3260	4884	134	54
119	IN118	72	5728	134	54	173	OUT113	3060	4844	134	54
120	IN119	272	5772	134	54	174	OUT112	3460	4804	134	54
121	IN120	72	5824	134	54	175	OUT111	3260	4764	134	54
122	IN121	272	5868	134	54	176	OUT110	3060	4724	134	54
123	IN122	72	5920	134	54	177	OUT109	3460	4684	134	54
124	IN123	272	5964	134	54	178	OUT108	3260	4644	134	54
125	IN124	72	6016	134	54	179	OUT107	3060	4604	134	54
126	IN125	272	6060	134	54	180	OUT106	3460	4564	134	54
127	IN126	72	6112	134	54	181	OUT105	3260	4524	134	54
128	IN127	279	6155	134	54	182	OUT104	3060	4484	134	54
129	SSGND'0	72	6208	134	54	183	OUT103	3460	4444	134	54
130	SSGND'1	272	6252	134	54	184	OUT102	3260	4404	134	54
131	SSGND'2	526	6218	186	234	185	OUT101	3060	4364	134	54
132	CBUS0'0	761	6215	98	238	186	OUT100	3460	4324	134	54
133	CBUS1'0	954	6216	98	238	187	OUT099	3260	4284	134	54
134	CBUS2'0	1146	6216	98	238	188	OUT098	3060	4244	134	54
135	CBUS3'0	1338	6216	98	238	189	OUT097	3460	4204	134	54
136	GND'0	1578	6218	186	234	190	OUT096	3260	4164	134	54
137	VCC'0	1858	6218	186	234	191	OUT095	3060	4124	134	54
138	VTSEL'0	2098	6216	98	238	192	OUT094	3460	4084	134	54
139	VISET'0	2338	6218	186	234	193	OUT093	3260	4044	134	54
140	VTHN'0	2622	6218	186	234	194	OUT092	3060	4004	134	54
141	VTHP'0	2906	6218	186	234	195	OUT091	3460	3964	134	54
142	CALVN'0	3142	6216	98	238	196	OUT090	3260	3924	134	54
143	CALVP'0	3334	6216	98	238	197	OUT089	3060	3884	134	54
144	ITH'1	3460	6004	134	54	198	OUT088	3460	3844	134	54
145	CALSP	3260	5964	134	54	199	OUT087	3260	3804	134	54

200	OUT086	3060	3764	134	54	253	OUT033	3260	1644	134	54
201	OUT085	3460	3724	134	54	254	OUT032	3060	1604	134	54
202	OUT084	3260	3684	134	54	255	OUT031	3460	1564	134	54
203	OUT083	3060	3644	134	54	256	OUT030	3260	1524	134	54
204	OUT082	3460	3604	134	54	257	OUT029	3060	1484	134	54
205	OUT081	3260	3564	134	54	258	OUT028	3460	1444	134	54
206	OUT080	3060	3524	134	54	259	OUT027	3260	1404	134	54
207	OUT079	3460	3484	134	54	260	OUT026	3060	1364	134	54
208	OUT078	3260	3444	134	54	261	OUT025	3460	1324	134	54
209	OUT077	3060	3404	134	54	262	OUT024	3260	1284	134	54
210	OUT076	3460	3364	134	54	263	OUT023	3060	1244	134	54
211	OUT075	3260	3324	134	54	264	OUT022	3460	1204	134	54
212	OUT074	3060	3284	134	54	265	OUT021	3260	1164	134	54
213	OUT073	3460	3244	134	54	266	OUT020	3060	1124	134	54
214	OUT072	3260	3204	134	54	267	OUT019	3460	1084	134	54
215	OUT071	3060	3164	134	54	268	OUT018	3260	1044	134	54
216	OUT070	3460	3124	134	54	269	OUT017	3060	1004	134	54
217	OUT069	3260	3084	134	54	270	OUT016	3460	964	134	54
218	OUT068	3060	3044	134	54	271	OUT015	3260	924	134	54
219	OUT067	3460	3004	134	54	272	OUT014	3060	884	134	54
220	OUT066	3260	2964	134	54	273	OUT013	3460	844	134	54
221	OUT065	3060	2924	134	54	274	OUT012	3260	804	134	54
222	OUT064	3460	2884	134	54	275	OUT011	3060	764	134	54
223	OUT063	3260	2844	134	54	276	OUT010	3460	724	134	54
224	OUT062	3060	2804	134	54	277	OUT009	3260	684	134	54
225	OUT061	3460	2764	134	54	278	OUT008	3060	644	134	54
226	OUT060	3260	2724	134	54	279	OUT007	3460	604	134	54
227	OUT059	3060	2684	134	54	280	OUT006	3260	564	134	54
228	OUT058	3460	2644	134	54	281	OUT005	3060	524	134	54
229	OUT057	3260	2604	134	54	282	OUT004	3460	484	134	54
230	OUT056	3060	2564	134	54	283	OUT003	3260	444	134	54
231	OUT055	3460	2524	134	54	284	OUT002	3060	404	134	54
232	OUT054	3260	2484	134	54	285	OUT001	3460	364	134	54
233	OUT053	3060	2444	134	54	286	OUT000	3260	324	134	54
234	OUT052	3460	2404	134	54	287	DRET'0	3060	284	134	54
235	OUT051	3260	2364	134	54	288	CALVP'1	3342	82	98	154
236	OUT050	3060	2324	134	54	289	CALVN'1	3150	82	98	154
237	OUT049	3460	2284	134	54	290	VTHP'1	2914	82	186	154
238	OUT048	3260	2244	134	54	291	VTHN'1	2630	82	186	154
239	OUT047	3060	2204	134	54	292	VIISET'1	2346	82	186	154
240	OUT046	3460	2164	134	54	293	VTSEL'1	2106	82	98	154
241	OUT045	3260	2124	134	54	294	VCC'1	1866	82	186	154
242	OUT044	3060	2084	134	54	295	GND'1	1586	82	186	154
243	OUT043	3460	2044	134	54	296	CBUS3'1	1346	82	98	154
244	OUT042	3260	2004	134	54	297	CBUS2'1	1154	82	98	154
245	OUT041	3060	1964	134	54	298	CBUS1'1	962	82	98	154
246	OUT040	3460	1924	134	54	299	CBUS0'1	770	82	98	154
247	OUT039	3260	1884	134	54	300	SSGND'3	534	82	186	154
248	OUT038	3060	1844	134	54	301	VCSP	3479	207	92	156
249	OUT037	3460	1804	134	54	302	VCSP2	2631	215	140	44
250	OUT036	3260	1764	134	54	303	VCSN	2147	219	140	52
251	OUT035	3060	1724	134	54	304	VX	1205	223	152	60
252	OUT034	3460	1684	134	54	305	VQ4	841	219	120	52

Table 3: Tabulation of Simulated Detector Signal

Time [ns]	Current [μA]	8.5	0.4317	18.5	0.0068
-1.0	0.0000	9.0	0.3383	19.0	0.0064
-0.5	0.0000	9.5	0.1628	19.5	0.0060
0.0	0.0000	10.0	0.0253	20.0	0.0056
0.5	0.1850	10.5	0.0195	20.5	0.0052
1.0	0.3931	11.0	0.0183	21.0	0.0048
1.5	0.4027	11.5	0.0172	21.5	0.0044
2.0	0.4025	12.0	0.0161	22.0	0.0040
2.5	0.4055	12.5	0.0151	22.5	0.0037
3.0	0.4124	13.0	0.0142	23.0	0.0033
3.5	0.4242	13.5	0.0133	23.5	0.0030
4.0	0.4373	14.0	0.0125	24.0	0.0027
4.5	0.4489	14.5	0.0117	24.5	0.0024
5.0	0.4615	15.0	0.0110	25.0	0.0021
5.5	0.4675	15.5	0.0103	25.5	0.0017
6.0	0.4709	16.0	0.0096	26.0	0.0013
6.5	0.4718	16.5	0.0090	26.5	0.0008
7.0	0.4725	17.0	0.0084	27.0	0.0002
7.5	0.4665	17.5	0.0078	27.5	0.0000
8.0	0.4588	18.0	0.0073		

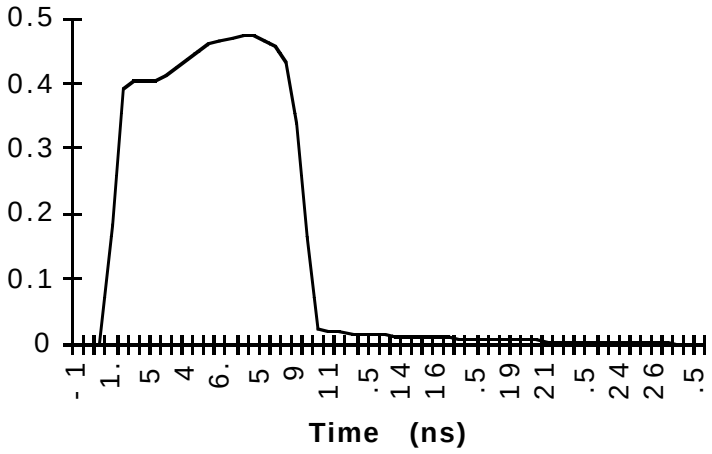

Figure 6: Simulated Depleted Detector n-Strip Signal
Signal is for an irradiated n-strip detector. For an unirradiated detector, the time scale should be scaled shorter by the ratio 0.60.
[See reference (9) J. Leslie, et al.]

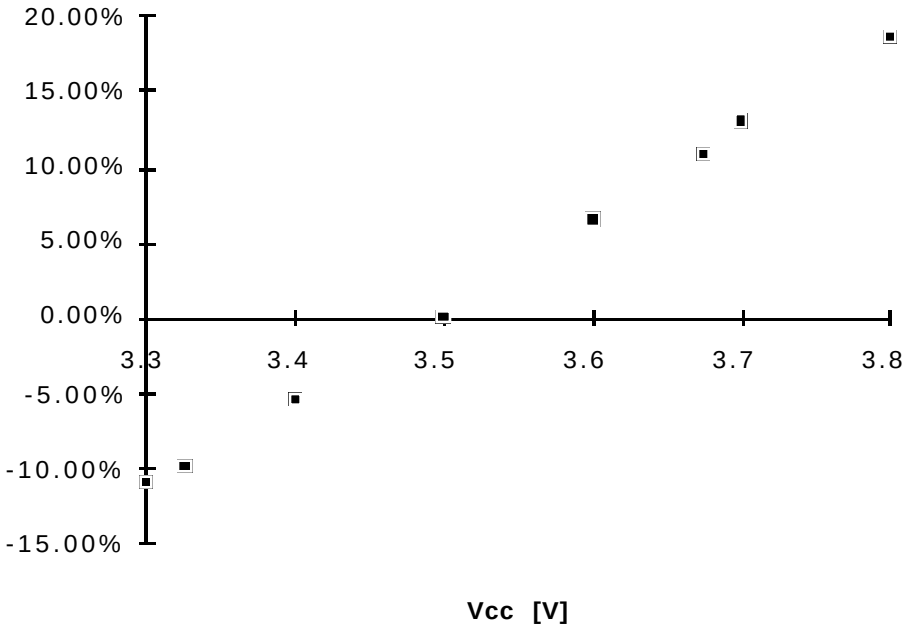

Figure 7: Simulated Gain Sensitiviy to Vcc for 1 fC signal